**Computer-Aided VLSI System Design**

**Homework 5 Report**

**Due Tuesday, Dec. 5, 14:00**

**Student ID: R12K41025**

**Student Name: 杜冠廷**

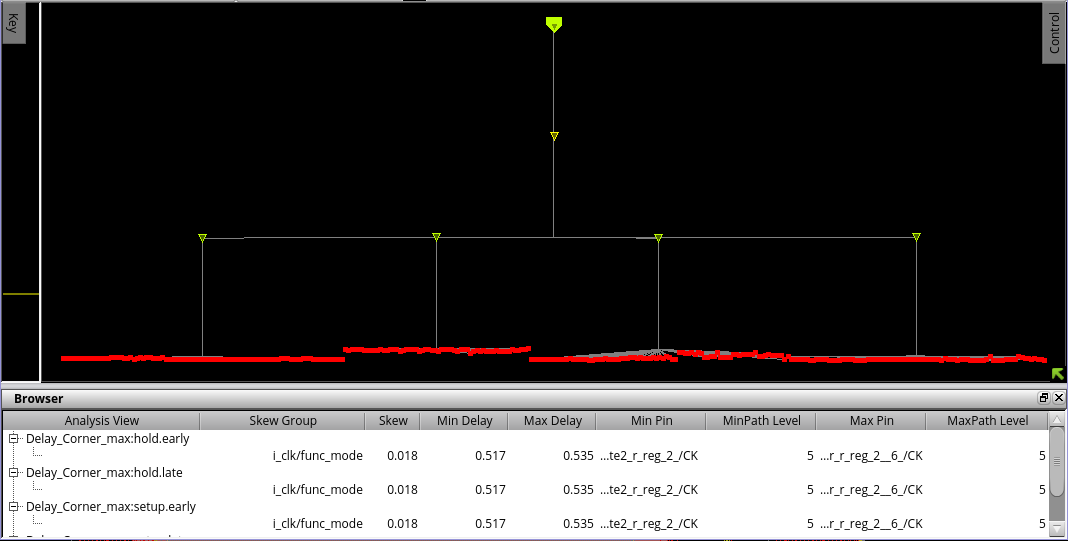
**APR Results**

1. Fill in the blanks below.

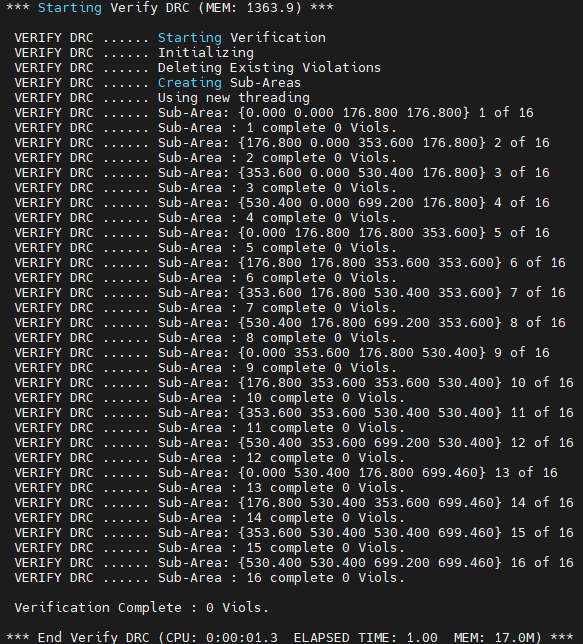
|  |  |  |
| --- | --- | --- |
| Design Stage | Description | Value |
| P&R | Number of DRC violations (ex: 0)  (Verify -> Verify Geometry…) | 0 |
| Number of LVS violations (ex: 0)  (Verify -> Verify Connectivity…) | 0 |
| Die Area (um2) | 489062.43 |
| Core Area (um2) | 290445.51 |
| Post-layout  Simulation | Clock Period for Post-layout Simulation (ex. 10ns) | 5.0 |
| Follow your design in HW3?  (If not, specify student ID of the designer or ‘from TA’) | | From TA |

**Questions and Discussion**

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).

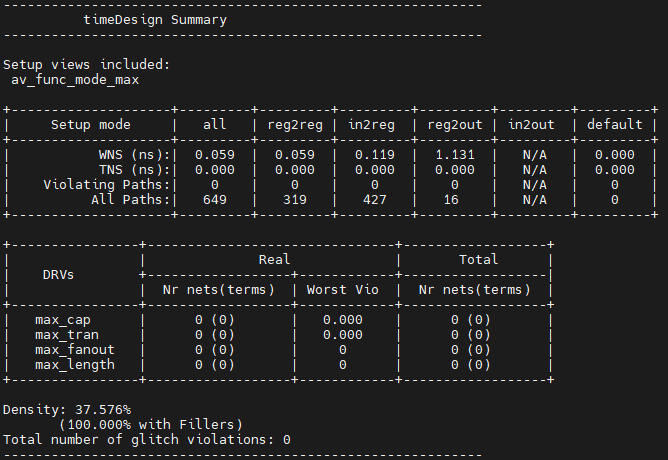


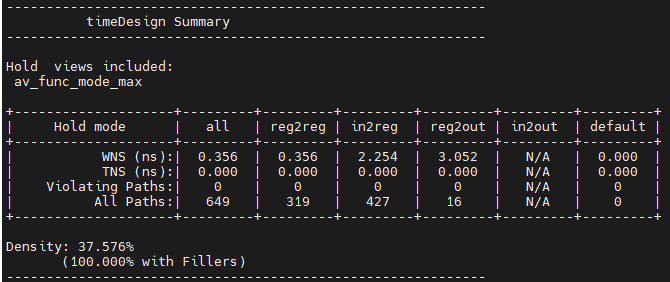
1. Attach the snapshot of DRC and LVS checking after routing. (5%)





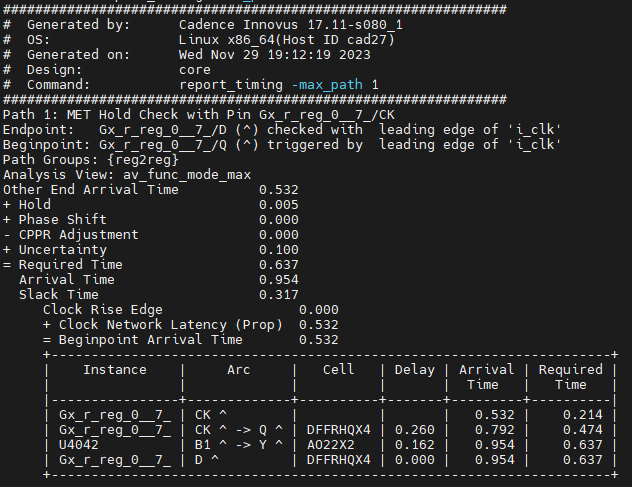
1. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)



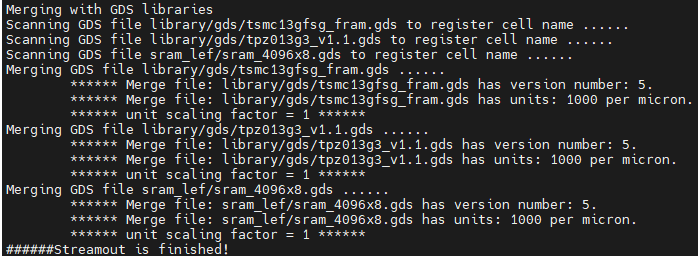


1. Show the critical path after post-route optimization. What is the path type? (10%)

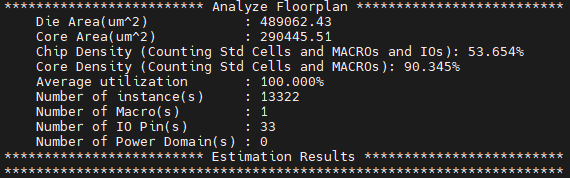
(The slack of the critical path should match the smallest slack in the timing report)



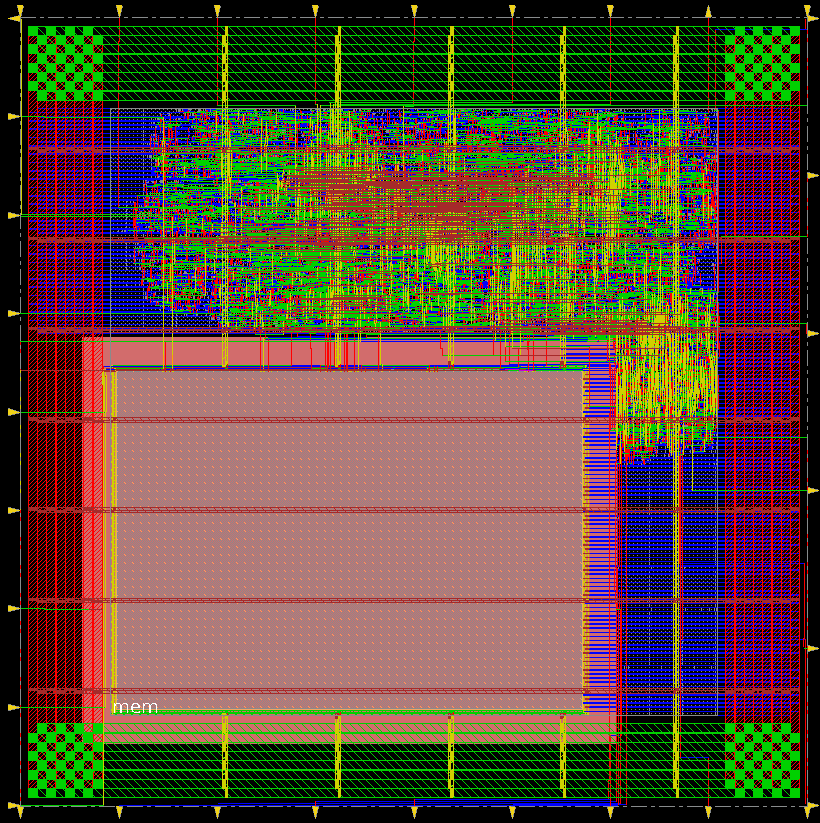
1. Attach the snapshot of GDS stream out messages. (10%)



1. Attach the snapshot of the final area result. (5%)



1. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



1. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

In this design, there is only one 4096x8 SRAM, and it is placed at the boundary of the core to ensure it receives a sufficient power supply. Additionally, all macros are positioned at the corners to simplify routing whenever possible.