Microprocessor Architecture and Interfacing

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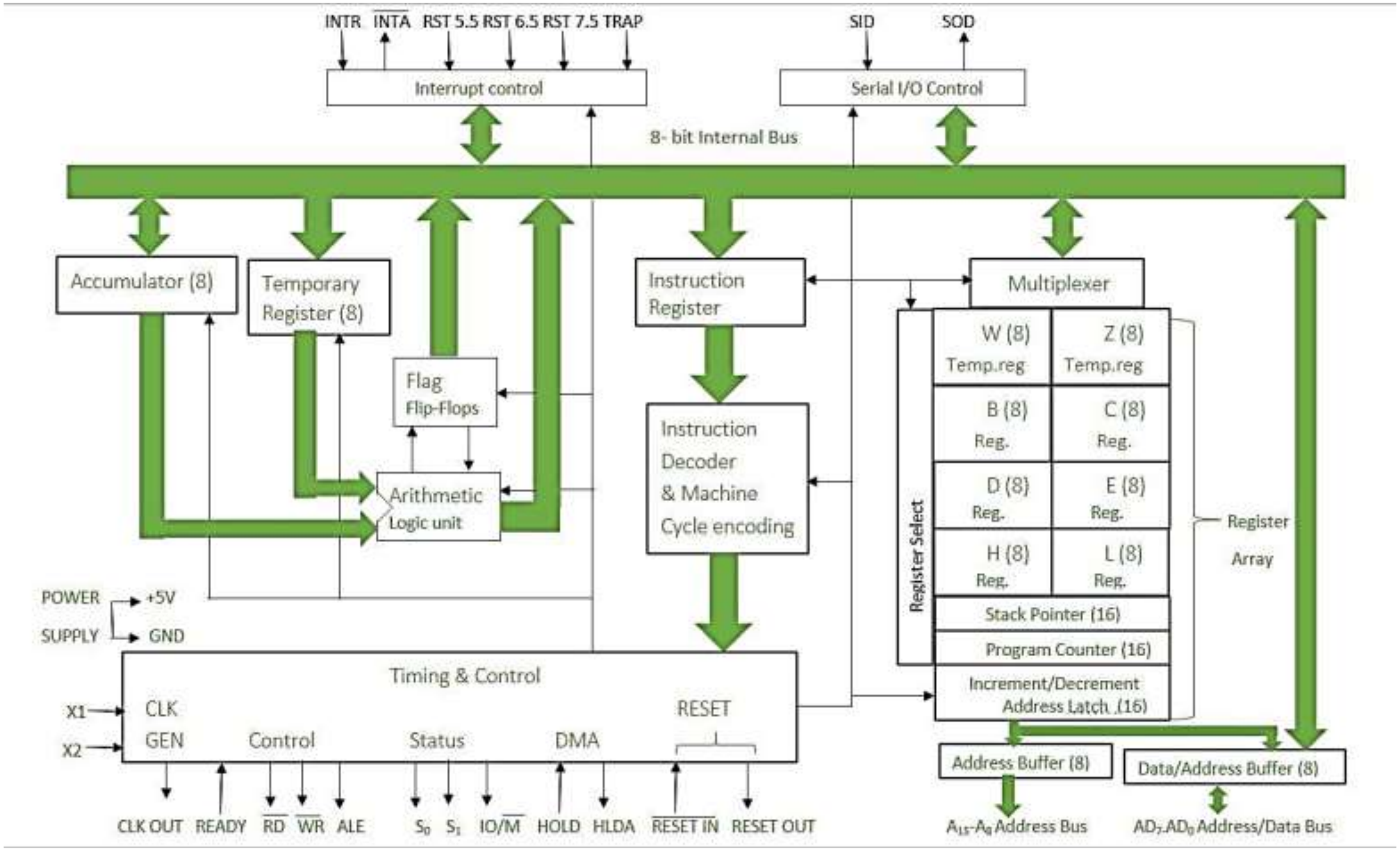
Microprocessor architecture and its operations



8085 Microprocessor Architecture

Microprocessor architecture and its operations

Arithmetic Logic Unit (ALU)
The ALU is responsible for performing arithmetic and logical operations on data. It can perform operations such as addition, subtraction, logical AND, logical OR, and more. The ALU operates on 8-bit data and provides flags to indicate conditions such as zero, carry, sign, and parity.

Control Unit (CU)
The Control Unit coordinates and controls the activities of the other functional units within the microprocessor. It generates timing and control signals to synchronize the execution of instructions and manage data transfer between different units.

Instruction Decoder
The Instruction Decoder decodes the instructions fetched from memory. It determines the type of instruction being executed and generates control signals accordingly. The decoded instructions guide the microprocessor in executing the appropriate operations.

Microprocessor architecture and its operations

Registers

The 8085 microprocessor has several registers that serve different purposes:

- **Accumulator (A):** The Accumulator is an 8-bit register used for storing intermediate results during arithmetic and logical operations.
- **General Purpose Registers (B, C, D, E, H, L):** These are six 8-bit registers that can be used for various purposes, including storing data and performing operations.
- **Special Purpose Registers (SP, PC):** The Stack Pointer (SP) is used to manage the stack in memory and the program counter (PC) keeps track of the memory address of the following instruction for fetching.

Address and Data Bus

The microprocessor uses a bidirectional address bus to specify the memory location or I/O device it wants to access. Similarly, it employs an 8-bit bidirectional data bus for transferring data between the microprocessor and memory or I/O devices.

Microprocessor architecture and its operations

Timing and Control Unit

The Timing and Control Unit generates the necessary timing signals to synchronize the activities of the microprocessor. It produces signals such as RD (Read), WR (Write), and various control signals required for instruction execution.

Interrupt Control Unit

The Interrupt Control Unit manages interrupts in the 8085 microprocessor. It handles external interrupt signals and facilitates interrupt-driven operations by interrupting the normal execution flow of the program and branching to specific interrupt service routines.

Memory Interface

The Memory Interface connects the microprocessor to the memory system. It manages the address and data transfers between the microprocessor and the memory chips, including Read and Write operations.

Microprocessor architecture and its operations

Interrupts:

The 8085 microprocessor supports 5 hardware interrupts as follows:

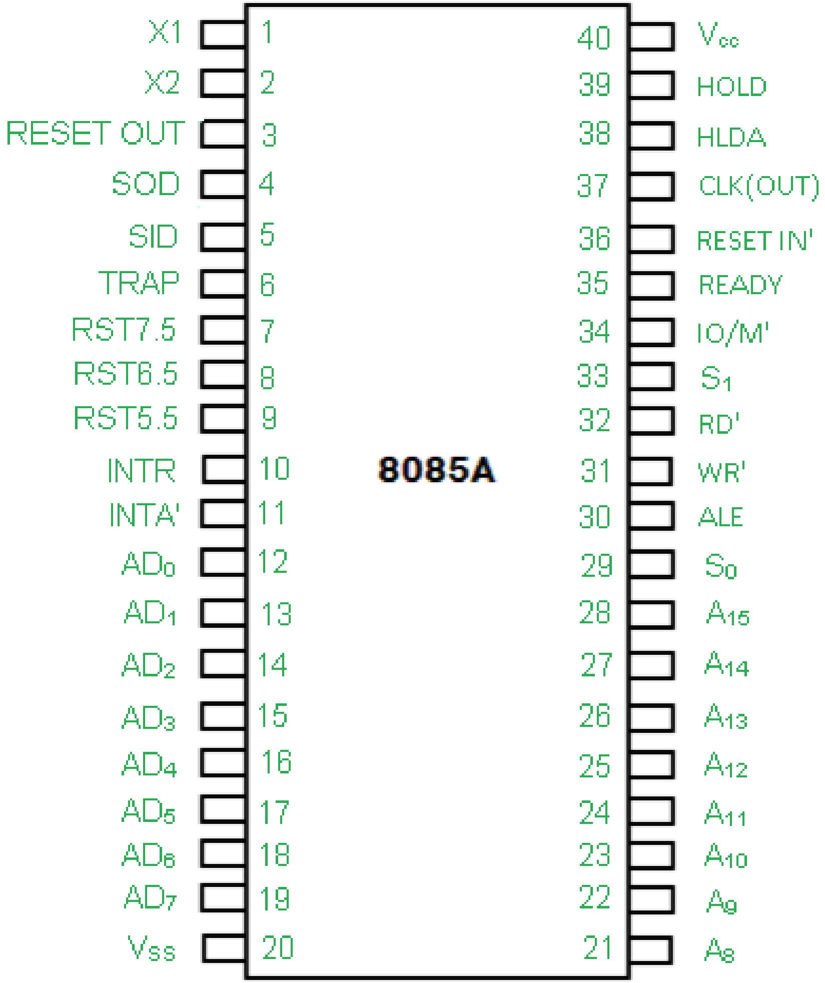
- INTR
- RST 5.5
- RST 6.5
- RST 7.5
- TRAP

Interrupts allow the microprocessor to respond to external events and handle them in a prioritized manner.

Input/Output (I/O) Ports:

The 8085 microprocessor has a limited number of I/O pins. It uses I/O ports to connect with external devices for input and output operations.

Microprocessor architecture and its operations



1 Address Bus and Data Bus:

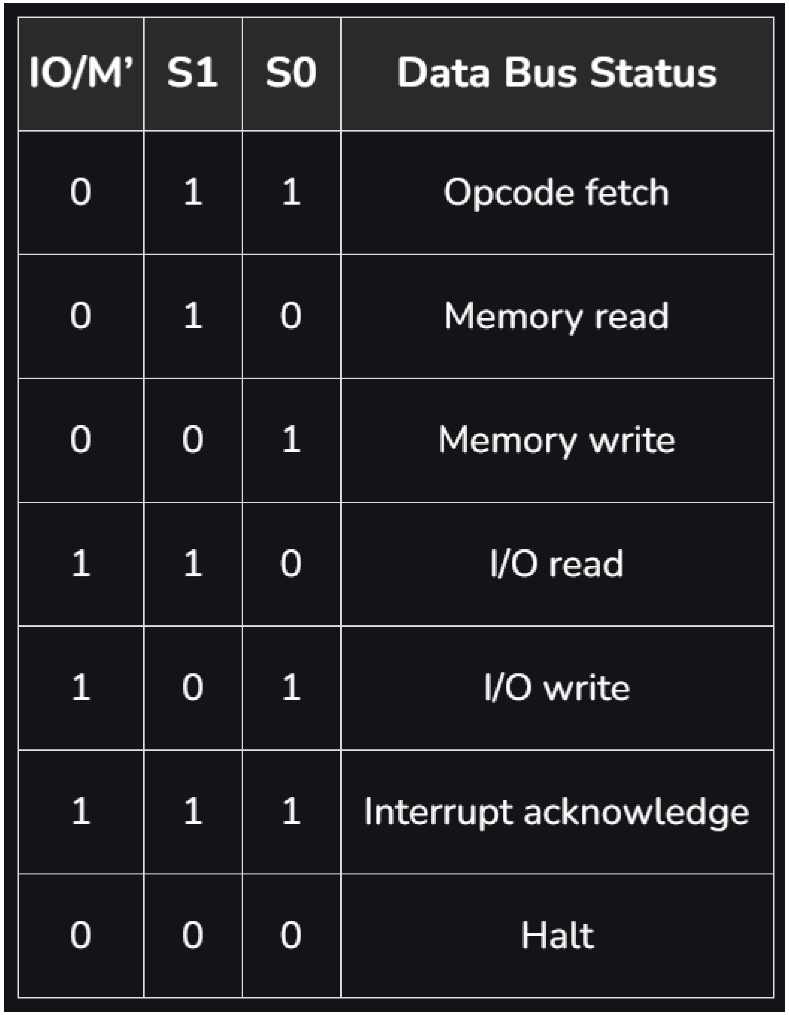
Address Bus (A8 to A15): The address bus is unidirectional, i.e., bits flow in one direction from the microprocessor unit to the peripheral devices and uses the higher order address bus.

Address Data Bus (AD0 to AD7): These are bi-directional data pins used to transfer data between the microprocessor and memory or I/O devices. The microprocessor is an 8-bit processor, so it uses 8 data lines. These pins serve the dual purpose of transmitting lower order address and data byte. During 1st clock cycle, these pins act as lower half of address. In remaining clock cycles, these pins act as data bus.

Microprocessor architecture and its operations

2 Control and Status Signals

- **ALE:** It is an Address Latch Enable signal. It goes high during first T state of a machine cycle and enables the lower 8-bits of the address, if its value is 1 otherwise data bus is activated.
- **IO/M’:** It is a status signal which determines whether the address is for input-output or memory. When it is high(1) the address on the address bus is for input-output devices. When it is low(0) the address on the address bus is for the memory.
- **SO, S1:** These are status signals. They distinguish the various types of operations such as halt, reading, instruction fetching or writing.



IO/M’	S1	S0	Data Bus Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt acknowledge
0	0	0	Halt

Microprocessor architecture and its operations

- **RD' –** It is a signal to control READ operation. When it is low the selected memory or input-output device is read.
- **WR' –** It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.
- **READY –** It senses whether a peripheral is ready to transfer data or not. If READY is high(1) the peripheral is ready. If it is low(0) the microprocessor waits till it goes high. It is useful for interfacing low speed devices.

3 Power Supply and Clock Frequency

- **Vcc:** +5v power supply
- **Vss:** Ground Reference
- **XI, X2:** A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3MHZ the crystal should have frequency of 6MHZ.
- **CLK (OUT):** This signal can be used as the system clock for other devices.

Microprocessor architecture and its operations

Interrupts and Peripheral Initiated Signals: The 8085 has five interrupt signals that can be used to interrupt a program execution.

- INTR
- RST 7.5
- RST 6.5
- RST 5.5
- TRAP

The microprocessor acknowledges Interrupt Request by INTA’ signal. In addition to Interrupts, there are three externally initiated signals namely RESET, HOLD and READY. To respond to HOLD request, it has one signal called HLDA.

- **INTR (Interrupt Request):** This pin is used to request an interrupt from an external device.
- **RST7.5, RST6.5, RST5.5:** These are vectored interrupts with different priority levels.
- **TRAP:** This is a non-maskable interrupt and has the highest priority.
- **INTA (Interrupt Acknowledge):** This pin is used to acknowledge interrupts from external devices.

Microprocessor architecture and its operations

Reset Signals

- RESET IN – When the signal on this pin is low(0), the program-counter is set to zero, the microprocessor unit is reset.
- RESET OUT – This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

DMA Signals

- HOLD – It indicates that another device is requesting the use of the address and data bus. Having received HOLD request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed. Internal processing may continue. After the removal of the HOLD signal the processor regains the bus.
- HLDA – It is a signal which indicates that the hold request has been received after the removal of a HOLD request, the HLDA goes low.

Microprocessor architecture and its operations

Serial I/O Ports: Serial transmission in 8085 is implemented by the two signals.

- SID and SOD – SID is a data line for serial input whereas SOD is a data line for serial output.

Features of 8085 Microprocessor:

- 8-bit Processor: Processes 8 bits of data at a time.
- 16-bit Address Bus: Can address up to 64 KB of memory.
- 5 MHz Clock Speed: Provides a decent processing speed for basic tasks.
- **Low Power Consumption:** Ideal for embedded systems with minimal power needs.
- Interrupt System: Features 5 interrupt pins for external signal response.

Memory and I/O devices

Memory is used to store instructions and data. In 8085, memory is addressed using 16-bit addresses, allowing access to 64 KB of memory.

Types of Memory

- ROM (Read-Only Memory):
  - Stores firmware or permanent programs like the bootstrap program.
  - Non-volatile (data is retained even after power off).
- RAM (Random Access Memory):
  - Stores temporary data and instructions during execution.
  - Volatile (data is lost when power is off).

Memory Interfacing with 8085

- Address Bus (A0–A15): 16-bit bus for addressing memory locations.
- Data Bus (D0–D7): 8-bit bus to transfer data to/from memory.

Memory and I/O devices

Control Signals:

- R$\overline{D}$ (Read): Active low signal, used when data is to be read.
- W$\overline{R}$ (Write): Active low signal, used when data is to be written.
- ALE (Address Latch Enable): Helps separate address and data on AD0–AD7 lines.

Address/Data Bus Multiplexing:

- Lower 8 bits (A0–A7) are multiplexed with D0–D7 to reduce pin count.
- A latch is used to separate the address from the data.

I/O devices are used for communication between the microprocessor and external peripherals like keyboards, displays, printers, etc.
Two Types of I/O Addressing

- **Memory-Mapped I/O:** I/O devices are treated as memory locations.Uses 16-bit addressing.Allows full memory instructions (like MOV, LDA, STA, etc.).Slower but more flexible.
- **I/O-Mapped I/O (Isolated I/O):** Separate address space for I/O.Only 8-bit addresses (can address 256 I/O devices).Uses specific I/O instructions like IN and OUT.Faster, but limited instruction set.

Memory and I/O devices

I/O Control Signals

- IO/$\overline{\text{M}}$ (I/O or Memory):
  - High → I/O operation.
  - Low → Memory operation.
- R$\overline{\text{D}}$ and W$\overline{\text{R}}$ are also used with IO/$\overline{\text{M}}$ to determine the type of operation:

IO/$\overline{\text{M}}$	**R$\overline{\text{D}}$**	**W$\overline{\text{R}}$**	**Operation**
0	0	1	Memory Read
0	1	0	Memory Write
1	0	1	I/O Read
1	1	0	I/O Write

Interfacing I/O Devices

Devices like LEDs, 7-segment displays, LCDs, ADC/DAC, and keyboards are connected using I/O ports. These ports are accessed using:

- IN port address – to read from an input device.
- OUT port address – to send data to an output device.

Memory and I/O devices

Feature	Memory Interfacing	I/O Interfacing (Isolated)
Address Lines	16-bit (64 KB)	8-bit (256 devices)
Instructions Used	General data transfer	IN, OUT
Address Space Shared	Yes (same as program/data)	No (separate space)
Speed	Comparatively slower	Faster
Flexibility	More (full instruction set)	Less (only IN/OUT)

Memory interfacing

- **Memory interfacing** is the process of connecting external memory devices, such as RAM (Random Access Memory) and ROM (Read-Only Memory), to the 8085 microprocessor. The interfacing allows the microprocessor to access and store data, as well as execute programs stored in memory.
- **Address Bus and Data Bus**
  - Address Bus (A0–A15):
    - The 8085 has a 16-bit address bus, which allows it to address 64 KB of memory.
    - The address bus carries the memory address of the location where the data is either to be read or written.
  - Data Bus (D0–D7):
    - The 8-bit data bus carries the data between the 8085 and the memory.
    - It is responsible for transferring 8 bits of data at a time.

Memory interfacing

Control Signals

- ALE (Address Latch Enable):
  - This is used to latch the lower 8 bits of the address (A0–A7) from the multiplexed address/data lines (AD0–AD7) into a latch.
  - When ALE is high, the address is valid and should be latched.
- $R\overline{D}$ (Read):
  - The $R\overline{D}$ signal is active low, and it indicates when the microprocessor is performing a read operation.
  - When $R\overline{D}$ is low, data is read from the memory.
- $W\overline{R}$ (Write):
  - The $W\overline{R}$ signal is active low, and it indicates when the microprocessor is performing a write operation.
  - When $W\overline{R}$ is low, data is written into memory.
- $IO/\overline{M}$ (I/O or Memory):
  - The $IO/\overline{M}$ signal indicates whether the operation is related to memory or I/O.
  - When $IO/\overline{M}$ = 0, the operation is related to memory, and when $IO/\overline{M}$ = 1, it indicates an I/O operation.

Memory interfacing

Memory Mapping

To interface memory with the 8085, we need to connect the address lines (A0–A15) and the data lines (D0–D7) to the memory chip. The address lines map to the address space of the microprocessor.

ROM Interfacing:

- ROM is typically used to store the program code, and it can be mapped to a specific range of addresses in memory.
- The 8085 uses **16-bit addressing**, so ROM can occupy a block of memory (for example, from address 0000H to FFFFH).

RAM Interfacing:

- RAM stores the variables and temporary data during program execution.
- Like ROM, RAM is also mapped to a range of addresses, but it may use only part of the available address space (for example, 0000H to 1FFFH for 8 KB of RAM).

Memory interfacing

Interfacing RAM (Read Operation)

For an 8 KB RAM,

- The address lines A0 to A12 are used to access the 8 KB memory (since 213=82 13 =8 KB).
- The microprocessor sends the address to the address bus.
- The data is transferred from the memory to the microprocessor over the data bus.

Steps for a read operation:

- The address is placed on the address bus (A0 to A15).
- The ALE signal is activated to latch the lower 8 bits of the address (A0 to A7) from the multiplexed address/data lines (AD0 to AD7).
- The microprocessor sends the R$\overline{D}$ signal to initiate a read operation.
- The data is then placed on the data bus (D0–D7) from the memory, which the 8085 reads.

Memory interfacing

Interfacing RAM (Write Operation)

- For an 8 KB RAM, the process of writing data from the microprocessor to memory is as follows:

Steps for a write operation:

- The address is placed on the address bus (A0 to A15).
- The ALE signal is activated to latch the address (A0 to A7).
- The microprocessor sends the $W\overline{R}$ signal to initiate a write operation.
- The data to be written is placed on the data bus (D0–D7).The memory stores the data at the specified address.

Interfacing I/O Devices

- Interfacing Input/Output (I/O) devices with the 8085 microprocessor allows it to communicate with external devices such as keyboards, displays, ADCs (Analog-to-Digital Converters), DACs (Digital-to-Analog Converters), sensors, etc. There are two common methods for I/O interfacing in the 8085 microprocessor: Memory-Mapped I/O and I/O-Mapped I/O (also called Isolated I/O).

Memory-Mapped I/O: In this method, I/O devices are treated as part of the memory. The microprocessor can use memory instructions (MOV, LDA, STA, etc.) to interact with I/O devices.

- Address Range: The I/O devices are assigned an address within the 64 KB address space. This means that I/O devices share the same address space as memory.
- Memory Instructions: Since I/O devices are mapped into the same address space, the microprocessor uses normal memory access instructions to read and write data.

Interfacing I/O Devices

Advantages of Memory-Mapped I/O:

- Uses standard memory instructions (MOV, LDA, STA, etc.), simplifying the programming.
- No need for special I/O instructions like IN and OUT.

Disadvantages of Memory-Mapped I/O:

- Less efficient use of address space since the I/O devices are sharing the memory address space, which limits the number of devices you can interface (because the microprocessor can address only 64 KB).

I/O-Mapped I/O (Isolated I/O): In this method, the I/O devices are assigned a separate address space distinct from memory. This method uses special I/O instructions to access these devices.

- Address Range: I/O devices are assigned addresses in a separate I/O address space, which is typically 256 I/O locations (using 8 bits for the address, so 28=2562 8 =256 I/O devices can be accessed).
- I/O Instructions: To interact with I/O devices, the 8085 uses special instructions like IN (Input) and OUT (Output).

Interfacing I/O Devices

Advantages of I/O-Mapped I/O:

- The full memory address space is available for RAM and ROM, which can be useful for larger systems.
- Separate address space for I/O devices makes it easier to manage memory and I/O devices.

Disadvantages of I/O-Mapped I/O:

- Requires special instructions (IN and OUT), which might be less convenient compared to memory-mapped I/O.

Example 1: Interfacing an LED Display (Output Device)

Step 1: Assign an I/O Port for the LED

- We will use port 01H to interface the LEDs.
- The microprocessor will send data (8 bits) to port 01H, which will turn the LEDs on or off depending on the value.

Step 2: Writing to the LED Display (OUT Instruction)

- To turn on or off an LED, we will use the OUT instruction. For example, sending FFH (all bits high) will turn on all LEDs, and sending 00H (all bits low) will turn off all LEDs.

```
MVI A, 0FFH   ; Load accumulator with 0FFH (turn on all LEDs)
OUT 01H       ; Send data to port 01H to turn on LEDs
```

Step 3: Reading Data from an Input Device (IN Instruction)If you want to read data from an input device (e.g., a switch or sensor), you can use the IN instruction to read the data from the I/O port. For example, reading the data from port 02H (connected to a sensor)

```
IN 02H        ; Read data from I/O port 02H into accumulator
```

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