

18/06/24

EXPERIMENT-12

- Aim: Design a 4:1 MUX with basic gates at circuit diagram or schematic with sizes of gates used in MUX Cleared labeled next to the devices. Plot a waveform showing output of MUX with different select input.
- Theory: A 4:1 multiplexer can be designed using three 2:1 mux. The 4:1 MUX has four input lines, two selector lines, and one output. The 2:1 MUX has two inputs, one select input, and one output. The design uses one 2:1 MUX in the first level and another in the second level. The outputs in the second level are connected as inputs to the third MUX. The two select lines, one from each set of MUXs, are connected together. The selection of which input is directed to the output is controlled by the select lines.
- Procedure:
 - Do the schematic of inverter and NAND in different cell view
 - Now make them as symbol
 - Create → Cell view → from cellview → OK
 - To view → symbol → modify the position of pins → OK
 - Rename as 4/1 as per size of inverter
 - Rename as inverter

Experiment No.

Date:

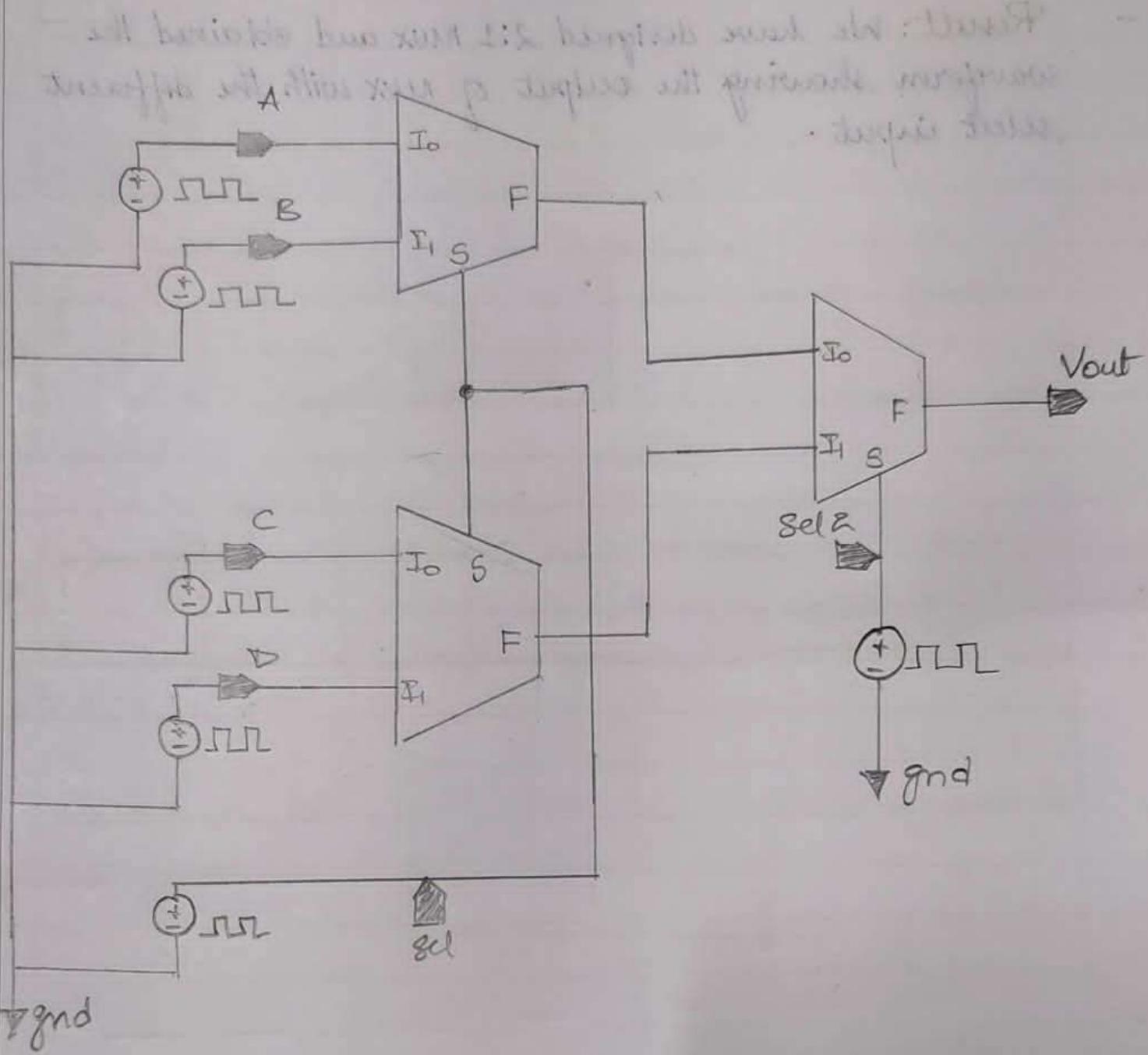
Name of the Experiment :

Page No.:

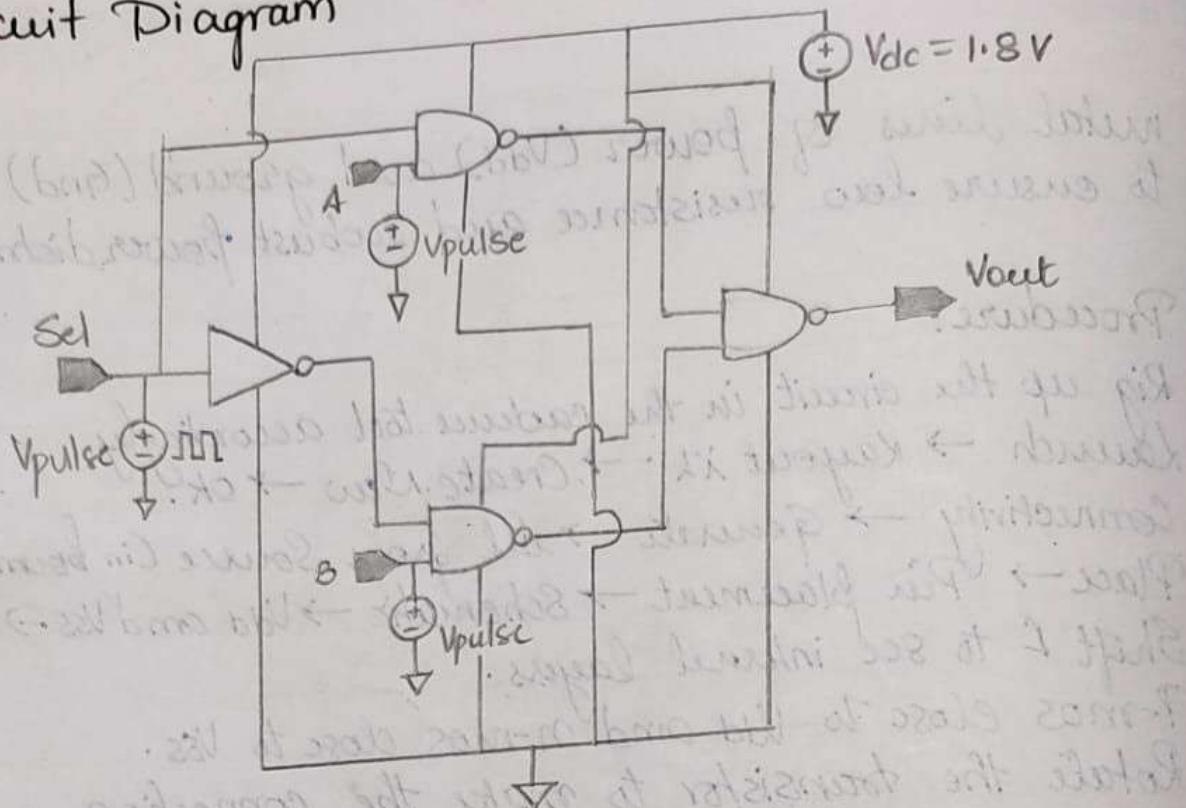
- To view → Symbol → modify the position of pins → ok
- Rename as 4/1 as per size of inverter
- Rename as inverter.
- Using the lines create the symbol and save.
- In the library manager the symbol will be saved.
- Similarly, do it for the nand gate.
- In a new cell view, using the created symbols of inverter and nand gate, make the schematic of the mux.
- To 'Y_P' of inverter give the pin as 'sel'.
- To 'O_P' of the nand gate give the pin as 'V_{out}'
- To the nand gate give the pin as 'A' and 'B'
- Give the V_{dc} and ground where ever required
- Perform the transient analysis and verify the output.

- Result:

Circuit Diagram



Circuit Diagram



V_{pulse} for A

$DC = 1.8V$ Pulse width = 10mscc

$V_{tg1} = 0V$ Rise time = 10fs

$V_{tg2} = 1.8V$ fall time = 10fs

Period = 20mscc

V_{pulse} for B

$DC = 1.8V$ Pulse width = 5mscc

$V_{tg1} = 0V$ Rise time = 10fs

$V_{tg2} = 1.8V$ fall time = 10fs

Period = 10mscc.

Analysis

Transient analysis

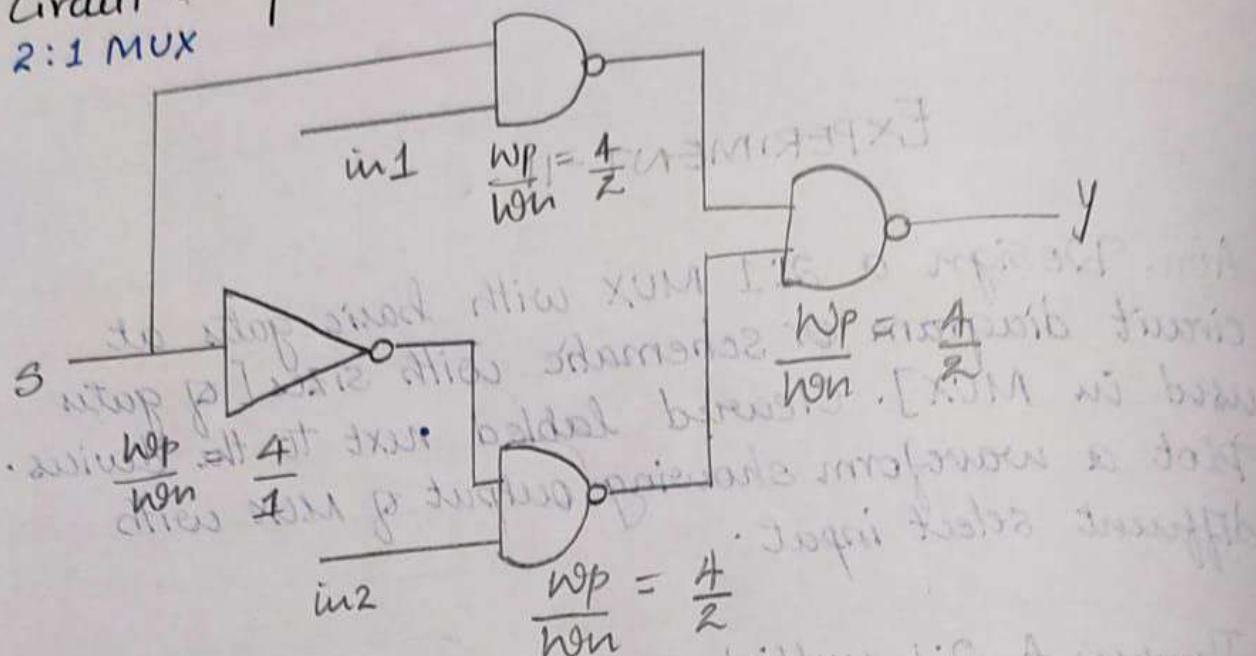
Stop time = 100ms and moderate

85|05|24

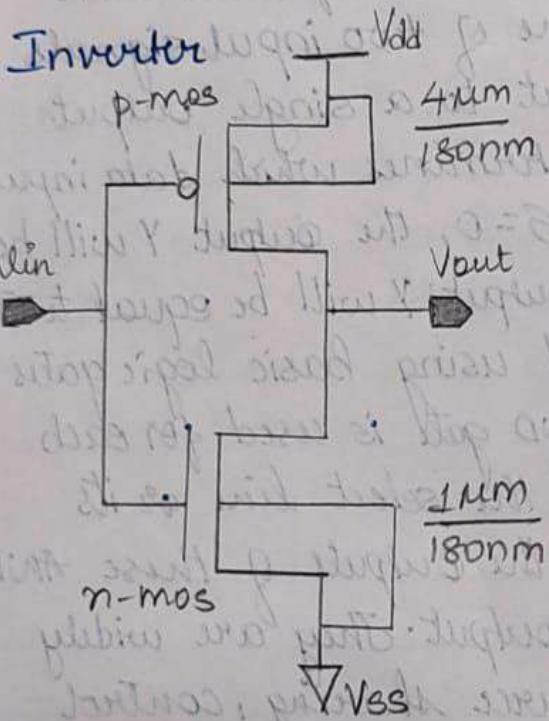
EXPERIMENT - II

- Aim: Design a 2:1 MUX with basic gates at circuit diagram or schematic with sizes [of gates used in MUX]. Cleared labeled next to the devices. Plot a waveform showing output of MUX with different select input.
 - Theory: A 2:1 multiplexer [MUX] is a fundamental digital switch that selects one of two input signals and forwards the selected input to a single output line. Here, the select input S determines which data input is connected to the output, if $S=0$, the output Y will be equal to I_0 , if $S=1$, the output Y will be equal to I_1 . A 2:1 MUX can be implemented using basic logic gates like AND, OR and NOT. An AND gate is used for each data input in combination with the select line or its inverse. An OR gate combines the outputs of these AND gates to produce the final output. They are widely used in data routing, resource sharing, control systems, arithmetic operations.
 - Procedure:
 - Do the Schematic of inverter and NAND in different cell views.
 - Now make them as symbol
 - Create → Cell view → from cell view → OK

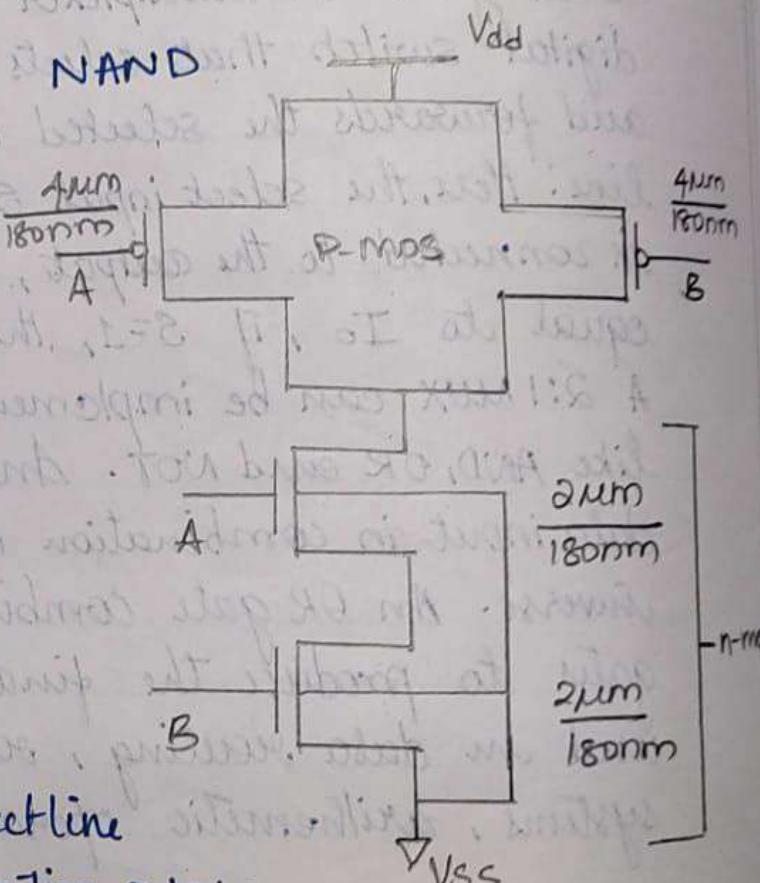
Circuit Diagram 2:1 MUX



Inverter



NAND



Parameters: Vpulse for Selectline

$$DC = 1.8V$$

$$V_{tg1} = 0V$$

$$V_{tg2} = 1.8V$$

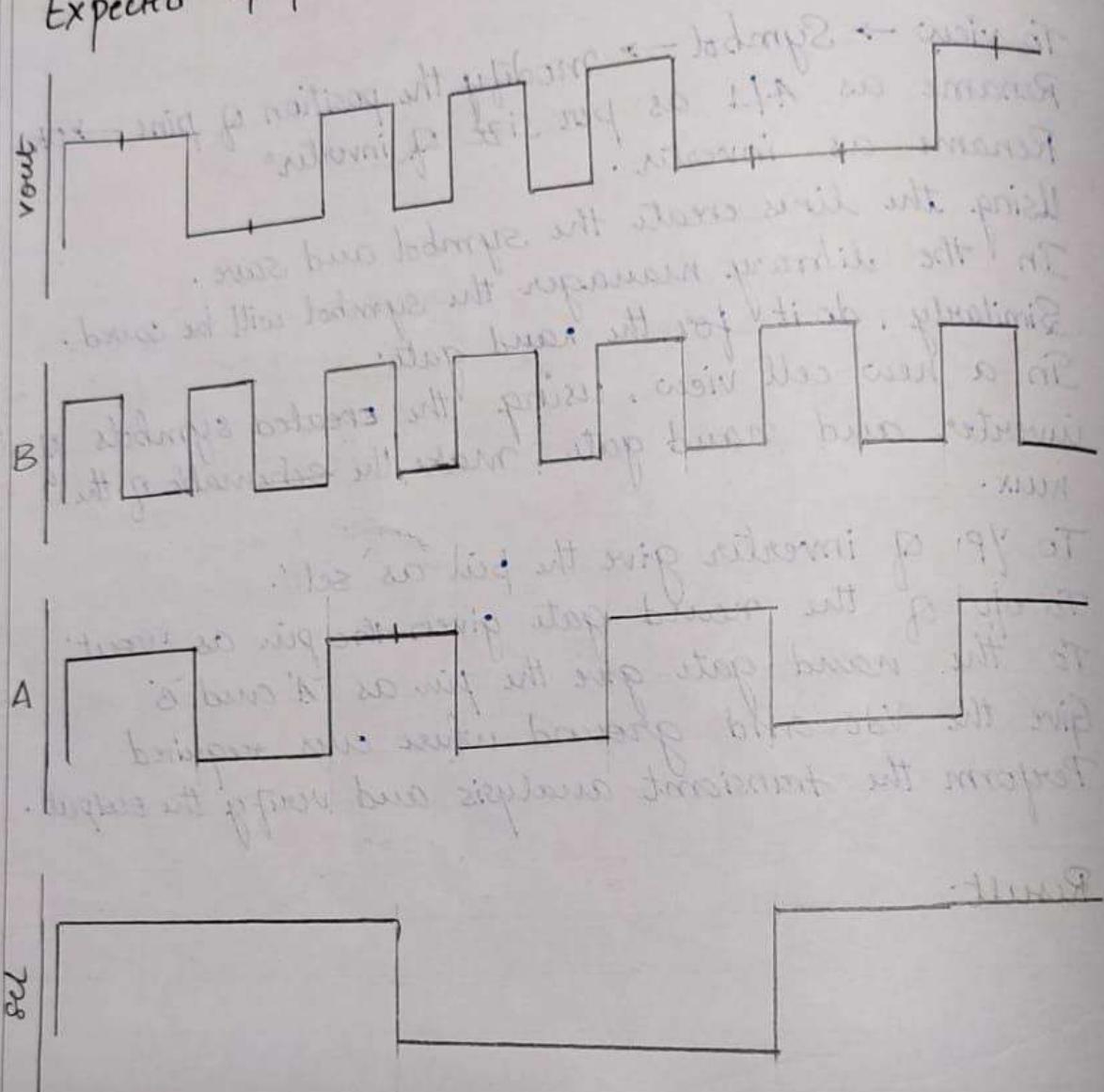
$$\text{Period} = 50\text{ms}$$

$$\text{Rise time} = 10\text{fs}$$

$$\text{fall time} = 10\text{fs}$$

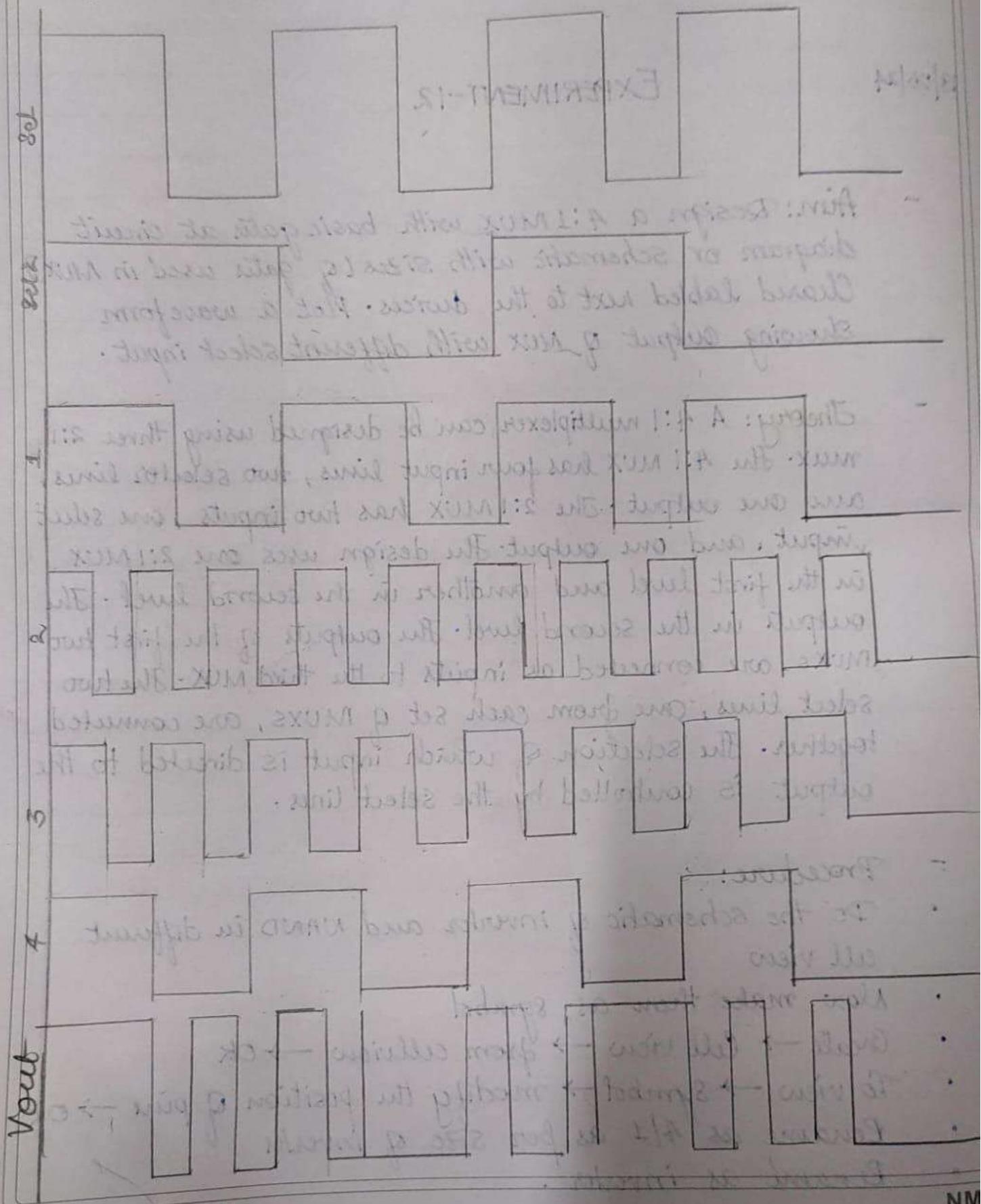
$$\text{Pulse width} = 25\text{msec}$$

Expected Graph



Expected Graph

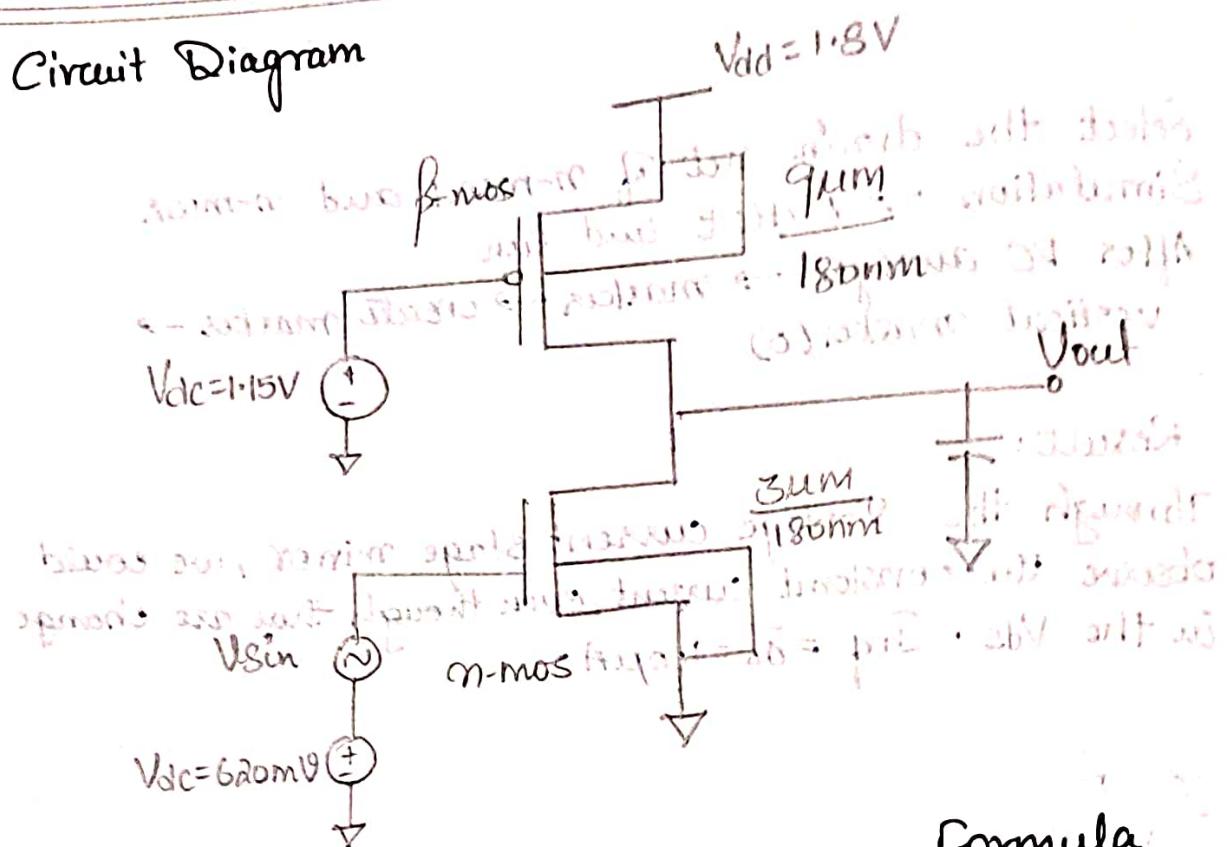
21



NM

shift ↑

Circuit Diagram



Parameters

V_{sin}: Ac mag = 1
 Amp = 10μV
 frequency = 10KHz

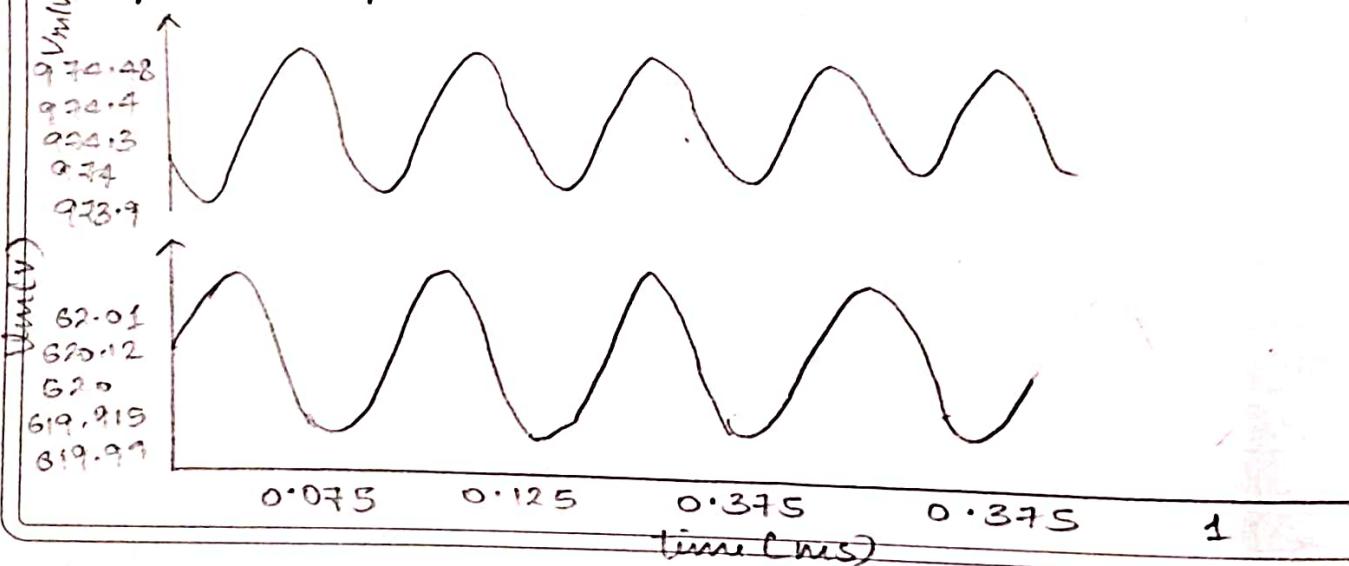
Formula

$$Av = -gmR_o$$

gm → transconductance

R_o → Drain Resistance

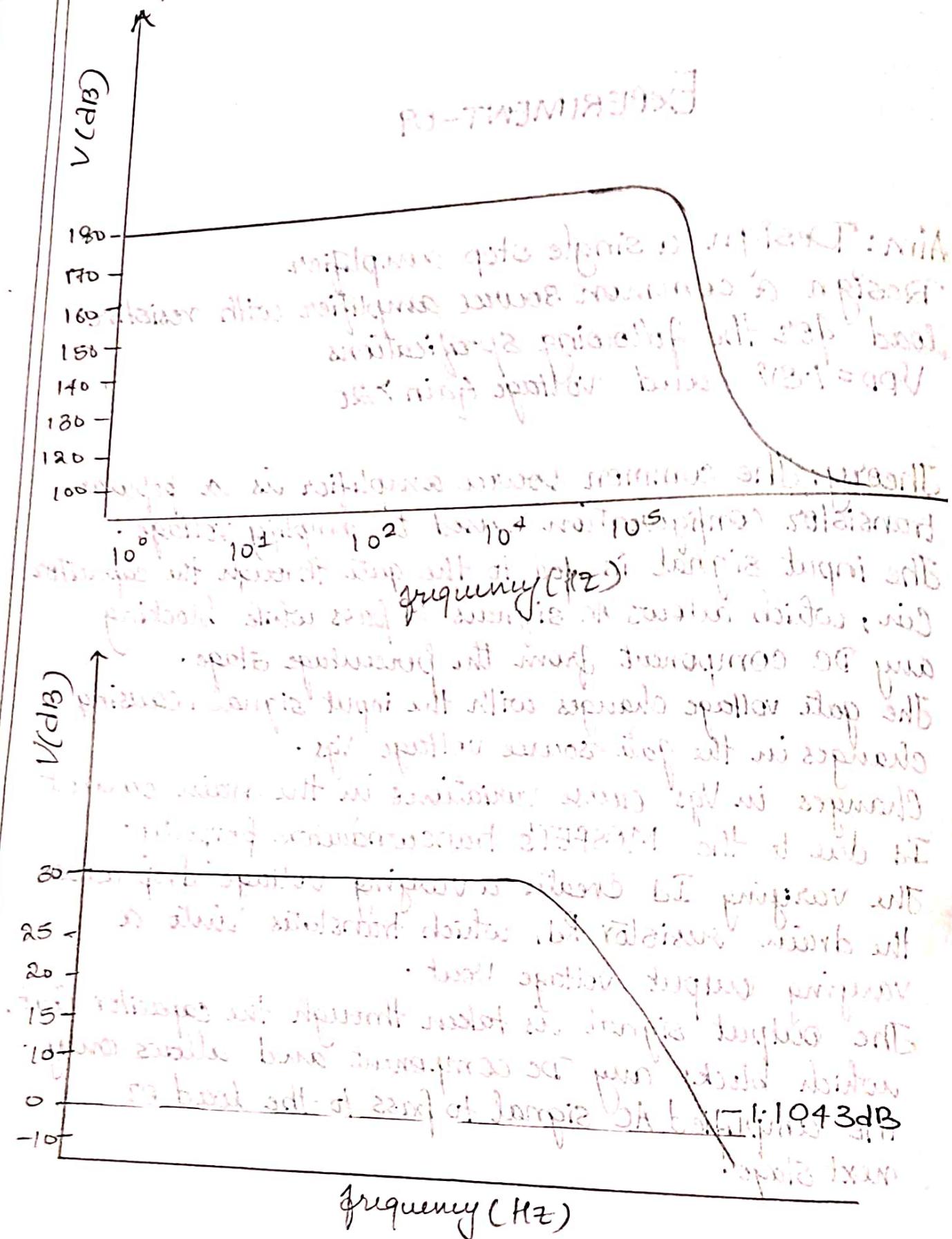
Expected Graph



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EXPERIMENT - 09

- Aim: Design a single step amplifier
Design a common source amplifier with resistive load for the following specifications
 $V_{DD} = 1.8V$ and Voltage Gain > 20
- Theory: The common source amplifier is a popular transistor configuration used to amplify voltage. The input signal is fed to the gate through the capacitor C_{in} , which allows AC signals to pass while blocking any DC component from the percentage stage. The gate voltage changes with the input signal, causing changes in the gate-source voltage V_{gs} . Changes in V_{gs} cause variations in the drain current I_d due to the MOSFET's transconductors property. The varying I_d creates a varying voltage drop across the drain resistor R_d , which translates into a varying output voltage V_{out} . The output signal is taken through the capacitor C_{out} , which blocks any DC component and allows only the amplified AC signal to pass to the load or next stage.

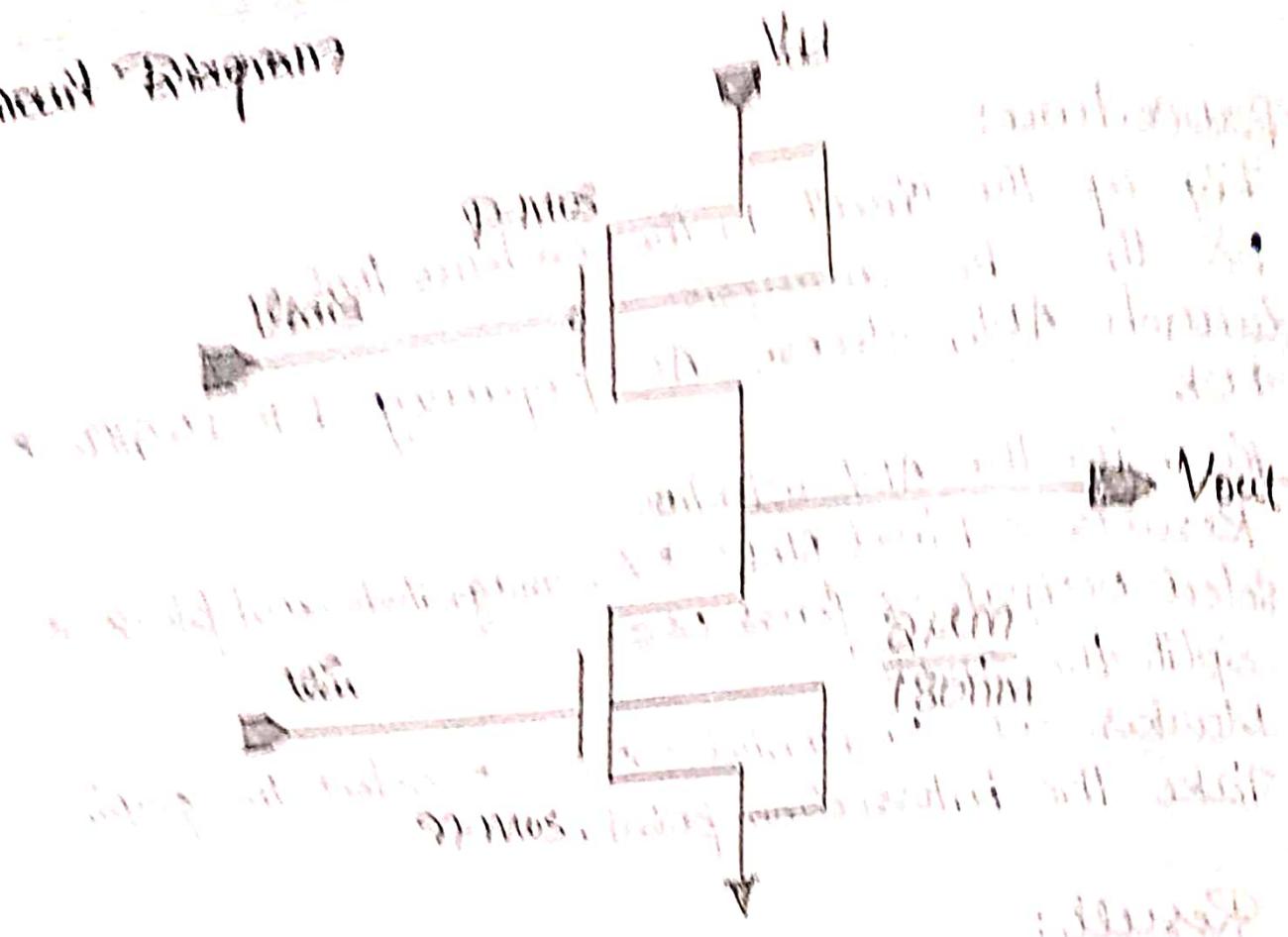


- Procedure:

- Rig up the circuit in the cadence tool
- Do the DC analysis
- Launch ADL, choose AC frequency 1 to 10 GHz →
→ OK
- Run in the ADL window
- Results → Direct plot → AC magnitude and phase →
Select output → press esc.
- Split the graph
- Marker at horizontal → 0 → select the graph
- Take the intersection point.

- Result:

Cloud Diagram



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EXPERIMENT - 10

- Aim:- Design a layout of a single stage amplifier having a common source amplifier with $V_{dd} = 1.8V$.

Theory:

Designing a common source amplifier in 180nm CMOS technology involves translating the schematic into a physical layout that can be fabricated on a silicon wafer. At transistor layout: active area defines the active regions where the transistor will be formed.

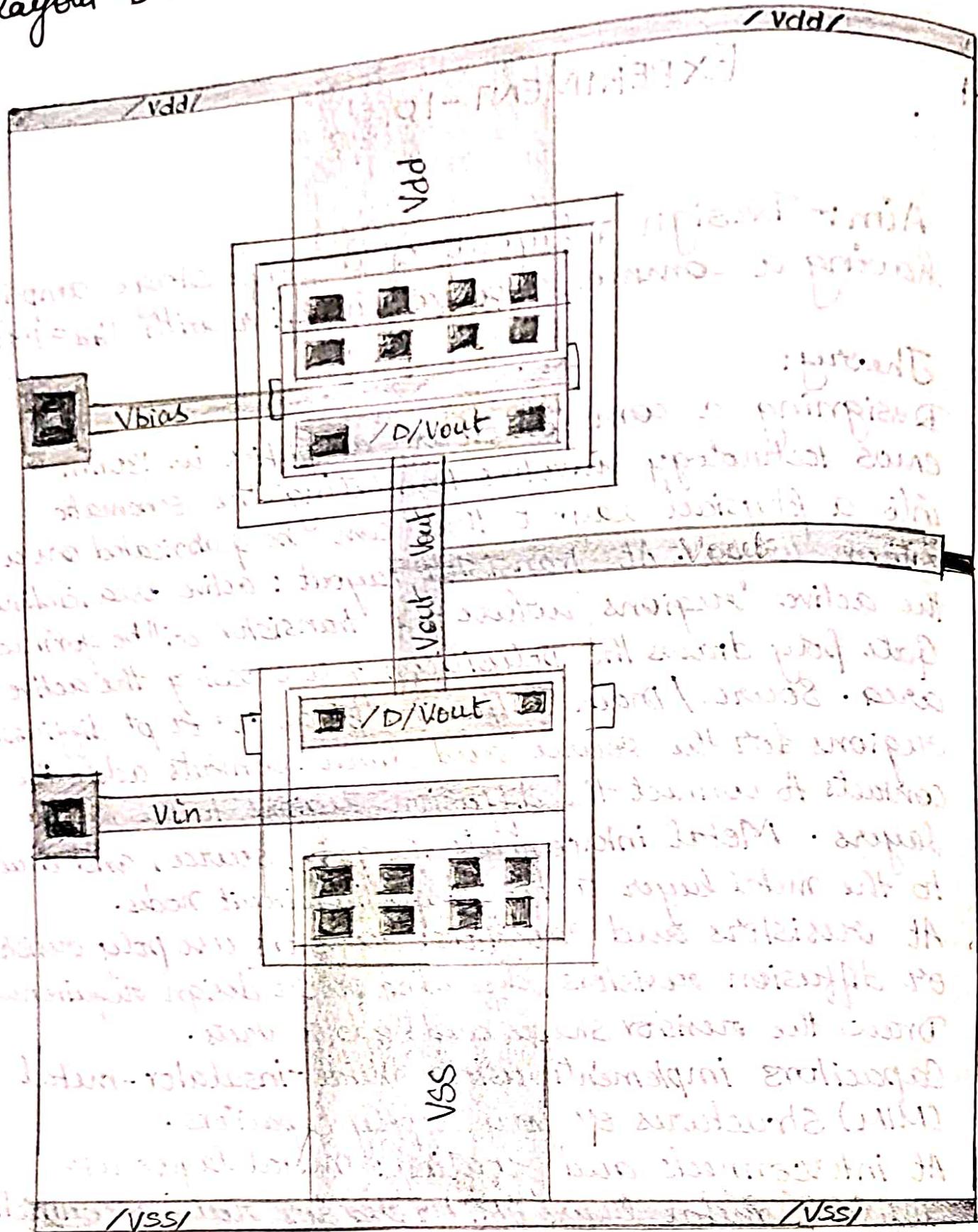
Gate poly draws the polysilicon gate crossing the active area. Source / Drain Diffusion places n^+ or p^+ diffusion regions for the source and drain. Contacts add the contacts to connect the diffusion regions to the metal layers. Metal interconnects the gate, source, and drain to the metal layer to the respective circuit nodes.

At resistors and capacitors: resistors use poly resistors or diffusion resistors, depending on the design requirements. Draw the resistor shapes and add contacts.

Capacitors implement using metal-insulator-metal (MIM) structures or poly to poly capacitors.

At interconnects and routing: metal layers use different metal layers (M_1, M_2 etc) for routing connections. Ensure proper use of vias to connect different metal layers. Power and ground routing designs a wide

Layout Schematic

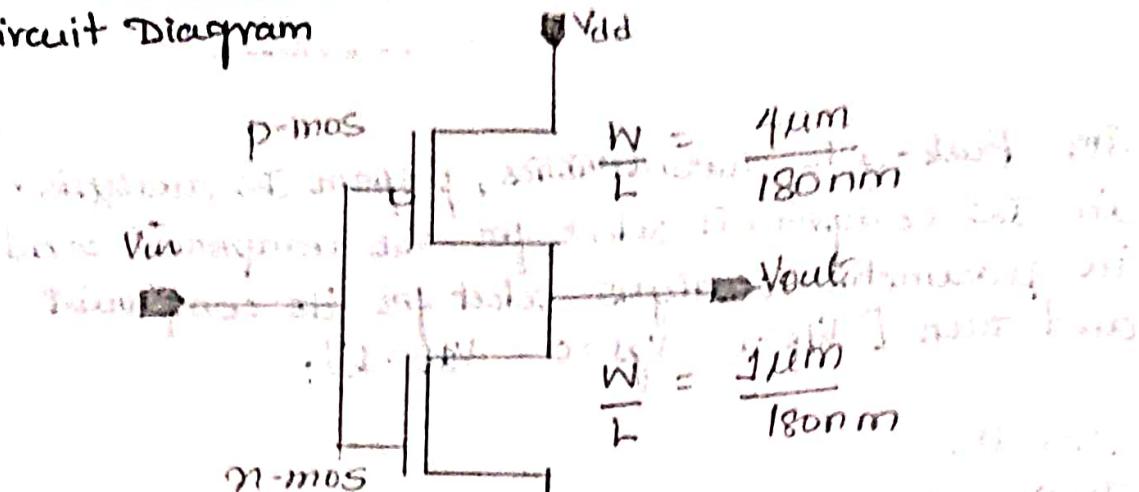


metal lines of power (V_{dd}) and ground (Gnd) to ensure low resistance and robust power distribution.

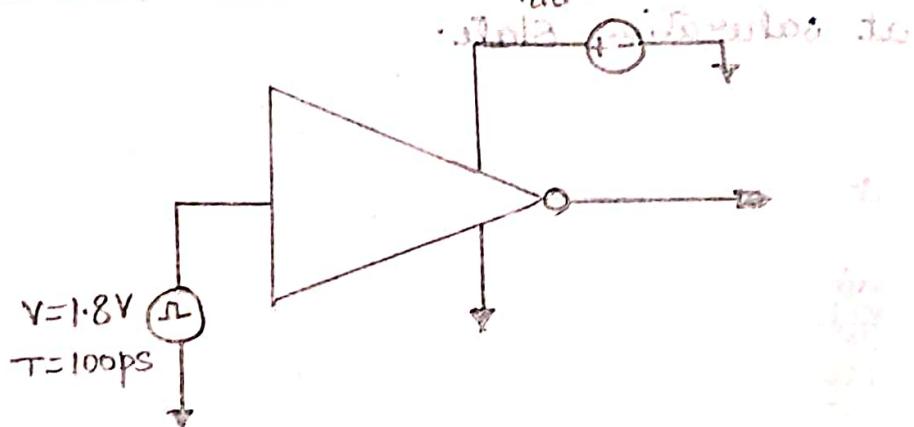
- Procedure:

- Rig up the circuit in the cadence tool accordingly
- Launch \rightarrow Layout $X1 \rightarrow$ Create New \rightarrow OK.
- Connectivity \rightarrow Generate \rightarrow all from Source (in boundary)
- Place \rightarrow Pin placement \rightarrow Schematic \rightarrow V_{dd} and $V_{ss} \rightarrow$ Pin rail
- Shift F to see internal layers.
- P-mos close to V_{dd} and n-mos close to V_{ss} .
- Rotate the transistor to make the connection
 Click on the transistor \rightarrow Right Click \rightarrow Rotate to right (Pmos)
 Click on the transistor \rightarrow Right Click \rightarrow Rotate to left (Nmos)
- In P-mos V_{dd} select 'P' and connect to V_{dd} .
- Similarly, from n-mos connect to the V_{ss} .
- From p-mos vout to n-mos vout a metal connection should be done.
- Right click on p-mos \rightarrow Property \rightarrow parameter \rightarrow body type integrated.
- Similarly, for n-mos (q)
- Create \rightarrow Via \rightarrow Metal to Poly
- Assura \rightarrow Technology \rightarrow Run DRC
- Assura \rightarrow Technology \rightarrow Run LVS.
- Result: There are no errors in DRC schematic and layout has matched.

Circuit Diagram



rechteckige Schaltung mit einem Inverter auf Basis eines OT im
zweiten Quadranten mit einer OT als aktiver Teil des
Schwingers mit der OT auf Leistungselementen OT und
nachfolgendem OT auf Basis eines aktiver Elementes OT des
Schwingers OT und einem aktiver Element OT des
Schwingers OT.

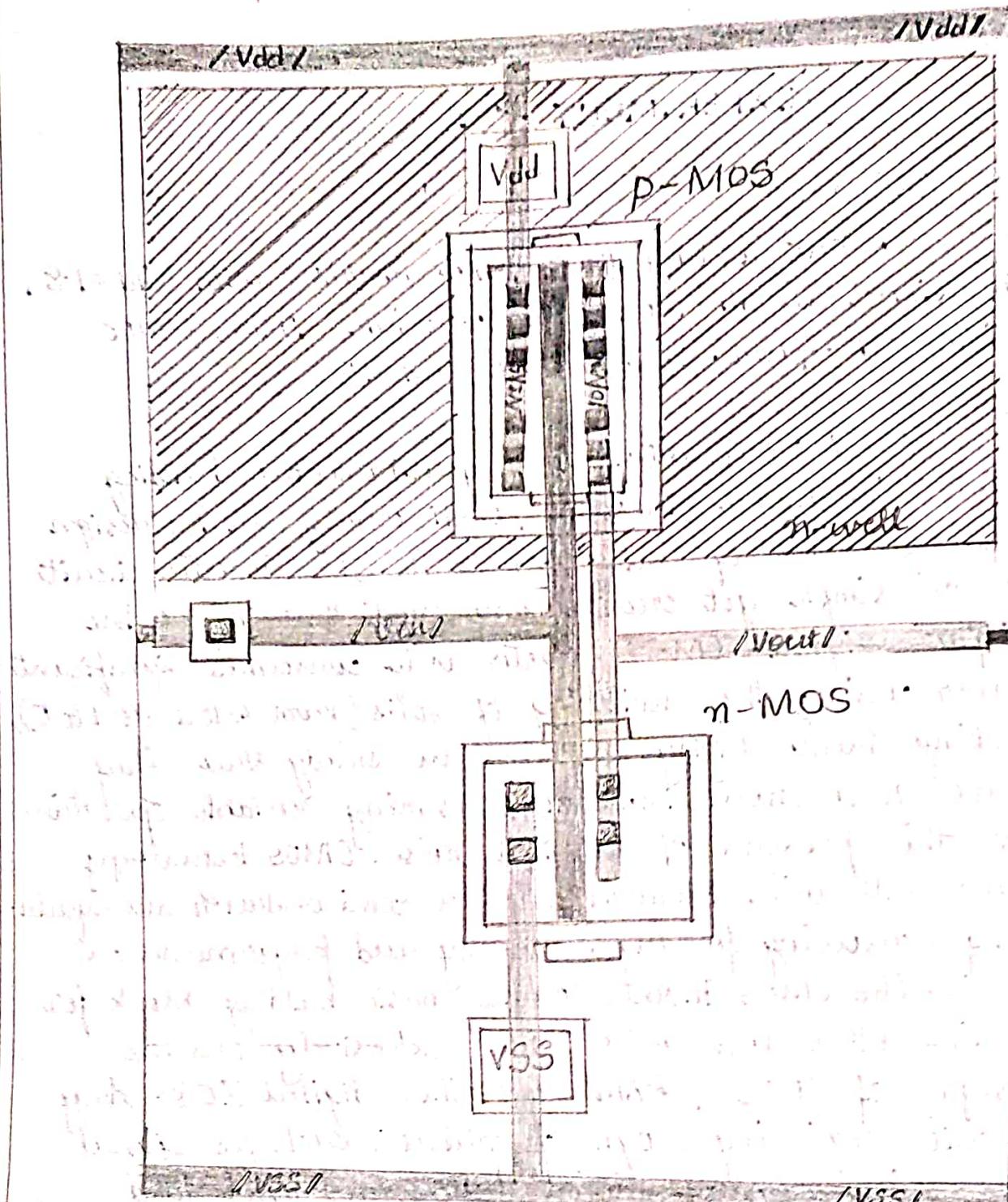


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EXPERIMENT - 06

- Aim:- Draw a layout of pmos inverter with $V_{dd} = 1.8$, transistor length = 180nm, nmos width = 1μm, pmos width $W_p = 4\mu m$. Verify DRC and LVS.
- Theory: CMOS inverter is a fundamental building block in digital electronics, particularly in the design and operation of integrated circuit. The inverter circuit is a simple yet crucial component that inverts the input signal. CMOS inverter only consumes significant power during the switching of states (from 0 to 1 or 1 to 0), making them highly efficient in steady state. They have good noise immunity, ensuring reliable operation in the presence of electrical noise. CMOS technology scales well with advancements in semiconductor manufacturing, allowing for higher density and performance in IC's. The CMOS inverter is the basic building block for creating other logic gates, used extensively in the design of CPU's, RAM and other digital IC's. Any circuit requiring logic operations, such as signal processing, communication devices and embedded systems.

Layout Schematic



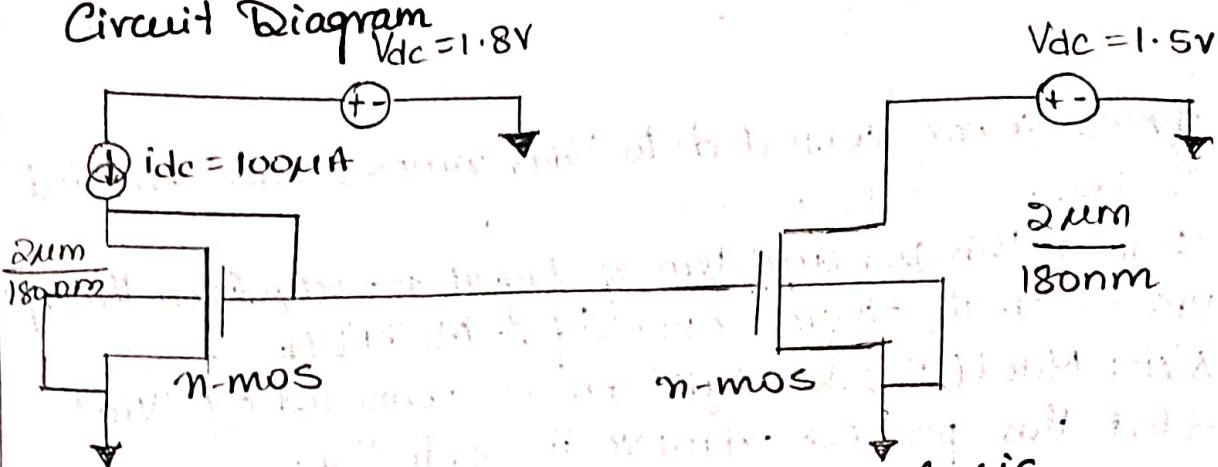
- Procedure:

- Create normal inverter in 180nm technology
- $W_p = 4\mu m$, $W_n = 1\mu m$ and add pins.
- Create - Cell view from cell view → OK
Left pins: V_{in} , Right = V_{out} , Top = V_{dd} , Bottom = V_{ss}
- Remove rectangle and move the label (V_{ss} , V_{in} etc.) accordingly by dragging it.
- Edit → Shape → line (draw □) and edit → shape → → circle (▷)
- Drag and wire & drop in corresponding places.
- Check and save the circuit.
- Open new cell view (exp-test) from same library
- Create → Instance → Browse → Select library created (inv_layout) → exp1 (cellView) symbol created → close (lide)
- Find V_{pulse} , V_{dc} , gnd from analoglib
- Create "Vout" pin and connect to the Vout line
- Reform Transistor analysis
- Open first schematic (fig.1)
- Launch → layoutXL → Create New → OK
- In layout window that appears, select connectivity → → Generate → DLL from source → OK (on new window) (Shift+F)
- Press S' to stretch the layout drawing area
- Select PMOS & NMOS & drag inside drawing area
- Right click on 4 boxes to check which pin it is each
- 'Shift + F' ⇒ to see source, drain etc inside pmos and nmos.
- Create → wiring → wire → and connect polysilicon of both n and p-mos (gate is short) and similarly for drain

- PMOS source connected to Vdd, nmos source connected to Vss.
- Connect Vin pin and Vin of layout ic-polysilicon through via \Rightarrow create \rightarrow via \rightarrow via def.: - M₁ POLY₁
- Note: Metal (Vin) & polysilicon are connected by "Via"
- Select Vin pin box & move it inside Via.
create \rightarrow wiring \rightarrow wire \rightarrow select outer part of via & connect to polysilicon of layout.
- Connect Sop pin and drain short area [both are metal to V_d via required]
- Create \rightarrow via \rightarrow via definition \rightarrow M₁ PSUB (for nmos)
Create \rightarrow via \rightarrow via definition \rightarrow M₁ NWEELL (for nwell)
- Select nwell from left side table/list \rightarrow create \rightarrow shape \rightarrow rectangle \rightarrow draw rectangle around pmos.
- Make sure no overlapping occurs.
- Check and save.
- For DRC:- Assura \rightarrow install \rightarrow foundary \rightarrow analog \rightarrow 180 \rightarrow Run DRC \rightarrow OK
- For LVS:- Assura \rightarrow install \rightarrow foundary \rightarrow analog \rightarrow 180 \rightarrow Run LVS \rightarrow OK

- Result:
There are no errors in DRC schematic and layout has matched.

Circuit Diagram

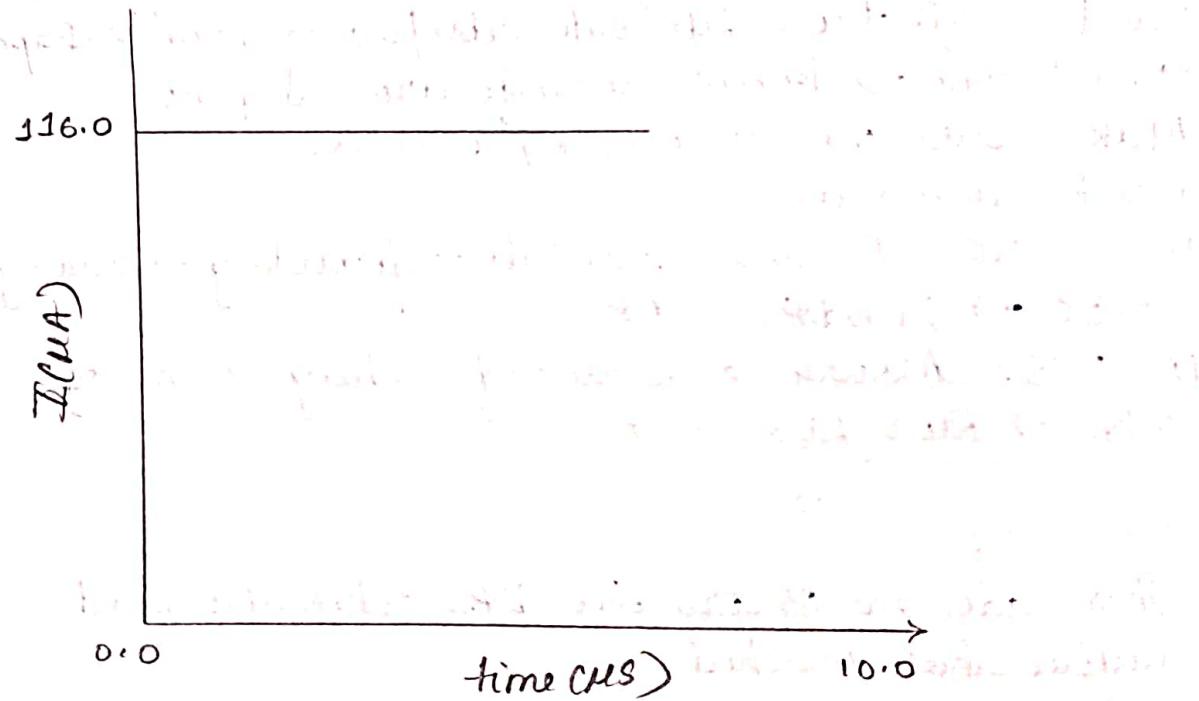


Transient Analysis.

Stop time = 10μs Start = 0 Stop = 1.8
moderate

DC analysis

Expected Graph



Experiment No.

Date :

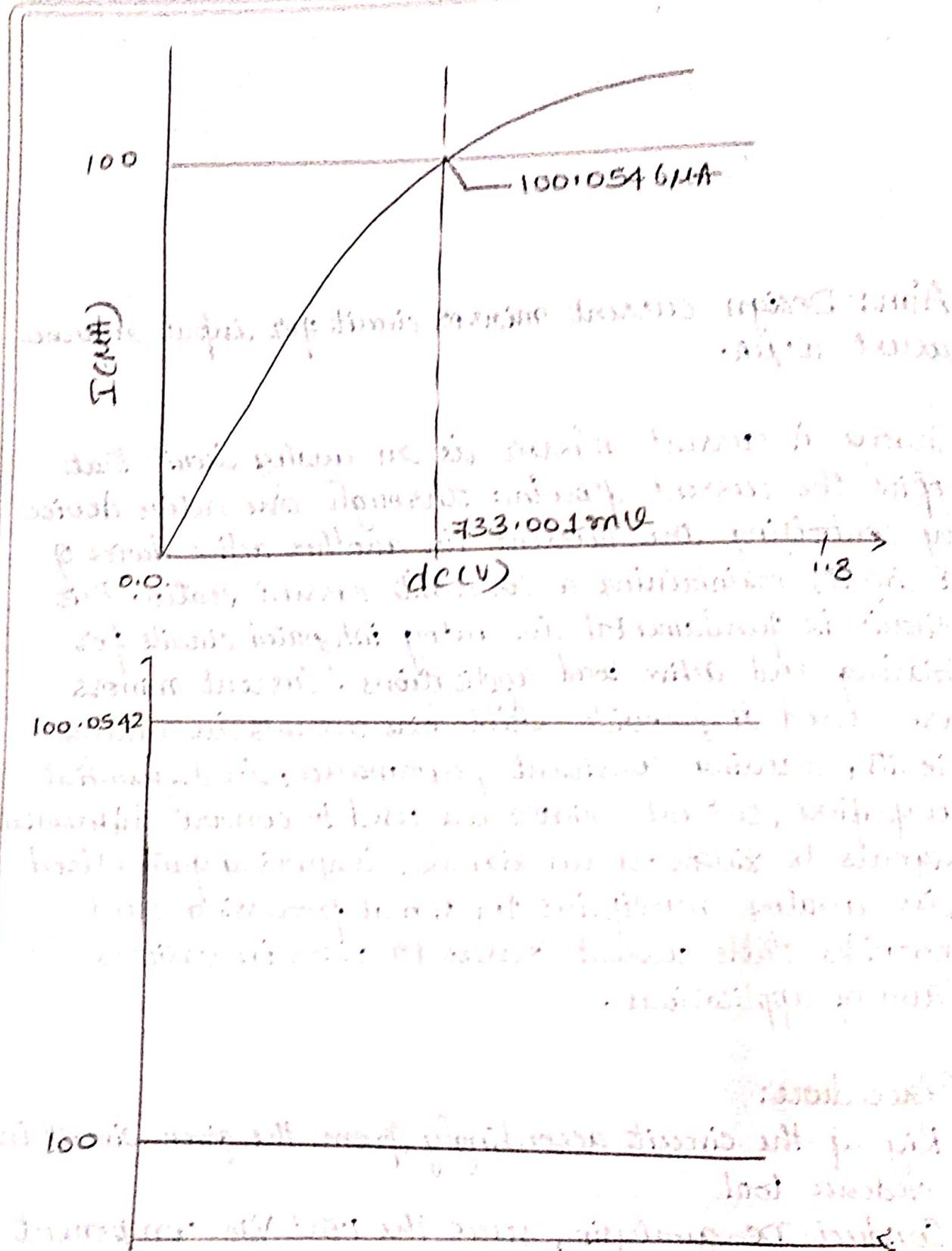
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EXPERIMENT - 07

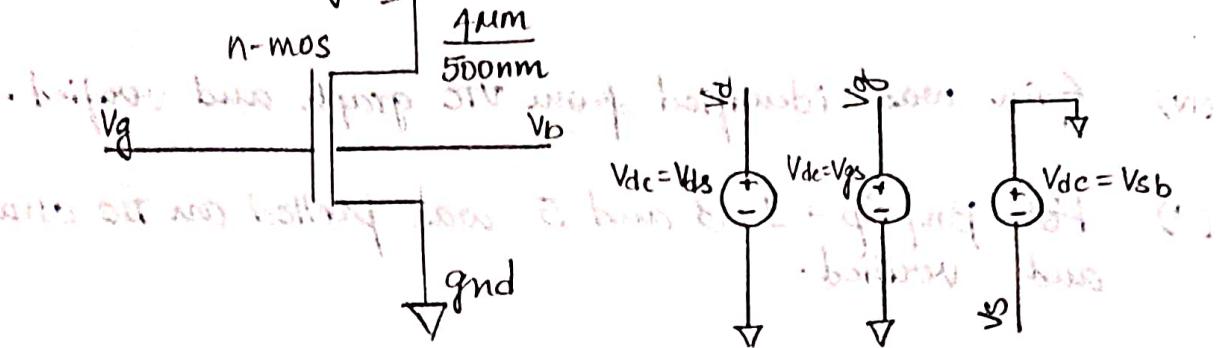
- Aim: Design current mirror circuit for input reference current $100\mu A$.
- Theory: A current mirror is an analog circuit that copies the current flowing through one active device by controlling the current in another active device of a circuit, maintaining a constant current ratio. This circuit is fundamental in analog integrated circuits for biasing and active load applications. Current mirrors are used to provide stable bias currents in analog circuits, ensuring consistent performance. In differential amplifiers, current mirrors are used to convert differential signals to single-ended signals, improving gain. Used in analog multipliers for signal processing and provides stable current sources or sinks in various analog applications.
- Procedure:
 - Rig up the circuit accordingly from the given circuit in cadence tool
 - Conduct DC analysis, select the $1.5V$ Vdc component
 - Conduct transient analysis, Output \rightarrow to be plotted
 \rightarrow select the drain net of n-mos1 and n-mos2
 - Simulation \rightarrow Netlist and Run



Wavelength, time (μs) mixed 10,000
Because the length of the pulse is longer

- After DC analysis \rightarrow marker \rightarrow create marker \rightarrow
 \rightarrow vertical marker (0)
 - Now at V_{dc} change the voltage which was obtained
in DC analysis.
 - Conduct transient analysis for this changed voltage.
- Result:
- Input Current = 100.0546 mA
 - Output Current = 100.0542629 mA

(1) Circuit Diagram



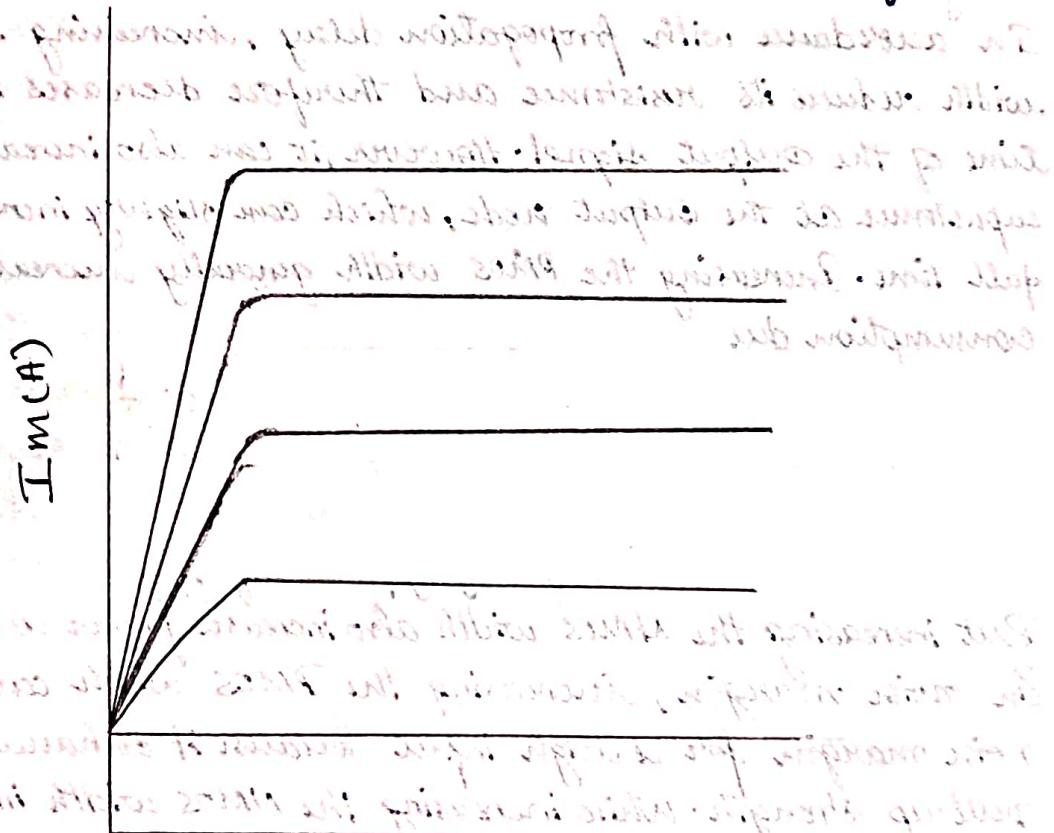
beispielhaft seien verschiedene neue Modelle von Parameters (vgl. Abbildungen)

Expected Graph

$$V_d, V_{dc} = V_{ds}$$

$$V_s, V_{dc} = V_{sb}$$

$$Vg + Vdc = Vgs$$



n-mos parameters

model name: myNmos

width: 4 μm and all processes follow this pattern.

Length : 500nm

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EXPERIMENT-05

- Aim:- Create a spectre model for the transistor by setting parameter values in the template shown in table and simulate the following DC characteristics curves with $V_{dd} = 1.8V$:

- Output characteristics: I_d vs V_{ds} for $V_{gs} = \text{linspace}(0V, V_{dd}, 6)$, $V_{sb} = 0V$, and $V_{ds} = \text{linspace}(0V, V_{dd}, 100)$
- Transfer Characteristics: I_d vs V_{gs} for $V_{ds} = \text{linspace}(0V, V_{dd}, 6)$ $V_{sb} = 0V$, and $V_{gs} = \text{linspace}(0V, V_{dd}, 100)$
- Back-gate Characteristics: I_d vs V_{sb} for $V_{ds} = \text{linspace}(0V, V_{dd}, 6)$ $V_{gs} = 0V$, and $V_{sb} = \text{linspace}(0V, V_{dd}, 100)$

- Theory: In output characteristics, the output voltage (V_{ds}) of the NMOS Transistor. It is typically plotted with the drain-to-source voltage (V_{ds}) on the x-axis and the drain current (I_d) on the y-axis. The output characteristics curve shows how the drain current changes with varying drain-to-source voltage, keeping the gate-to-source voltage (V_{gs}) constant. During transfer characteristics, the gate-to-source voltage (V_{gs}) and the drain current (I_d) of the NMOS transistor. It is plotted with V_{gs} on the x-axis and I_d on the y-axis. The transfer characteristics curve illustrates how the drain current varies with different gate-to-source voltages, typically with a fixed drain-to-source voltage (V_{ds}). In back-gate characteristics, characteristics are related to the back-gate or substrate of the NMOS

(ii) Circuit Diagram



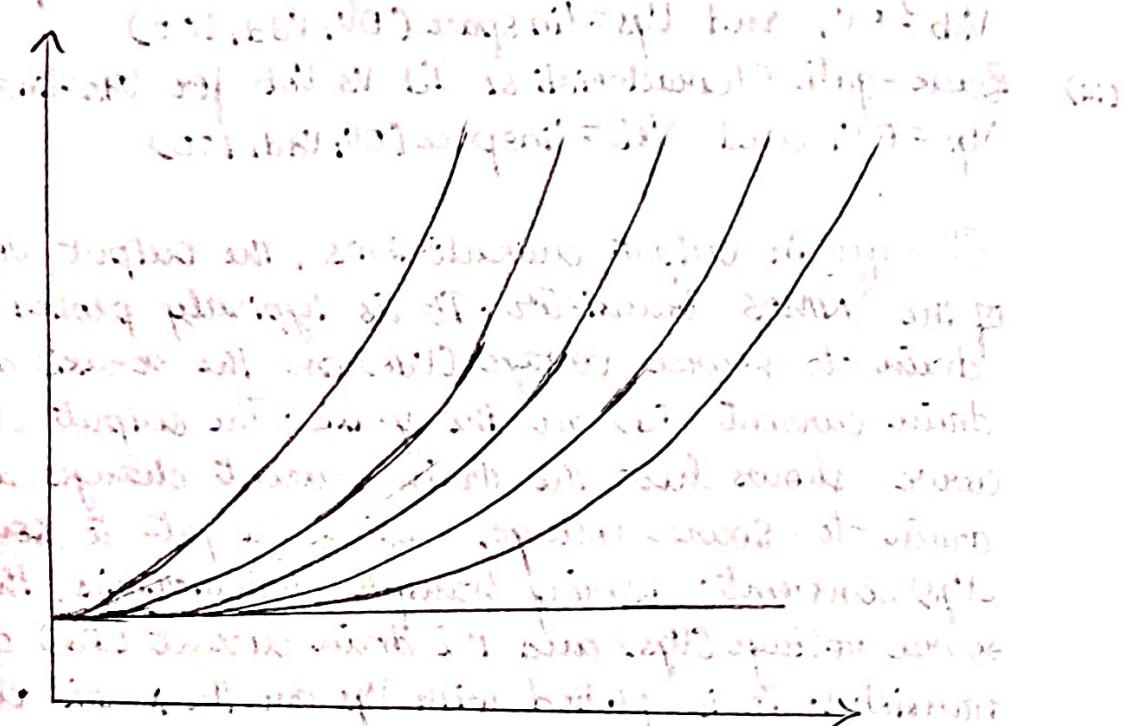
Given it will only depend on V_{gs} and V_{ds} . As V_{ds} is constant, we can ignore it. The current I_D is given by the equation:

$$I_D = \frac{K}{2} \cdot A \cdot (V_{gs} - V_T)^2$$

For $V_T = 0.5\text{V}$, $K = 100\text{mA/V}^2$, and $A = 1000\text{mm}^2$, the graph of I_D vs V_{gs} is as follows:

Expected Graph

Start = 0 Stop = 1.8



The graph shows that the drain current I_D increases with V_{gs} and remains constant after reaching a certain value. This is because the drain current is limited by the drain-to-source voltage V_{ds} . The saturation current is given by the equation:

$$I_D = \frac{K}{2} \cdot A \cdot (V_{gs} - V_T)^2$$

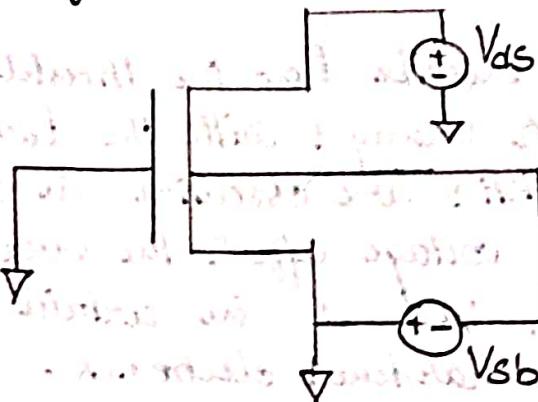
For $V_T = 0.5\text{V}$, $K = 100\text{mA/V}^2$, and $A = 1000\text{mm}^2$, the saturation current is approximately 400 mA.

transistor. They describe how the threshold voltage (V_{TH}) of the transistor changes with the back-gate voltage. Back-gate characteristics are essential in applications where the substrate's voltage affects the overall behavior of the transistor, such as in certain power devices or in radiation-hardened electronics.

- Procedure:
- Invoke the cadence tool from the terminal.
- Select analoglib in the library.
- Create the cell view
- Create an instance for n-mos in analog library and select "nmos4".
- Give wiring. Click on wire name - "Vd", "Vg", "Vb"
- Create instance for Vds and connect accordingly.
- Create wire name for Vdc - "Vd", "Vb" and "Vg".
- In ADEL window, select the unknown parameters by clicking "Copy from Cell View".
- Give the values of $V_{DS} = 1$, $V_{GS} = 1$, $V_{SB} = 0$
- In setup icon \rightarrow modal libraries \rightarrow add modal file \rightarrow add "lab1.scs" \rightarrow Apply.
- Perform DC analysis, for outputs select V_t node i.e. M₁
- In parametric analysis varying from 0 to 1.8 having 6 steps.
- For transfer characteristics, perform DC analysis.
- In DC components select for V_{gs} component and in parametric analysis select for V_{ds} component and run.

(iii) Circuit Diagram

(iii) Später hinzugefügt, um die Verstärkung
der negativen Spannung zu verstehen.
Hierbei wird die positive Spannung auf
die negative Spannung aufgetragen und
durch einen Pfeil gekennzeichnet.
Die negative Spannung ist hierbei
negativ, was bedeutet, dass sie
die positive Spannung aufhebt.



Expected Graph

Die Graphen mit den entsprechenden Werten sind oben
angegeben. Die graphische Darstellung zeigt
einen linear abfallenden Graphen, der die
negative Spannung auf die positive Spannung aufhebt.
Der Graph beginnt bei einer negativen Spannung von $-V_{ds}$ und endet bei einer positiven Spannung von V_{dd} .
Die Steigung des Graphen ist gleich der negativen Steigung
der negativen Spannung. Der Graph verläuft durch den Ursprung.
Die Steigung ist definiert als $\frac{\Delta V_{ds}}{\Delta V_{sb}}$.

Die Steigung ist eine negative Zahl, da die negative Spannung
auf die positive Spannung aufhebt. Die Steigung ist
gleich dem negativen Wert der negativen Spannung.

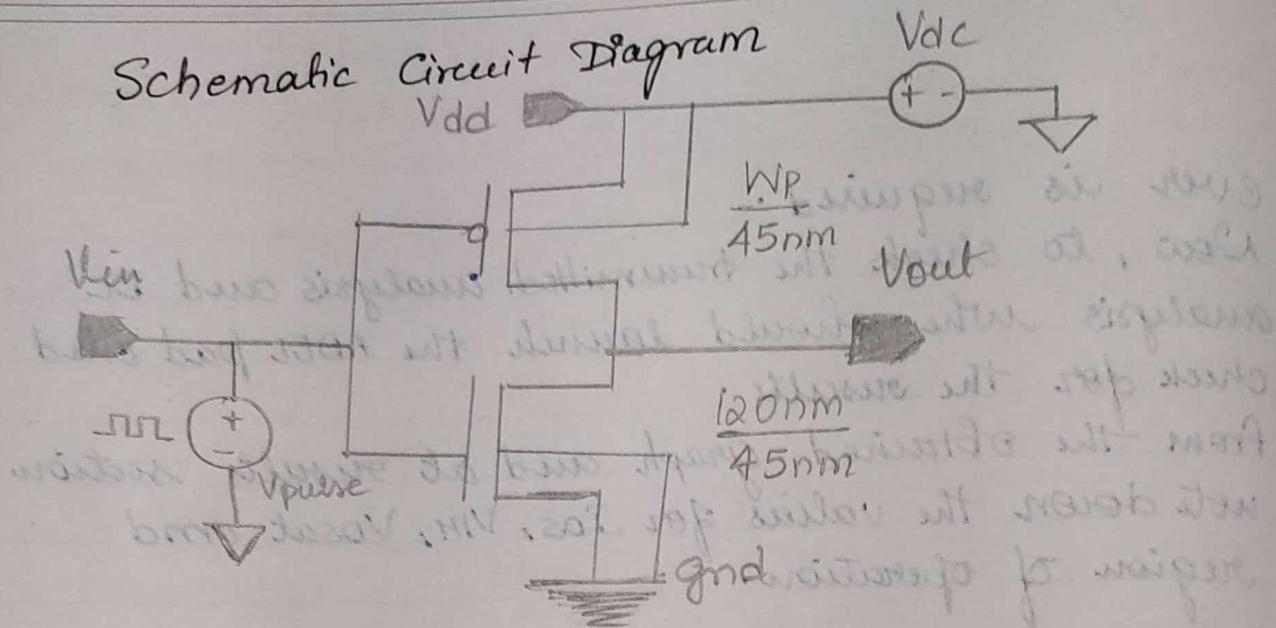
dcv

- For Bulk-gate characteristics, perform DC analysis.
- In DC component select for V_{sb} component and in parametric analysis select for V_{ds} component and run [$V_{ds} = 1$ $V_{gs} = 0$ $V_{sb} = 1$].

- Result:

- i) Design for specific model of the n-mos-transistor by setting parameter in cadence, DC characteristics was obtained for I_d vs V_s this graph.
- ii) DC characteristics was obtained for I_d and V_{ds} where, when the drain voltage increases, then the electric field also increases.
- iii) DC characteristics was obtained for I_d vs V_{sb} where, initial the current is increased and then reaches at saturation state.

Schematic Circuit Diagram



Parameters

V_{pulse}

Rise time = 10fs

V_{tg1} = 0V

Fall time = 10fs

V_{tg2} = 1V

Pulse width = 50p

Period = 100ps

delay = 10ps

V_{dc} DC voltage = 1V

trans Analysis

Stop time - 2dop, moderate

DC Analysis

Start = 0

Stop = 1V

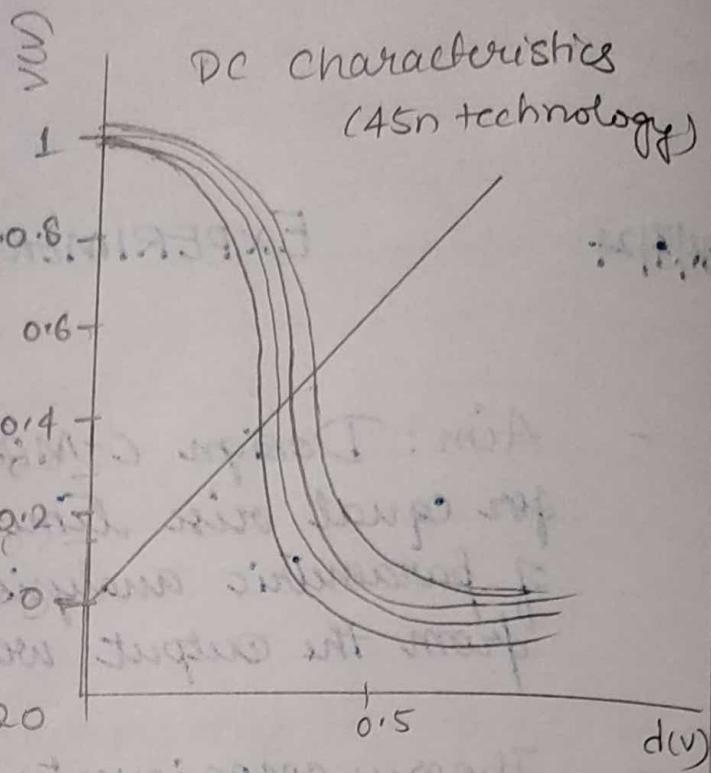
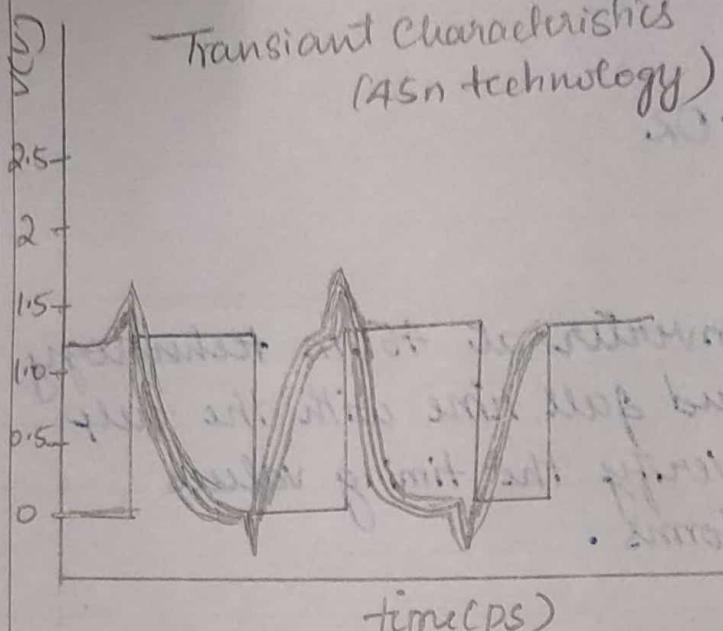
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EXPERIMENT - 02

- Aim: Design C-MOS inverter at 45nm technology for equal rise time and fall time with the help of parametric analysis. Verify the timing values from the output waveforms.
- Theory: CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET [Field Effect Transistor], composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data in small circuits.
- Procedure:
 - Invoke the cadence tool from the terminal.
 - Create an instance for n-mos and p-mos by giving total width = w for p-mos.
 - Give the wiring for the p-mos and n-mos.
 - Give the input, output, VDD and GND pins.
 - Create instances for Vpulse and Vdc and connect accordingly.

Expected Graph

Transient characteristics
(45n technology)

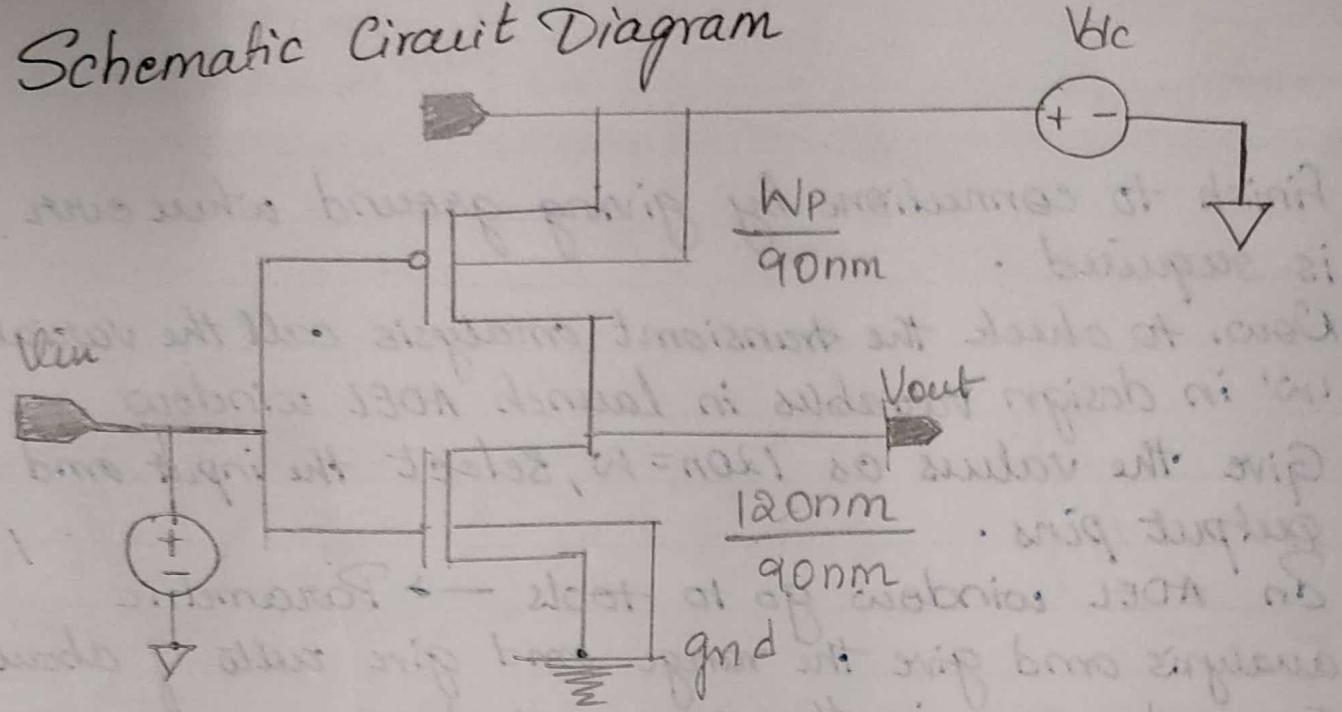


Initial state is in waiting period around 200ns. If present in waiting period then it will be in Tabular Column

W(nm)	t _{on} (ps)	t _{off} (ps)	d(v)
120n	4.46P	3.685P	500mV
180n	4.46P	4.380P	505mV
240n	4.105P	5.131P	510mV
300n	3.877P	5.845P	515mV
360n	3.700P	6.556P	520mV

- finish to connections by giving ground where ever is required.
 - Now, to check the transient analysis call the variable 'w' in design variables in launch ADEL window
 - Give the values as $120n = w$, select the input and output pins.
 - In ADEL window go to tools \rightarrow Parametric analysis and give the range and give value of about 5 and run in the same window.
 - Save obtained graph
 - Now calculate the rise time for each graph in calculator and note down the values.
 - Note down values of V_m from DC graph.
- Result: Design for C-MOS inverter of 45n technology was executed in cadence and graph of transient and dc analysis was obtained and rise and fall time for the different widths has been obtained. We can observe that 180n has equal rise and fall time.

Schematic Circuit Diagram



Parameters

V_{pulse}

delay = 10ps

DC = 1V

Rise time = 10fs

V_{tg 1} = 0V

Fall time = 10fs

V_{tg 2} = 1V

Pulse width = 50p

Period = 100ps

DC voltage = 1V

tran Analysis

Stop time - 220p, moderate

DC Analysis

Start = 0

Stop = 1V

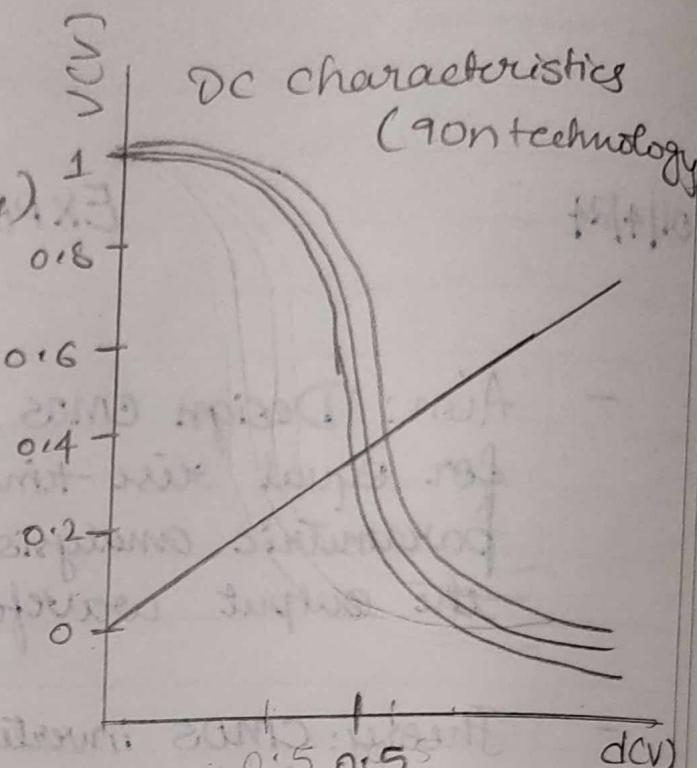
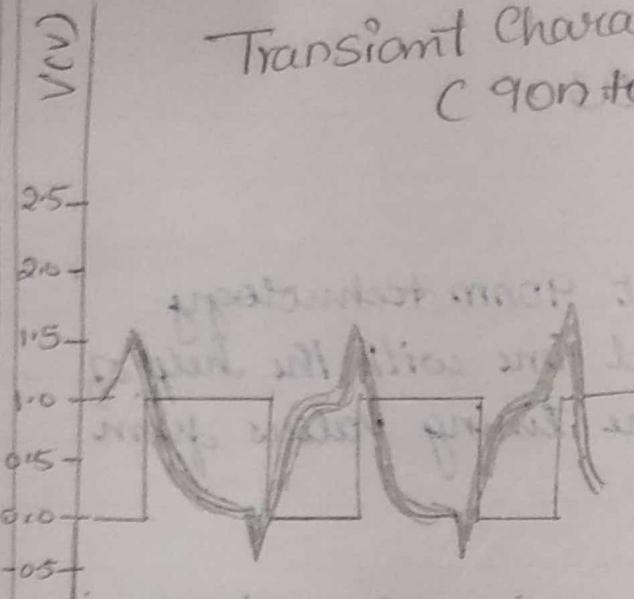
01/4/24

EXPERIMENT - 03

- Aim: Design CMOS inverter at 90nm technology for equal rise time and fall time with the help of parametric analysis. Verify the timing values from the output waveform.
- Theory: CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET [Field Effect Transistor]. Composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data in small circuits.
- Procedure:
 - Invoke the cadence tool from the terminal
 - Create an instance for n-mos and p-mos by giving of total width = w for p-mos
 - Give wiring for the p-mos and n-mos
 - Give the input, output, VDD and gnd pins.
 - Create instances for Vpulse and Vdc and connect accordingly.

Expected Graph

Transient Characteristics
(90nm technology)



Tabular Column

W	V _m	t _r	t _f
120n	410.53mV	11.6P	4.936P
195n	445.53mV	8.412P	5.565P
270n	469.318mV	6.887P	6.042P
345n	487.20mV	6.326P	6.845P
420n	500.86mV	5.933P	7.648P

- finish the connections by giving ground where ever is required .
 - Now, to Check the transient analysis call the variable 'W' in design variables in launch ADEL window .
 - Give the value as $120n = W$ and select the input and output pins .
 - In ADEL window go to tools \rightarrow parametric analysis and give the range and give linear step of about 10 and run in the same window .
 - Save obtained graph
 - Now calculate the risetime for each graph in calculator and note down the values .
 - Note down values of V_m from DC graph .
- Result : Design for CMOS inverter of 90n technology was executed in cadence and graph of transient and DC analysis was obtained , rise and fall time for the different widths has been obtained . We can observe that at 345n has equal rise and fall time .

Parameters

V_{pulse}

$$DC = 1.8V$$

$$\text{delay} = 1.0 \text{ PS}$$

$$V_{tg1} = 0V$$

$$\text{Risetime} = 1.0 \text{ PS}$$

$$V_{tg2} = 1.8V$$

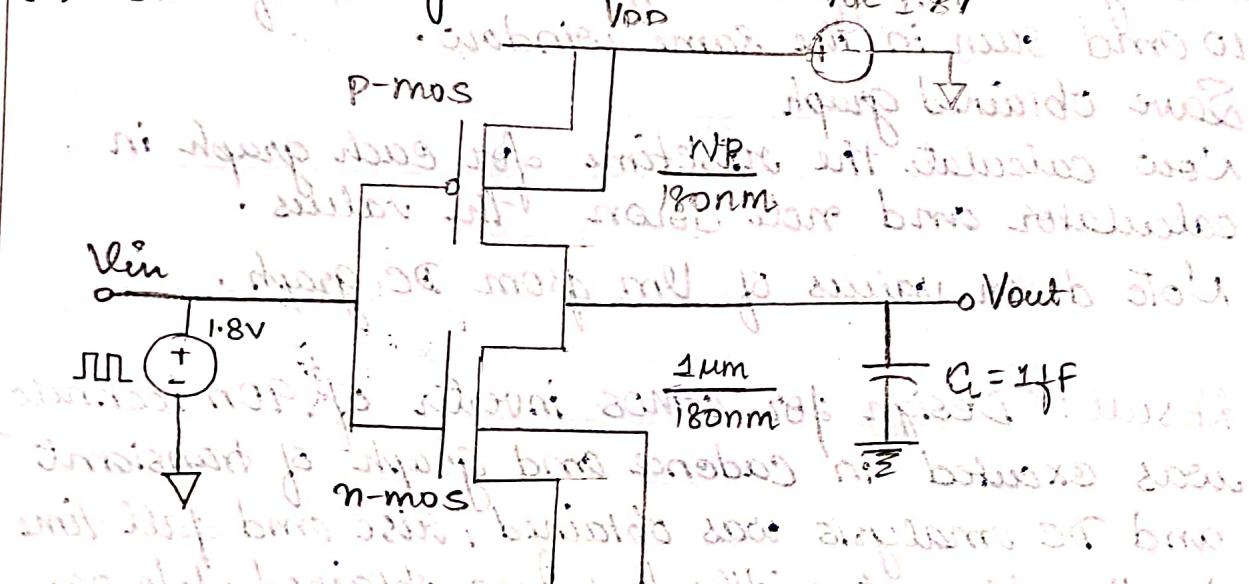
$$\text{fall time} = 1.0 \text{ PS}$$

$$\text{Period} = 1.00 \text{ PS}$$

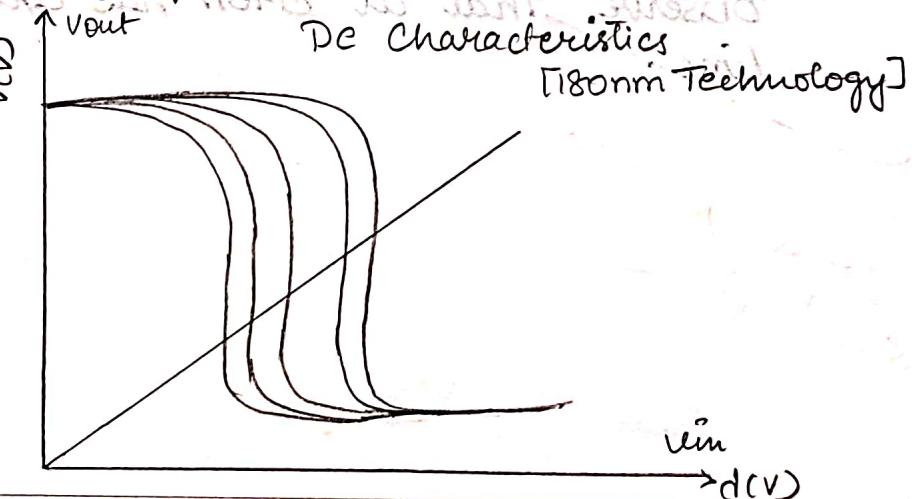
$$\text{Pulse width} = 50\%$$

$$V_{dc} : DC V_{tg} = 1.8V$$

(1) Circuit Diagram



Expected Graph



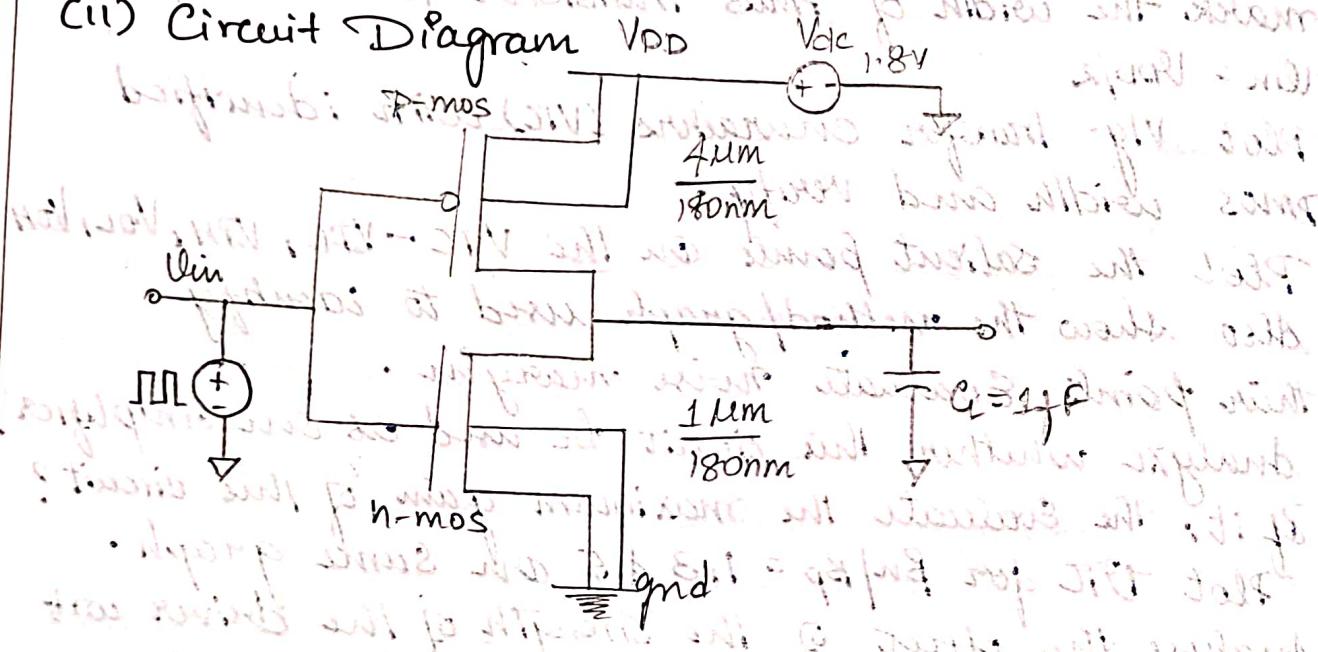
EXPERIMENT - 04

- Aim :- Design a CMOS inverter with $V_{DD} = 1.8V$, transistor length $L_n = L_p = 180\text{nm}$, n-mos width (W_n) = 1 μm , load Capacitance $C_L = 1\text{fF}$
 - (i) Plot transition V_{TG} vs width of PMOS transistor mark the width of PMOS transistor for which $I_m = V_{DD}/2$.
 - (ii) Plot V_{TG} transfer characters (VTC) with identified PMOS width and verify.
 - (iii) Plot the salient points on the VTC - V_{IL}, V_{TH}, V_{OL}, V_{OH}
Also show the method/graph used to identify their points. Evaluate noise margin.
 - (iv) Analyze whether this circuit can be used as an amplifier? If it, evaluate the maximum gain of this circuit?
 - (v) Plot VTC for $B_n/B_p = 1, 3 \& 5$ on same graph.
Analyze the effect of the strength of the driver on load on VTC, I_m & noise margin.
 - (vi) Analyze static and dynamic power dissipation of this circuit.
- Theory:- A CMOS inverter is a basic logic gate that swaps between two fixed voltage levels of 0 or 1 in digital electronics circuit. When a high input voltage is given to the CMOS inverter, the PMOS transistor switches off, while the NMOS transistor switches on. This avoids

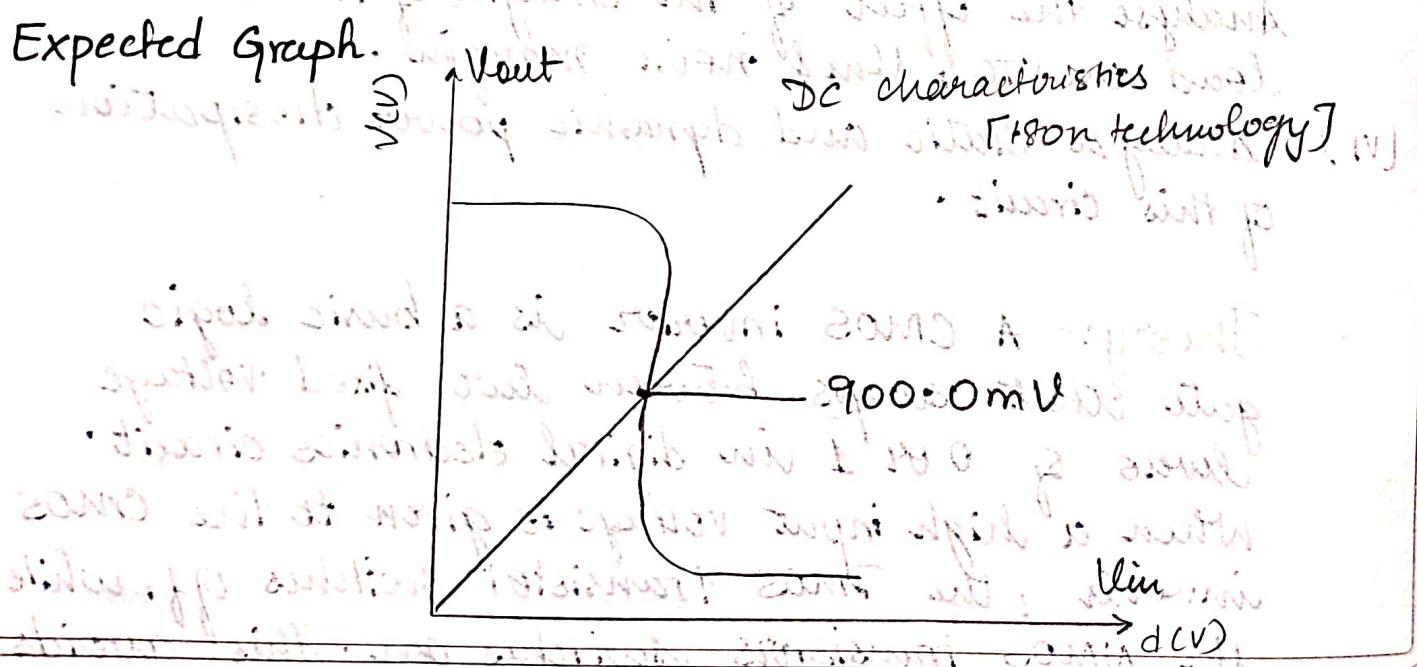
Output Column

PMOS width	VDD/2
1 μm	742.84 mV
2 μm	814.70 mV
3 μm	864.0 mV
4 μm	900.0 mV
5 μm	923.07 mV

(ii) Circuit Diagram VDD



Expected Graph.



Experiment No.

Date :

Name of the Experiment :

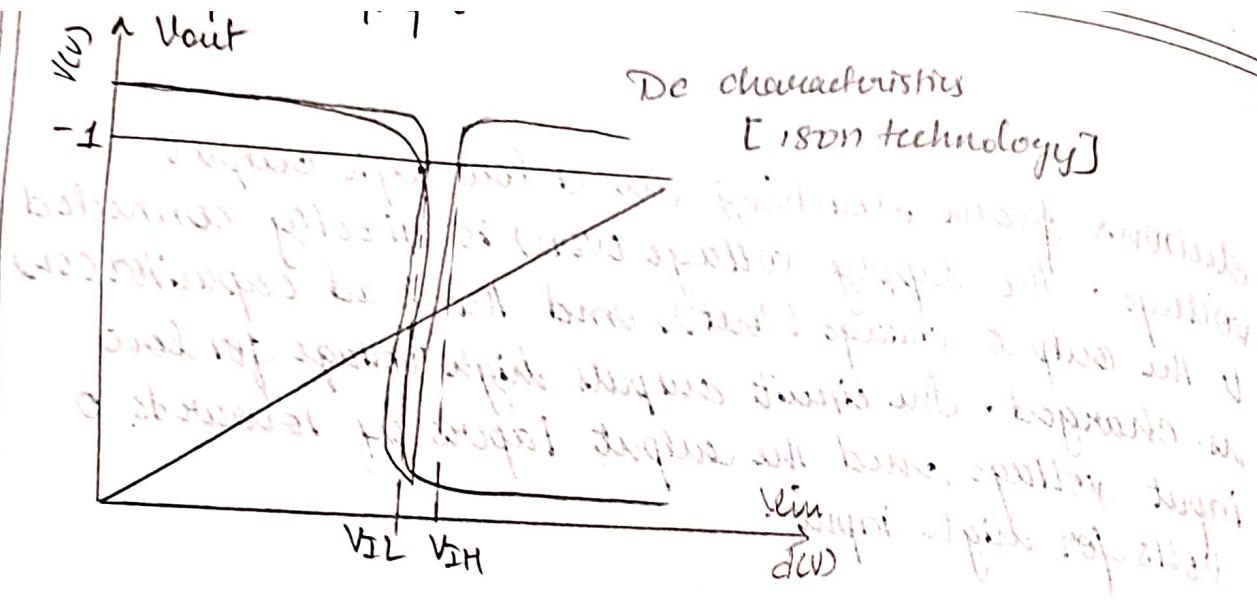
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electrons from reaching in a low logic output voltage. The supply voltage (V_{DD}) is directly connected to the output voltage (V_{out}), and the load capacitor (C_L) is charged. The circuit outputs high voltage for low input voltage, and the output tapers off towards 0 Volts for high input.

- Procedure:

- Invoke the cadence tool from the terminal
- Create an instance for n-mos and p-mos by giving total width = W for p-mos and $1\mu m$ for n-mos.
- Give the wiring for the p-mos and n-mos.
- Give the input, output, V_{DD} and gnd pins.
- Create instances for V_{pulse} and V_{DC} and connect accordingly.
- Finish the connections by giving ground where ever is required.
- Now, to check the transient analysis call the variable ' W ' in design window in lewinch ADEL
- In ADEL window go to tools \rightarrow parametric analysis and give the range and give auto of about 5 by giving range 1μ to 5μ and open in the same window.
- Save the obtained graph.
- In ADEL window, Open calculator [in tools], functions, under special function [select Vs] \rightarrow select Output line \hookrightarrow select driv and simulate in the calculator.
- Split the graph
- Go to marker \rightarrow create marker \rightarrow select horizontal

-1 \leftarrow [Select graph] NMI



Calculations

$$V_{IL} = 776.5707 \text{ mV}$$

$$V_{IH} = 1.03786 \text{ V}$$

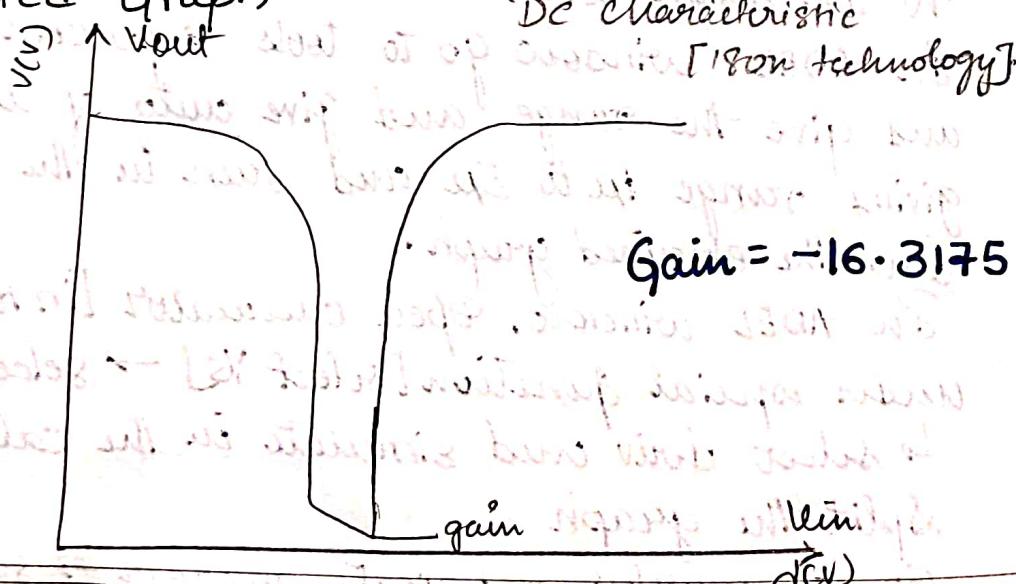
$$N_{MH} = V_{OH} - V_{IH} = 1.8 - 1.03786 = 0.76214$$

$$N_{ML} = V_{ZL} - V_{OL} = 762.14 \text{ mV}$$

$$= 776.5707 \text{ mV} - 0$$

$$\text{Answer is } \underline{\underline{776.5707 \text{ mV}}}$$

(IV) Expected Graph



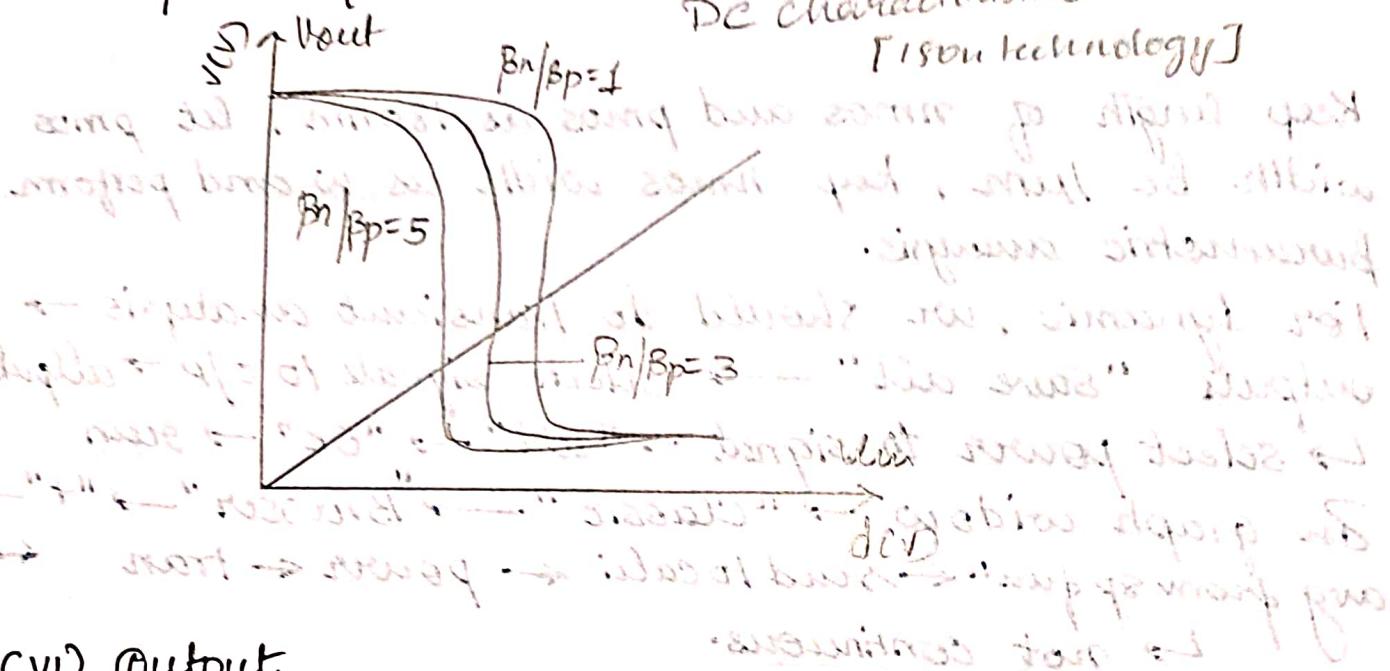
Experiment No.

Name of the Experiment:

Date:
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- Keep length of nmos and pmos as 180nm, let pmos width be 1μm, keep nmos width as w and perform parametric analysis.
- For dynamic, we should do transient analysis → outputs "Save all" → selects signals to O/P → all pub
↳ select power to signal → "all" → "OK" → green
- In graph window → "Classic" → "Browser" → "+" avg from spfun ← send to calc ← power ← tran ↳ not continuous.
- For static, we should do DC analysis → outputs "Save all" → select signals to O/P → all pub
↳ select power to signal → "all" → "OK" → green
- In graph window → "Classic" → "Browser" → "+"
(nmos. → 1μm pmos → 4μm) drop. ↳

(v) Expected Graph



(vi) Output

$$\text{Dynamic Power dissipation} = 1.08 \times 10^{-3} \text{W}$$

$= 1.08 \text{mW}$

$\text{Static Power dissipation} = \underline{\underline{2.67 \times 10^{-11} \text{W}}}$

STEPS TO INVOKE CADENCE TOOL

- Steps Involved

Activities → Files → in home → Desktop →

open in terminal ← open the folder ← Create a file

- Commands:

- csh
- source /home/install/cshrc
- virtuoso

- Creating a New library

file → new → name → attach to an existing
technology library

gdk 180/45/90... ←

- Creating a New Cell view

File → new → cell view → library (name) → name
cell.

- Simulation

- instances → 'i'
- library browse → gpdk 180 → nmos (symbol) / pmos ...
- wiring (w) | create → wire (narrow) | symbol (icon)
- i → browse → analog lib → Vpulse | Vdc ...
- pins → 'P'
- Rotate - 'R'

- To check Outputs

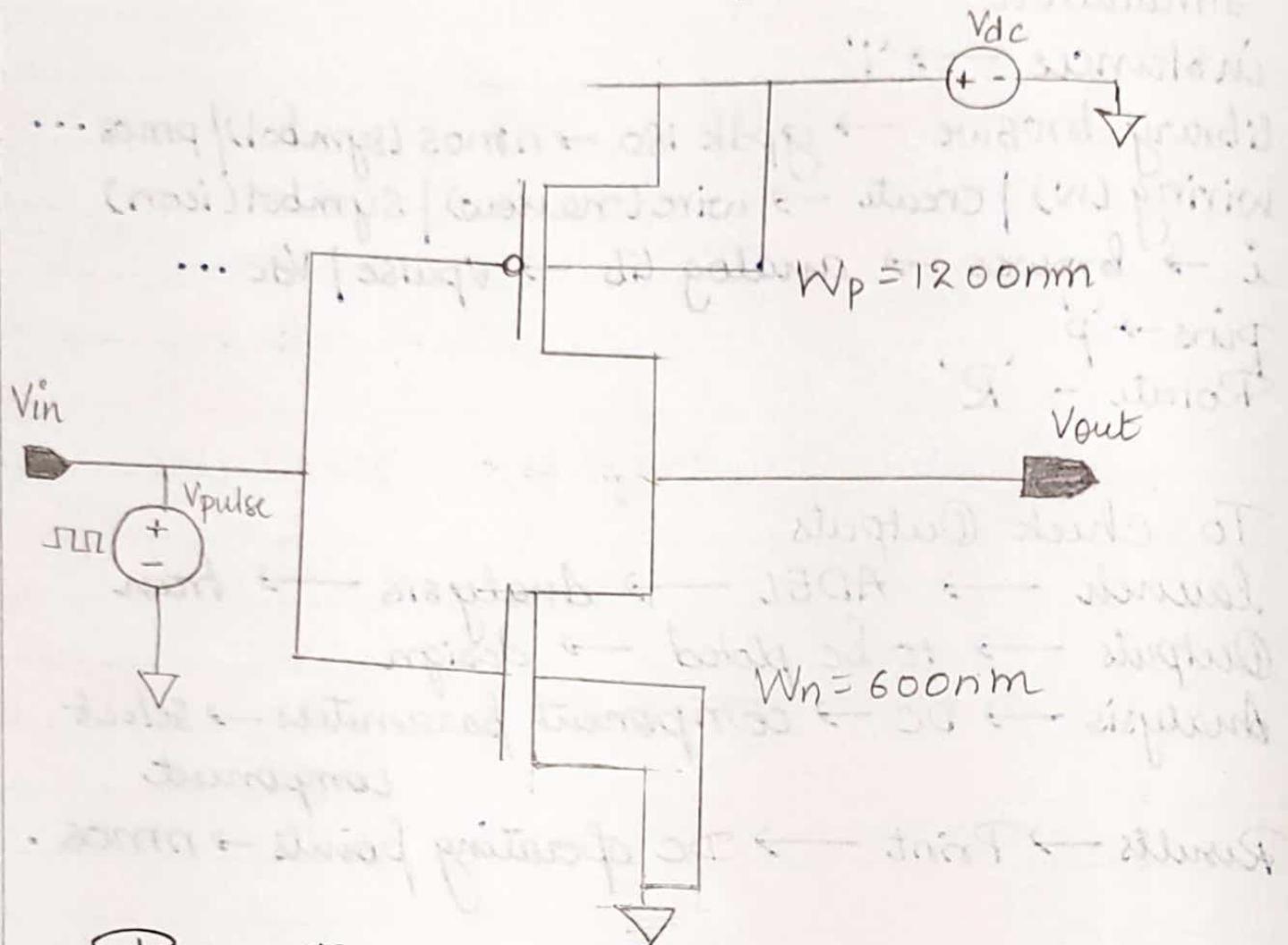
launch → ADEL → Analysis → tran
 Outputs → to be plotted → design
 analysis → DC → component parameters → select
 component

Results → Print → DC operating points → nmos.

29.1.5 pulse
 29.1.2 initial
 29.1.5 initial
 29.1.5 initial select

29.1.5 initial select

Schematic Circuit Diagram:-



Parameters

V_{pulse}

$$DC = 1.8V$$

$$V_{tg\ 1} = 0V$$

$$V_{tg\ 2} = 1.8V$$

$$\text{Period} = 100 \text{ ps}$$

$$\text{delay} = 10 \text{ ps}$$

$$\text{Rise time} = 10 \text{ fs}$$

$$\text{fall time} = 10 \text{ fs}$$

$$\text{Pulse width} = 50 \text{ ps}$$

V_{dc}

$$\text{DC voltage} = 1.8V$$

19/3/24

EXPERIMENT - 01(A)

- Aim :- Design a CMOS inverter at 180nm technology and perform the following using cadence virtuoso, $V_{DD} = 1.8V$ and calculate the transient analysis, DC operating point analysis and list the values of I_{DS} , V_{TH} , V_{DSAT} and region.
- Theory :- CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET [Field effect transistor], composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data in small circuits.
- Procedure :-
 - Invoke cadence tool from the terminal.
 - Make the schematic diagram of CMOS in the workspace.
 - Create an instance for n-mos and p-mos
 - Give the wiring for the p-mos and n-mos
 - Give the input, output, V_{DD} and gnd pins.

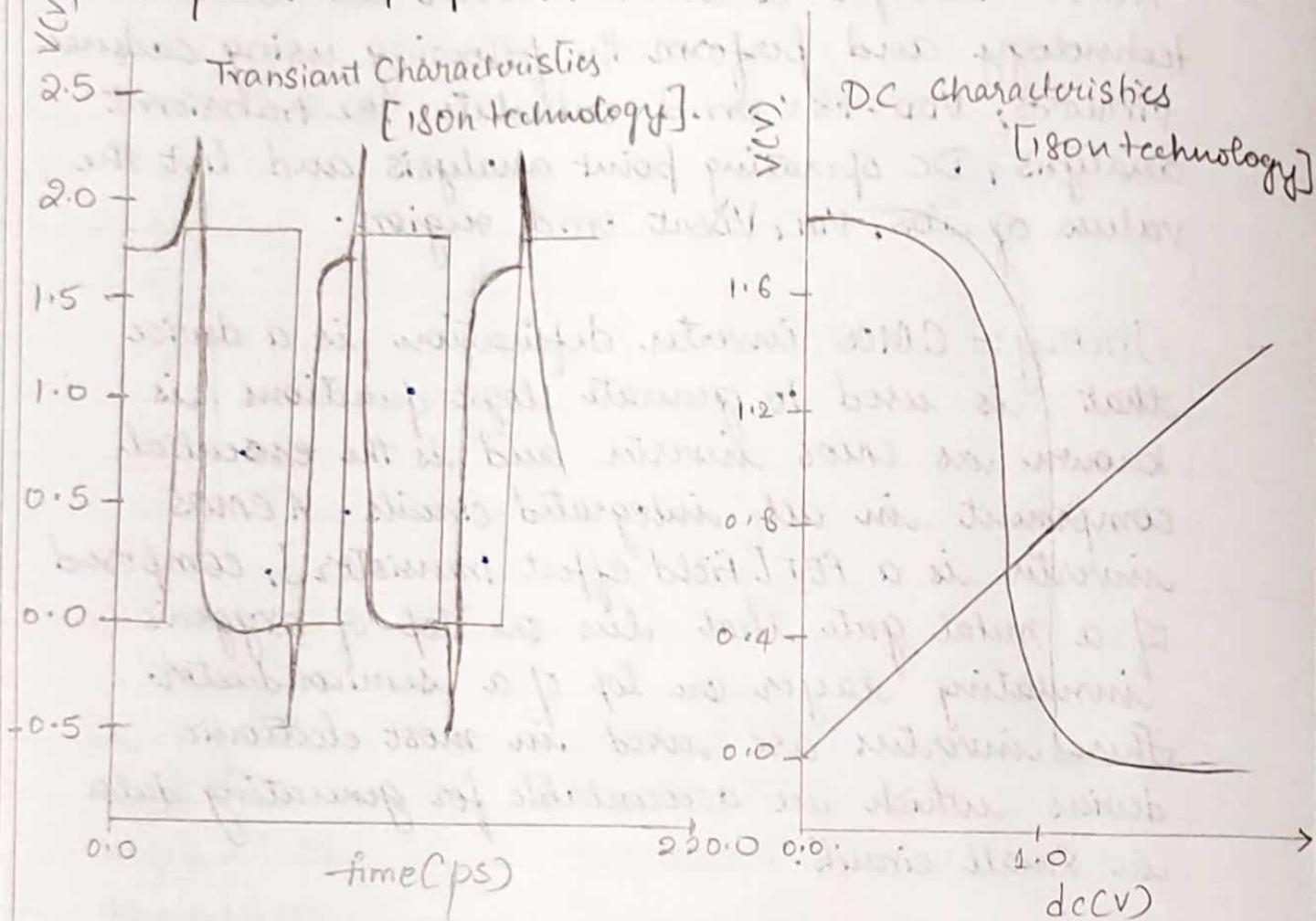
tran Analysis

Stop time - 220p, modulate

DC Analysis

Start - 0 Stop - 1.8

Expected graph



Obtained Parameters

$$I_{DS} = 4.40608P$$

$$V_{DSat} = 486.253m$$

$$V_{TH} = 513m$$

$$\text{Region} = 1$$

Experiment No.

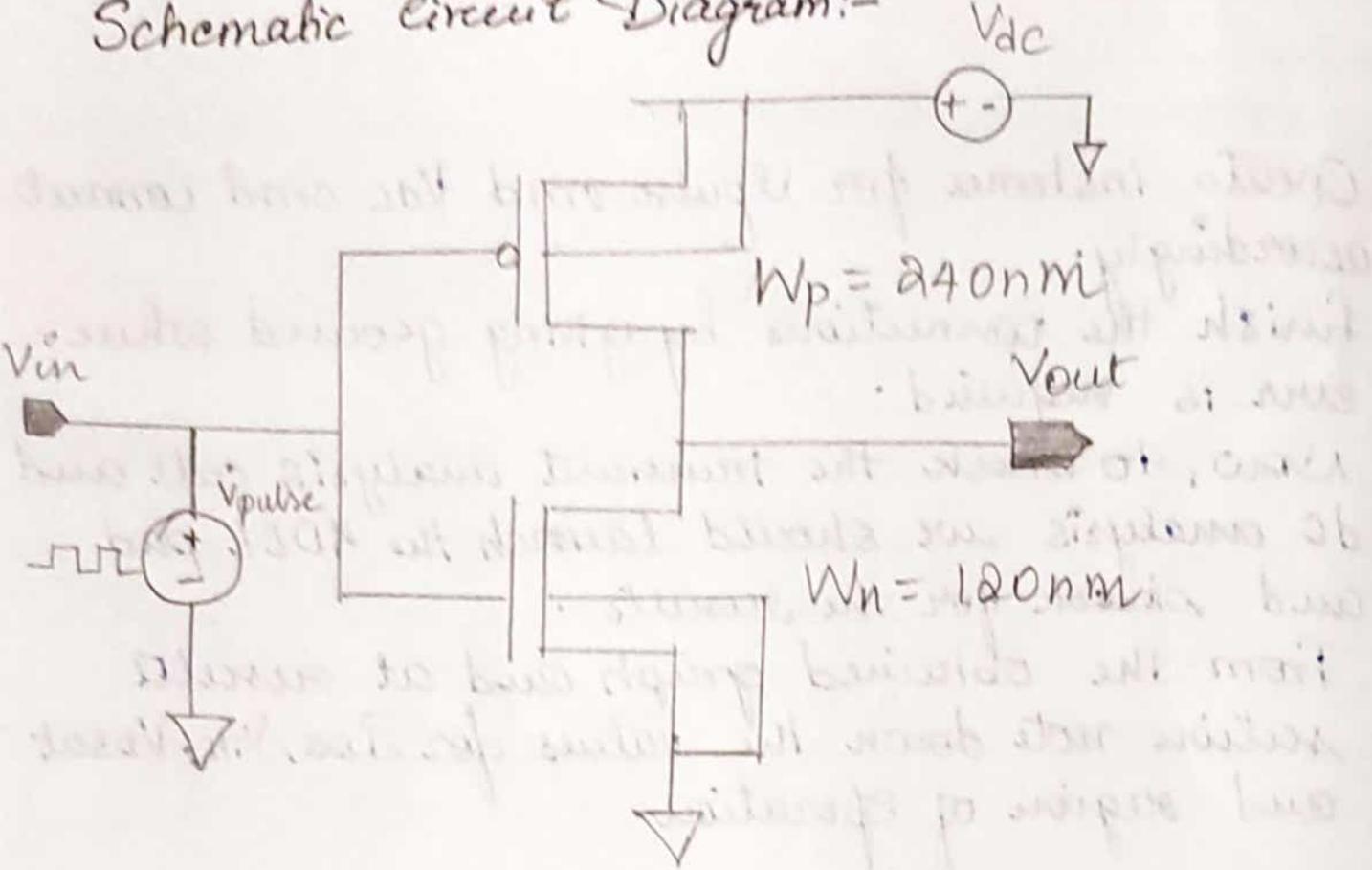
Date

Name of the Experiment

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- Create instance for Vpulse and Vdc and connect accordingly.
- finish the connections by giving ground where ever is required.
- Now, to check the transient analysis call and dc analysis we should launch the ADEL pad and check for the results.
- from the obtained graph and at results section note down the values for I_{DS} , V_{TH} , V_{DSAT} and region of operation.

Schematic Circuit Diagram:-



Parameters

Vpulse

D_C = 1V
V_{Tg 1} = 0V
V_{Tg 2} = 1V
Period = 100ps

delay = 10ps
Rise time = 10fs
Fall time = 10 fs
Pulse width = 50p

Vdc

Dc Voltage - 1V

tran Analysis

Stop time - 220p, moderate

DC Analysis

Start - 0

Stop - 1

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EXPERIMENT-01 (B)

- Aim: Design a CMOS inverter at 45nm technology and perform it in cadence virtuoso having $V_{DD} = 1V$ and calculate the transient, DC operating points analysis and list the values of I_{DS} , V_{TH} , V_{OSAT} and region of operation.
- Theory: CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET [Field Effect Transistor], composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data in small circuits.
- Procedure:
 - Invoke cadence tool from the terminal.
 - Create an instance for nmos and pmos
 - Give the wiring for the p-mos and n-mos.
 - Give the input, output, V_{DD} and gnd pins.
 - Create instance for V_{PULSE} and V_{OC} and connect accordingly.
 - Finish the connections by giving ground where

Experiment No.

Date

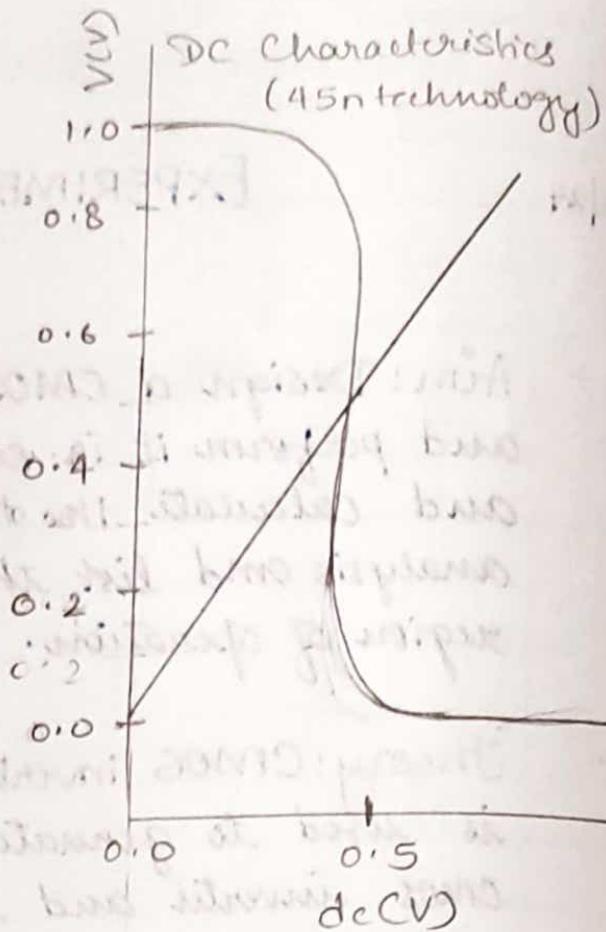
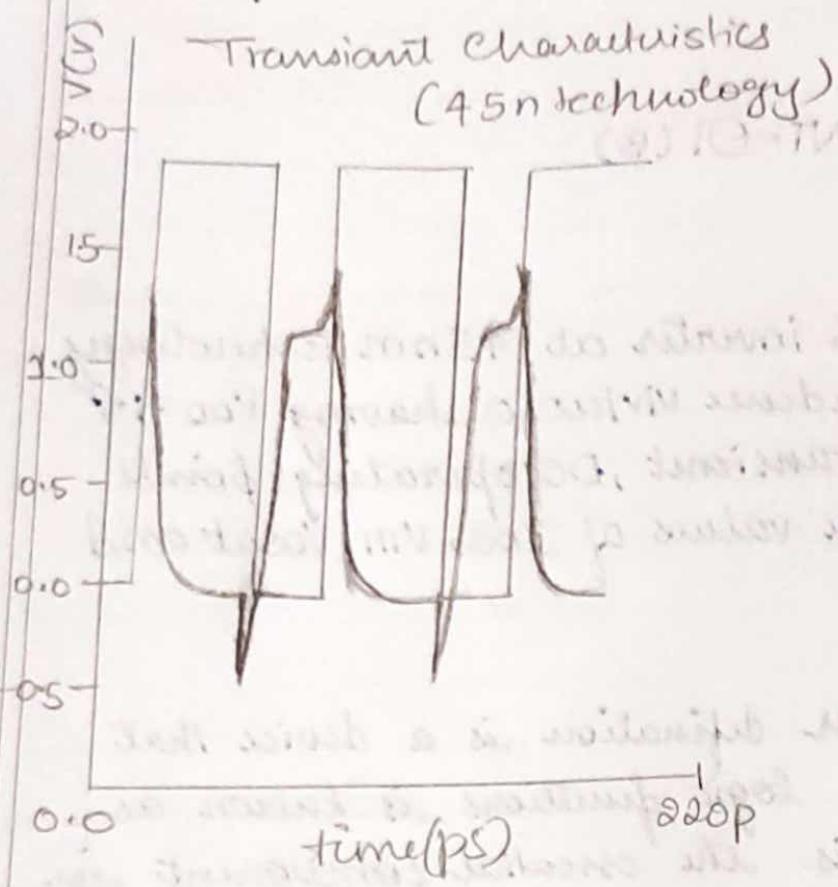
Name of the Experiment

Page No.

ever is required.

- Now, to check the transmitted analysis and DC analysis we should launch the ADEL pad and check for the results.
- From the obtained graph and at results section note down the values for I_{DS} , V_{TH} , V_{Dsat} and region of operation.

Expected Graph



Obtained Parameters

$$I_{DS} = 54.4245 \mu A$$

$$V_{TH} = 611.966 mV$$

$$V_{DSat} = 625.473 mV$$

$$\text{Region} = 1$$