Code No:C214 Set No. 1

BVRIT HYDERABAD COLLEGE OF ENGINEERING FOR WOMEN II B.Tech. I Sem., I Mid-Term Examinations, December-2020 Computer Organization and Architecture Objective Exam

Name: Hall Ticket No.	
Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min.	Marks: 10.
I. Choose the correct alternative:	
 The two phases of executing an instruction are Instruction decoding and storage b) Instruction fetch and instruction execution Instruction execution and storage d) Instruction fetch and Instruction processing 	
2. Location of the operand in instruction is a) operation field b) Mode field c) address field d) None	[]
3. Branch unconditional stands for a) BUS b) BCUN c) BUN d) BDC	[]
4. Interrupts initiated by an instruction is called as a) internal b)external c) software d) hardware	[]
5. In instruction code of 16 bits, length of operation field is a)4 b)8 c) 1 d)3	[]
6. Which type of Microoperation Used to Carry the information from one registe a)Data transfer b) Arithmetic c) Program control d) Logical	r to another []
7. The mode bit is for direct address, for indirect address a) 0,1 b) 1, 0 c) 1,1 d) 0,0	[]
8. In indirect address, defines address of the operand a) Operation code b) memory word c) effective address d) register	[]
9. $(125)_{10} = ()_8$ $a)(145)_8$ $b)(175)_8$ $c)(134)_8$ $d)(205)_8$	[]
10.2's complement of 1011010 a) 0100101 b)0010100 c)1010010 d)0100110	[]

Cont.....2

II. Fill in the Blanks:

11. Length of INPR/OUTR is	
12. A Register capable of shifting a bit to	either left or right once is
13 is the length of Accumulator	
14. Mnemonic for Load the accumulator	is
15 Holds the address of next in	nstruction in the sequence
16. A stack organized computer use	instruction format
17. Next address generator is also called a	us
18. Addressing mode in which operand va	alue specified directly is
19. 1's complement of 1100010 is	.
20. A - B is represented in 2's complement	nt as

Code No:C214 Set No. 2

BVRIT HYDERABAD COLLEGE OF ENGINEERING FOR WOMEN II B.Tech. I Sem., I Mid-Term Examinations, December-2020 Computer Organization and Architecture Objective Exam

Jame:Hall Ticket No.			Hall Ticket No.			
Answer All Questions.	All Questions	Carry Equal M	arks. Ti	ime: 20 Min.	Marks:	10.
I. Choose the correct alter	rnative:					
1. Branch unconditional sta a) BUS c) BUN	nds for b) BCUN d) BDC					[]
2. Interrupts initiated by an a) internal b)external	instruction is c c) software		rdware			[]
3. In instruction code of 16 a)4 b)8	bits, length of c) 1	operation field d)3	is			[]
4.Which type of Microopera a)Data transfer b) Arithmeti		-		m one register	to anoth	ier []
5.The mode bit is for dia		for indirect a	address			[]
6.In indirect address, do a)Operation code b) memo		-	d) registe	r		[]
7.(125) $_{10} = ()_{8}$ a)(145) ₈ b)(175) ₈	c)(134) ₈	d)(20	95) ₈			[]
8.2's complement of 10110 a) 0100101 b)001	10 10100	c)1010010		d)0100110		[]
9.The two phases of execution a) Instruction decoding and c) Instruction execution and	storage b) In	on are astruction fetch struction fetch				[]
10.Location of the operand a) operation field b) Mod	_	s ddress field	d) None			[]

II. Fill in the Blanks:

11 is the length of Accumulator	
12. Mnemonic for Load the accumulator is	
13 Holds the address of next instruction in	the sequence
14. A stack organized computer use	_ instruction format
15. Next address generator is also called as	
16. Addressing mode in which operand value specified	d directly is
17. 1's complement of 1100010 is	
18. A - B is represented in 2's complement as	
19. Length of INPR/OUTR is	
20. A Register capable of shifting a bit to either left or	right once is

Code No: C214 Set No. 3

BVRIT HYDERABAD COLLEGE OF ENGINEERING FOR WOMEN II B.Tech. I Sem., I Mid-Term Examinations, December-2020 Computer Organization and Architecture Objective Exam

Name	:Hall Ticket No.	
A	Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks	: 10.
I.	Choose the correct alternative:	
1. In ii a)4	nstruction code of 16 bits, length of operation field is b)8 c) 1 d)3	[]
	ich type of Microoperation Used to Carry the information from one register to anota a transfer b) Arithmetic c) Program control d) Logical	her []
	mode bit is for direct address, for indirect address b) 1, 0 c) 1,1 d) 0,0	[]
	ndirect address, defines address of the operand eration code b) memory word c) effective address d) register	[]
	5) $_{10} = ()_{8}$ $_{(145)_8}$ b)(175) $_{8}$ c)(134) $_{8}$ d)(205) $_{8}$	[]
6.2's o a) 010	complement of 1011010 00101 b)0010100 c)1010010 d)0100110	[]
a) Inst	two phases of executing an instruction are truction decoding and storage b) Instruction fetch and instruction execution truction execution and storage d) Instruction fetch and Instruction processing	[]
	eation of the operand in instruction is eration field b) Mode field c) address field d) None	[]
9. Bra a) BU c) BU	,	[]
10. In a) inte	aterrupts initiated by an instruction is called as ernal b)external c) software d) hardware	[]

II.Fill in the Blanks:

11 Holds the address of next instruction in t	he sequence
12. A stack organized computer use	instruction format
13. Next address generator is also called as	
14. Addressing mode in which operand value specified	l directly is
15. 1's complement of 1100010 is	
16. A - B is represented in 2's complement as	
17. Length of INPR/OUTR is	
18. A Register capable of shifting a bit to either left or	right once is
19 is the length of Accumulator	
20. Mnemonic for Load the accumulator is	

Code No: C214 Set No. 4

BVRIT HYDERABAD COLLEGE OF ENGINEERING FOR WOMEN II B.Tech. I Sem., I Mid-Term Examinations, December-2020 Computer Organization and Architecture Objective Exam

Name:		Hall Ticket No	o.	
Answer All Questions.	All Questions	s Carry Equal Mark	ss. Time: 20 Min.	Marks: 10.
I.Choose the correct alter	native:			
1.The mode bit is for day 0,1 b) 1, 0 c) 1,1	irect address, d) 0,0	for indirect add	ress	[]
2.In indirect address, do a)Operation code b) memor		<u>-</u>	egister	[]
3. $(125)_{10} = ()_8$ a) $(145)_8$ b) $(175)_8$	c)(134) ₈	d)(205) ₈		[]
4.2's complement of 10110 a) 0100101 b)001	10 10100	c)1010010	d)0100110	[]
5. The two phases of execut a) Instruction decoding and c) Instruction execution and	storage b)	Instruction fetch and		
6. Location of the operand i a) operation field b) Mod	n instruction	is	None	[]
7. Branch unconditional sta a) BUS c) BUN	nds for b) BCUN d) BDC			[]
8. Interrupts initiated by an a) internal b)external	instruction is c) software		vare	[]
9. In instruction code of 16 a)4 b)8	bits , length c	of operation field is _ d)3		[]
10.Which type of Microope a)Data transfer b) Arithmeti		•	ion from one registe	er to another [

II.Fill in the Blanks:

11. Next address generator is also called as	
12. Addressing mode in which operand value spe	cified directly is
13.1's complement of 1100010 is	
14. A - B is represented in 2's complement as	
15. Length of INPR/OUTR is	
16. A Register capable of shifting a bit to either le	eft or right once is
17 is the length of Accumulator	
18. Mnemonic for Load the accumulator is	
19 Holds the address of next instructio	n in the sequence
20 A stack organized computer use	instruction format