UNIT - IV

1. Explain Set Associative mapping for organizing cache memory.
2. Differentiate Isolated I/O and memory mapped I/O.
3. Differentiate Programmed I/O and Interrupt initiated I/O
4. Differentiate logical and physical address representations.
5. Write about first-in and first-out buffers in asynchronous data transfer.
6. Explain Cache memory organization with Associative mapping? Explain how it improves the memory access time?
7. Show internal configuration of a DMA controller diagrammatically and explain how it's working.
8. Explain about Prioritized Interrupts and interrupts cycle.
9. Explain Cache with Set-Associative and direct mapping. Assume your own example address and explain.
10. Explain how memory management unit provides memory protection.
11. Explain with a neat diagram, system configuration incorporating an I/O processor.
12. Explain how the logical address is translated into physical address in paging.
13. Explain the relationship between address and memory space in virtual memory system.
14. Explain the following with respect to serial communication: Character oriented protocol and Bit Oriented protocol.
15. What are the handshaking signals? Explain handshake control of data transfer during input and output operations.
16. Explain Cache with associative and two way Set- Associative mapping with a line size of 4 bytes.
17. What are the techniques used to write Data into the Cache?
18. Explain different types of I/O communication techniques with merits and demerits.
19. What is the need for I/O Processor? Explain the working style of I/O processor.
20. What is Memory system? Define Memory refreshing.
21. What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory.
22. Discuss any six ways of improving the cache performance.
23. Discuss about priority interrupt.
24. Explain about Input-output interface.
25. What do you mean by content addressable memory?
26. Explain the functionalities of memory management hardware.
27. Explain various mapping procedures of cache memory with an example.
28. Demonstrate how communication proceeds between CPU and IOP.
29. Explain in detail various I/O modes of transfer.
30. A computer employs RAM chips of 256×8 and ROM chips of size 1024×8. Extend the memory system to 4096 bytes of RAM and 4096 bytes of RAM. List the memory address map and indicate what size decoders are needed.
31. Demonstrate with an example address mapping using pages.
32. Design parallel priority interrupt hardware for a system with eight interrupt sources.

33. What is direct memory transfer? Give an overview and the block diagram of a DMA controller.
34. What do you mean by vectored interrupt?
35. Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 µs; level 2 contains 1,00,000 words and has an access time of 0.1µs. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose, we ignore the time required to determine whether the word is in level 1 or level 2 and 95% of the memory accesses are found in the cache, then what is the average access time of a word.
36. What is cache memory? What are its advantages? Explain.
37. Demonstrate interrupt-initiated I/O.
38. Explain the functionalities of an IOP interface unit.
39. What do you mean by associative memory? Give applications of associative memory.
40. Demonstrate logical to physical address mapping using segmented-paging.
41. What is virtual memory? Explain.
42. Give an overview of parallel priority interrupt hardware.
43. Discuss the different mapping techniques used in cache memories and their relative merits and demerits.
44. Discuss about memory management hardware.
45. Describe the data transfer method using DMA.
46. Discuss the design of a typical input or output interface.
47. How main memory is useful in computer system? Explain the memory address map of RAM and ROM.
48. Discuss associative mapping and direct mapping in organization of cache memory
49. Explain paging and address translation with example.
50. What is cache coherence? Explain in brief.
51. What is cache memory? Explain how it enhances speed of accessing data?
52. What is asynchronous data transfer? Differentiate between strobe control method and handshaking method.
53. What is cache miss and cache hit?
54. Explain the significance of every bit of Program Status Word (PSW).
55. Differentiate Programmed I/O and Interrupt initiated I/O
56. Define the virtual memory organization and explain briefly?
57. Explain cache memory to reduce the execution time?
58. Define CPU registers, Main memory, Secondary memory and cache memory?
59. List the various types of semiconductor RAMs?
60. Define Random Access Memory and types of RAMs present?
61. Explain the necessary for memory hierarchy?
62. Define HIT and MISS ratio in memory with an example?
63. Differentiate SRAM and DRAM?
64. List out two kinds of address locality of reference in cache memory?

65. List out the two parameters for performance of a computer system?
66. State the differences between static and dynamic memories?
67. Define virtual or logical address?
68. Define cache memory? Explain how it is used to reduce the execution time? Explain the mapping procedures adopted in the organization of a Cache Memory?
69. Discuss the function of a TLB? (Translation Look-aside Buffer)
70. Differentiate volatile and non volatile memory organization?
71. Discuss the multilevel hierarchy of storage devices?
72. Explain memory management unit (MMU)? Discuss the enhancements used in the memory management?
73. List the factors that determine the storage device performance?
74. Define Memory Access Time?
75. Discuss RAM and ROM chips with diagrams?
76. State and Explain virtual memory organization technique?
77. Define a mapping function? Explain Set-Associative mapping technique?
78. Define virtual memory? Discuss Address mapping using pages in virtual memory?
79. Explain i) ROM ii) PROM iii)EPROM iv)EEPROM.
80. Explain i) Write through policy ii) write back policy iii) Hit and Miss ratio.
81. Explain virtual memory Address translation?
82. Explain briefly about Memory connection to CPU?
83. Discuss Strobe Control method of Asynchronous data transfer technique?
84. Explain Asynchronous communication interface with diagram?
85. Discuss various techniques used for Modes of Transfer?
86. Describe asynchronous serial transfer? Discuss Handshaking method of Asynchronous data transfer technique