Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, September - 2021
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Draw the block diagram of a digital computer and explain the purpose of each part.
b) Design a 4-bit combinational circuit decrementer using four full-adder circuits. [6+9]

2. What are the common fields found in instruction format? Explain various instruction formats based on types of CPU Organization? [15]

3. Perform the arithmetic operation (+41)+(-13) and (-41)-(-13) in binary using signed 2's complement representation for negative numbers. [15]

4.a) Draw the block diagram of a typical DMA controller and explain.
b) Explain Daisy-Chain priority interrupt in detail. [8+7]

5.a) Construct a diagram for a 4×4 omega Switching network. Show the switch setting required to connect input 3 to output 1.
b) Give a brief note on mutual exclusion with a semaphore. [9+6]

6.a) Differentiate between computer organization and computer architecture.
b) Explain the Stored Program organization in detail. [7+8]

7. Explain the microprogram sequencer for a control memory with a neat diagram. [15]

8. Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in the signed-2's complement representation. [15]

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