# UNIT - V

1. What is cache coherence? Explain in brief.
2. Explain pipeline processing conflict.
3. Explain Flynn's classification
4. What is speedup? Derive the equation of speedup for k-segment pipeline processing for task
5. What is tightly coupled and loosely coupled multiprocessor architecture.
6. Draw and explain shared memory architecture of multiprocessor system.
7. Explain RISC and CISC processor.
8. Explain overlapped register windows.
9. Explain daisy chain arbitration.
10. Differentiate between tightly coupled and loosely coupled systems
11. Describe SIMD array processor.
12. Explain Daisy chain priority interrupt.
13. Write down the expressions for speedup factor in a pipelined architecture.
14. Describe in detail about pipeline processing.
15. Write short notes on Interprocessor Communication and Synchronization.
16. Explain the concept of pipelining for floating - point addition and subtraction.
17. Derive speedup achieved by a pipeline unit over a non-pipeline unit.
18. Define cycle stealing.
19. Give the major characteristics of RISC and CISC architectures.
20. Design parallel priority interrupt hardware for a system with eight interrupt sources.
21. What are the pipeline conflicts that cause the instruction pipeline to deviate from its normal operation?
22. Illustrate with an example an instruction pipeline.
23. Illustrate with an example an arithmetic pipeline.
24. What is bus arbitration? Explain.
25. Distinguish between multiprocessors and multi computers.
26. Discuss about priority interrupt.
27. What are multiprocessors? Mention the categories of multiprocessors?
28. List the major MIMD Styles.
29. Describe the data and control path techniques in pipelining.
30. What is the need for replacement? Explain various cache block replacement algorithms.
31. Write about i) No-operations ii) instruction reordering iii) annulling
32. What is cache coherence problem? Explain various protocols to handle it.
33. Explain how to resolve branch conflicts in Instruction pipeline.
34. Discuss various inter connection structures available for multiprocessor systems.
35. What is data transparency?
36. Define delayed load and delayed branch.
37. Write short notes on the following
38. a) Parallel Arbitration b) Matrix multiplication using vector processing. c) RS232 serial Interface.

39. Write short notes on three segment instruction pipeline.
40. Explain different physical forms available to establish inter-connection between various functional units in multiprocessor systems.
41. With neat sketch explain Time Shared Common Bus Organization and also discuss its merits and demerits.
42. Explain different hazards in pipeline concept while an instruction is transferred?