2022 NYCU Computer Aided Design - Homework 4 Report

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1 Lab1: Show the waveform of vctrl signal and schematic view

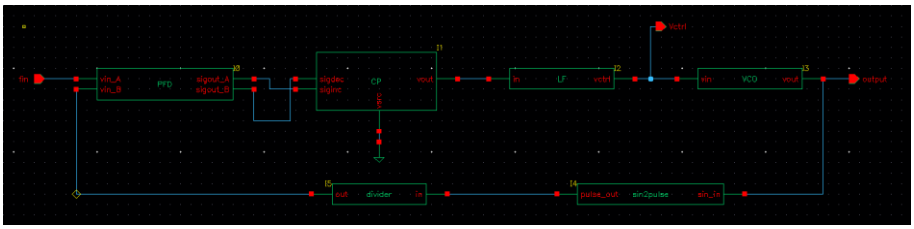


Fig1. Lab1 - PLL schematic view

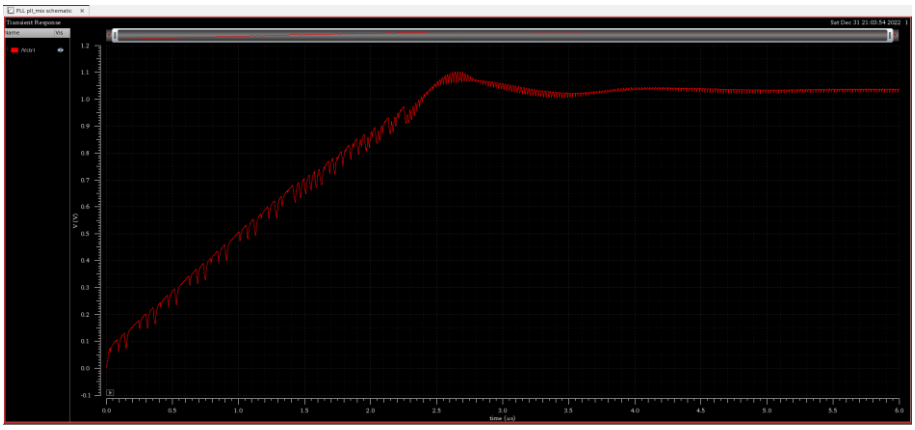


Fig2. Lab1 - Vctrl signal waveform

2 Lab2: Show the waveform of vctrl signal, the output of the divider, and the schematic view

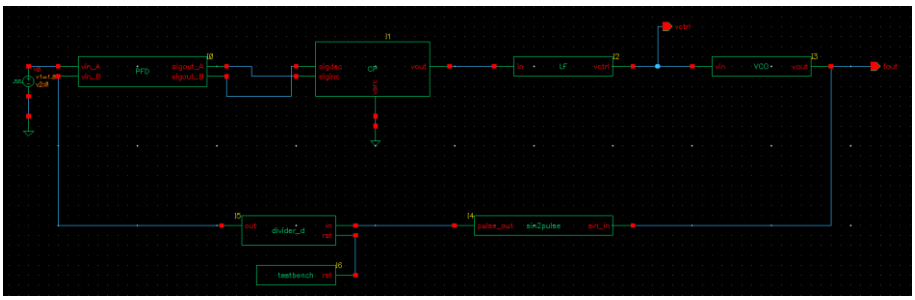


Fig3. Lab2 – Mix-PLL schematic view

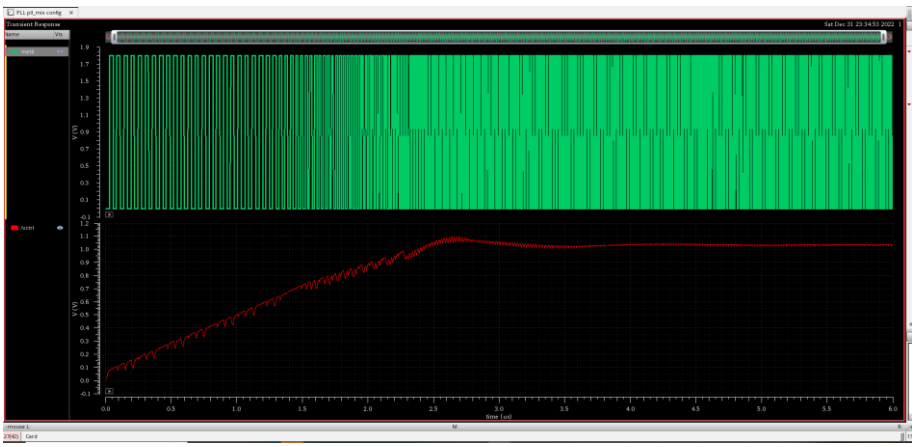


Fig4. Lab2 – Vctrl signal & output of divider waveform

3 Lab3

(1) Schematic cellview

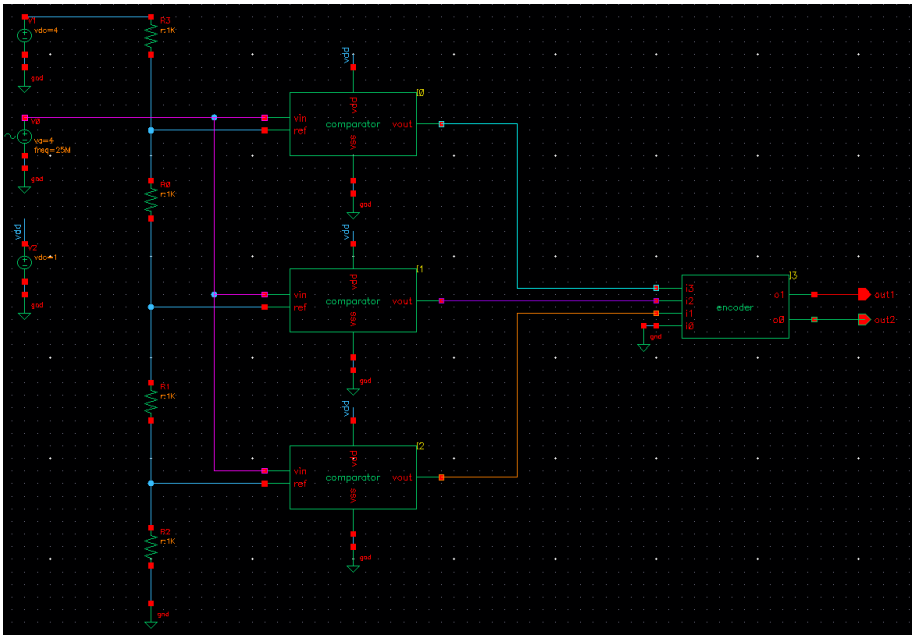


Fig5. Lab3 – 2-bit ADC with Verilog-AMS schematic cellview

(2) The waveform of outputs of comparators, Encoder and Input

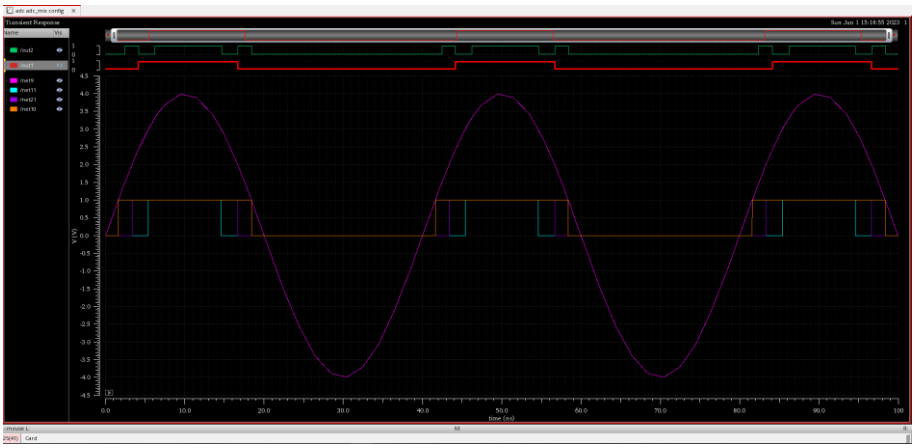


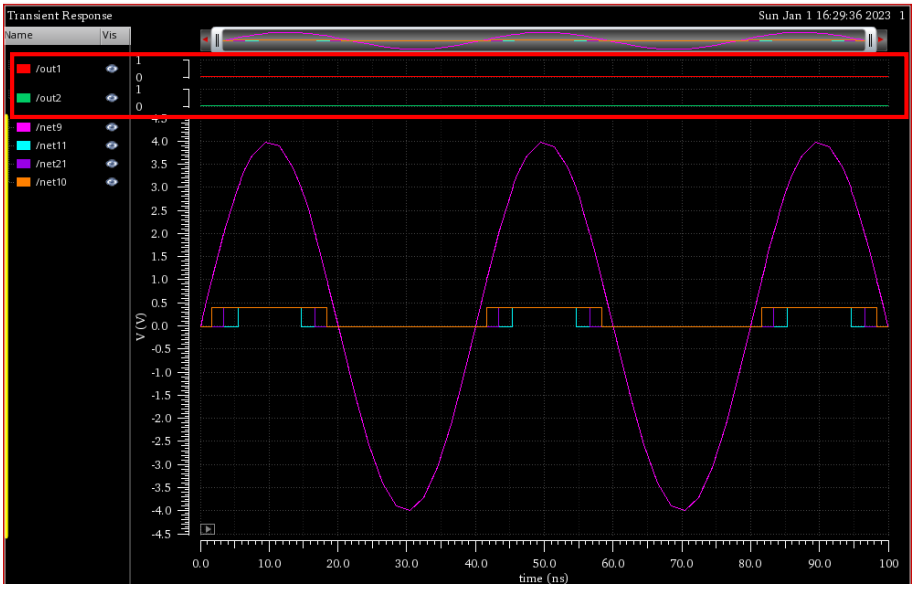
Fig5. Lab3 – Waveform of outputs of comparators, Encoder, and Input

4 What you have learned from this homework?

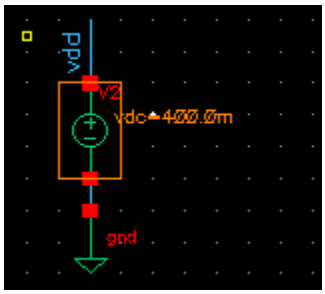
透過這 3 個 Lab 的實作，讓我了解到如何使用 Cadence Virtuoso 的 tool 與使用 Verilog-A & Verilog-AMS 來模擬類比訊號與混和訊號的電路。透過類似 Verilog 的語法，就能快速模擬出電路的 behavior，這個真的方便許多。經過這次 Lab 也讓我回憶以前 VLSI 在畫 Schematic 的技巧，讓整體熟練度又提升了不少！

5 Questions and solutions

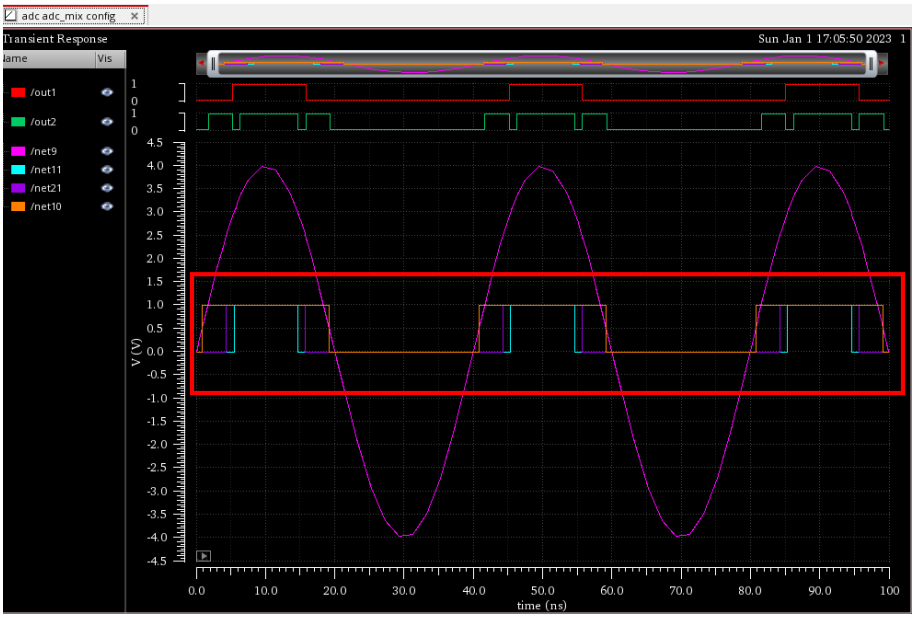
(1) Questions 1: 在以下 Lab3 圖中，encoder 的 output 沒有值的原因可能是甚麼?



Solutions 1：Op-amp comparators 的 Vdd 太小(ex: Vdd = 0.4V)。



(2) Questions 2: 在以下 Lab3 圖中，comparators 的 output 不符合預期的原因可能是甚麼?



Solutions 2：電阻值不相同導致 comparators 輸入的分壓不一致。