2023 Spring NYCU Digital Integrated Circuits – Homework2
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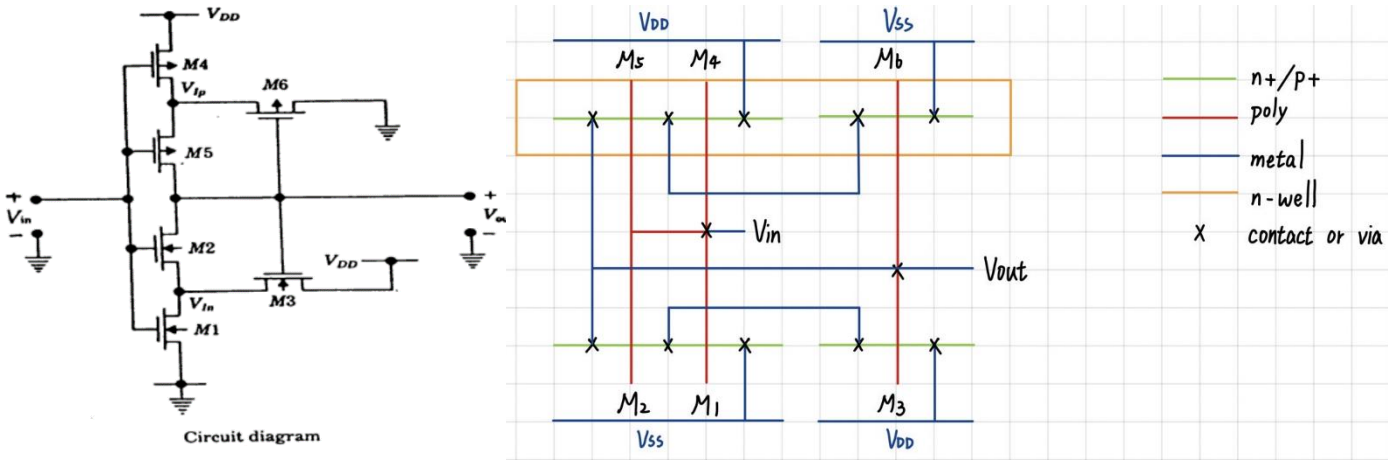
Using 32 nm CMOS devices with VDD= 0.9 V, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of V_t: High V_t, medium V_t and low V_t CMOS

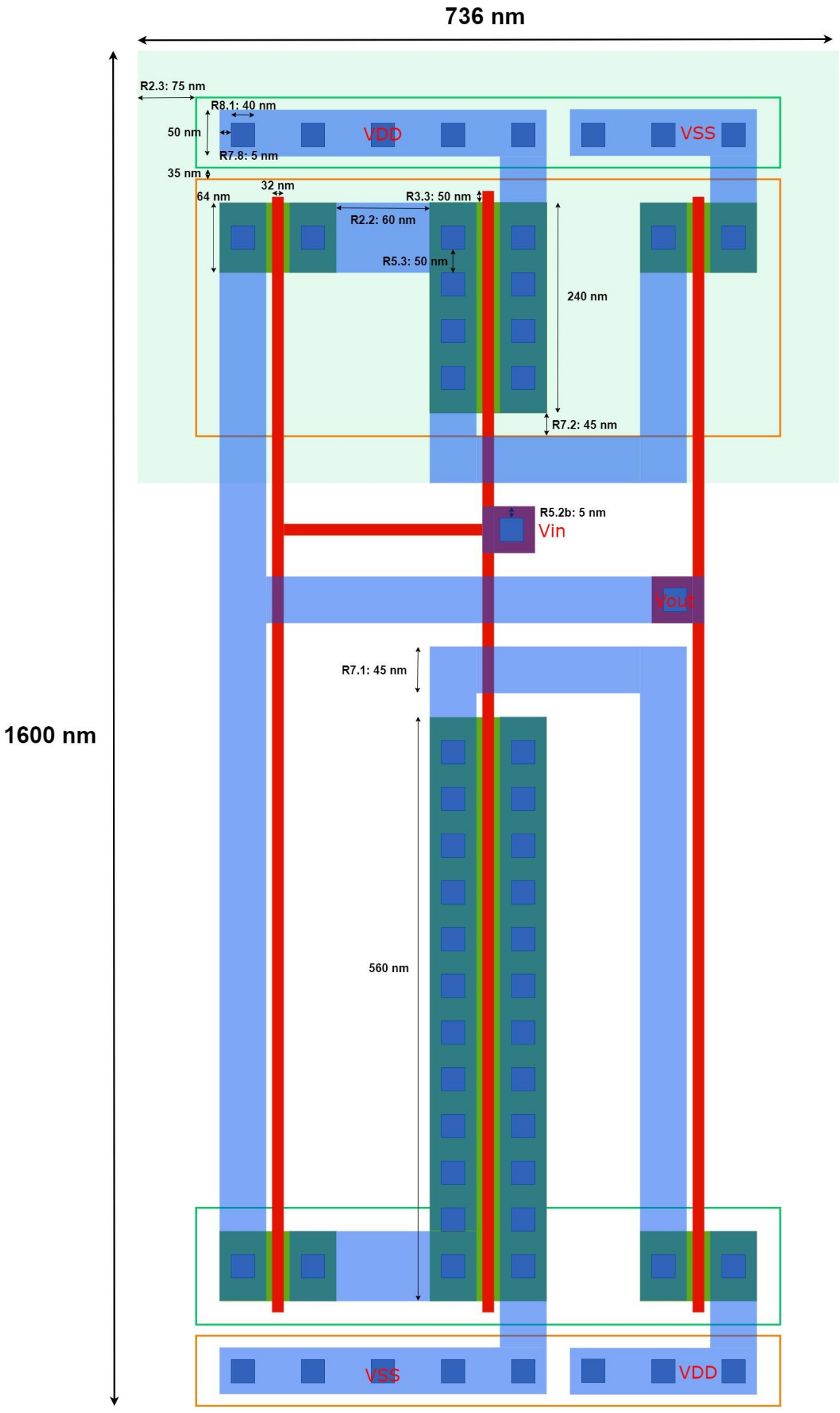
1. (50%) Draw the layout (in a standard cell layout style like the NAND3) of the Schmitt trigger that you design at HW1 using the design rules of table 3.3 with a scale factor of 32/65 for 32nm case for all rules. Use the style as shown in Fig.1.39 to show each layer. You should include substrate contact in your layout. List the square area (? um by ? um) of your rectangular cell. Also, in your layout, mark at least five rules as that shown in Fig.3.19. (Do your best to have a compact layout and list the X and Y size. The size of the area will not affect your score)

首先，先依照 Schmitt trigger 的 schematic 畫出 layout 對應的 stick diagram，並盡量讓 metal 的連線簡單、不重疊，然後盡可能地去優化。



然後使用 HW1 的參數來設計 Schmitt trigger NMOS 與 PMOS 的 Size，並盡量使用最極限的 design rule 去將 layout 畫出來。最終 layout 的 square area ，經過估算約等於 1600 nm x 736 nm = 1177600 (nm x nm)。

	M1	M2	M3	M4	M5	M6
Type	NMOS	NMOS	NMOS	PMOS	PMOS	PMOS
W / L [nm / nm]	560/32	64/32	64/32	240/32	64/32	64/32
W * L [nm * nm]	17,920	2,048	2,048	7,680	2,048	2,048
Total W * L [nm * nm]	33,792					


736 nm
1600 nm
R2.3: 75 nm
R8.1: 40 nm
50 nm
R7.8: 5 nm
35 nm
VDD
VSS
32 nm
64 nm
R3.3: 50 nm
R2.2: 60 nm
R5.3: 50 nm
240 nm
R7.2: 45 nm
R5.2b: 5 nm
Vin
Vout
R7.1: 45 nm
560 nm
VSS
VDD

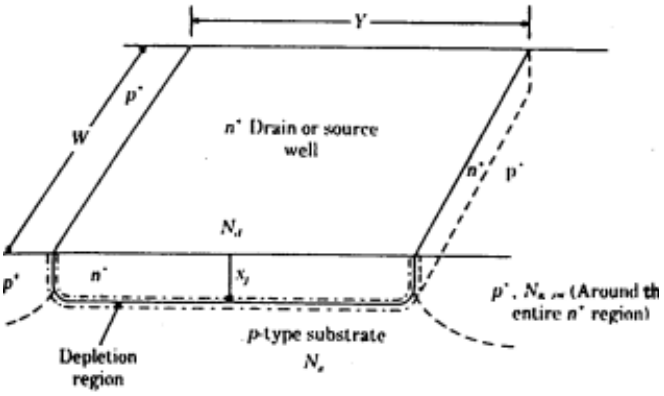
2. Do the power and timing analysis of the schmitt trigger which has two fanouts of the same Schmitt trigger.

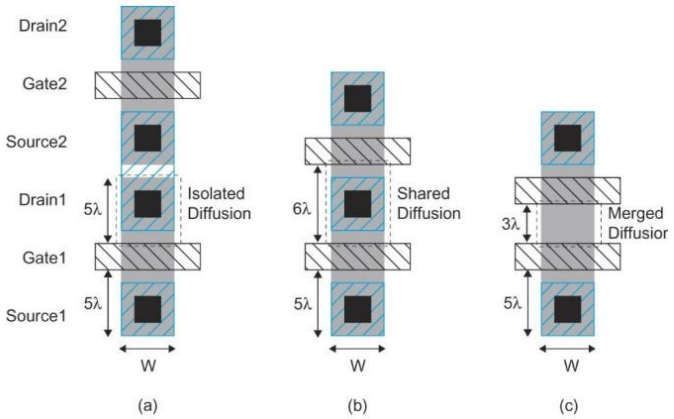
(i) (10%)Run SPICE to get the input and output capacitance of the Schmitt trigger when input and output are in 0/1 and 1/0 respectively (Be careful to indicate the AD, AS, PD, PS)

下表為 Homework 1 設計的電路元件規格:

	M1	M2	M3	M4	M5	M6
Type	NMOS	NMOS	NMOS	PMOS	PMOS	PMOS
W / L [nm / nm]	560/32	64/32	64/32	240/32	64/32	64/32

根據講義第 4 章 p.5 的公式，可以計算出對應的 AS, AD, PS, PD：





- Rule 5.1: Contact – Width (exact) = 0.8 μm
- Rule 5.4: Contact – Spacing to gate = 0.07 μm
- Rule 5.2(b): Contact – Overlap by poly or active = 0.01 μm

$Y_{Drain} = (0.07 + 0.08 + 0.07) * \frac{32}{65} = 108.31\ (nm)$

$Y_{Source} = (0.07 + 0.08 + 0.01) * \frac{32}{65} = 78.77\ (nm)$

Area: AD = AS = W x Y

	Drain			Source		
	W (nm)	Y (nm)	AD (f)	W (nm)	Y (nm)	AS (f)
M1	560	108.31	60.6536	560	78.77	44.1112
M2	64	108.31	6.93184	64	78.77	5.04128
M3	64	108.31	6.93184	64	78.77	5.04128
M4	240	108.31	25.9944	240	78.77	18.9048
M5	64	108.31	6.93184	64	78.77	5.04128
M6	64	108.31	6.93184	64	78.77	5.04128

Sidewall perimeter: PD = PS = 2 (W + Y)

	Drain			Source		
	W (nm)	**Y (nm)**	**PD (nm)**	**W (nm)**	**Y (nm)**	**PS (nm)**
M1	560	108.31	1336.6	560	78.77	1277.5
M2	64	108.31	344.62	64	78.77	285.54
M3	64	108.31	344.62	64	78.77	285.54
M4	240	108.31	696.62	240	78.77	637.54
M5	64	108.31	344.62	64	78.77	285.54
M6	64	108.31	344.62	64	78.77	285.54

SPICE 模擬結果如下:

- 0→1

```
maximum nodal capacitance=   2.025E-15          on node     0:fnode

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:fnode   =   2.0250f 0:out2    = 484.9857a 0:out3    = 484.9857a
+0:vdd     =   0.      0:vin     =   1.0316f 0:vss     =   0.
+1:n12     =   1.5395f 1:n45     = 715.8752a 1:vdd     =   1.8645f
+1:vss     = 196.9073a 2:n12     =   1.2146f 2:n45     = 754.6210a
+2:vdd     =   1.8487f 2:vss     = 196.1273a 3:n12     =   1.2146f
+3:n45     = 754.6210a 3:vdd     =   1.8487f 3:vss     = 196.1273a
```

- 1→0

```
maximum nodal capacitance=   2.002E-15          on node     0:fnode

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:fnode   =   2.0024f 0:out2    = 484.9857a 0:out3    = 484.9857a
+0:vdd     =   0.      0:vin     = 758.6994a 0:vss     =   0.
+1:n12     =   1.2146f 1:n45     = 754.6210a 1:vdd     =   1.8487f
+1:vss     = 196.1273a 2:n12     =   1.2146f 2:n45     = 754.6210a
+2:vdd     =   1.8487f 2:vss     = 196.1273a 3:n12     =   1.2146f
+3:n45     = 754.6210a 3:vdd     =   1.8487f 3:vss     = 196.1273a
```

整理成表格如下：

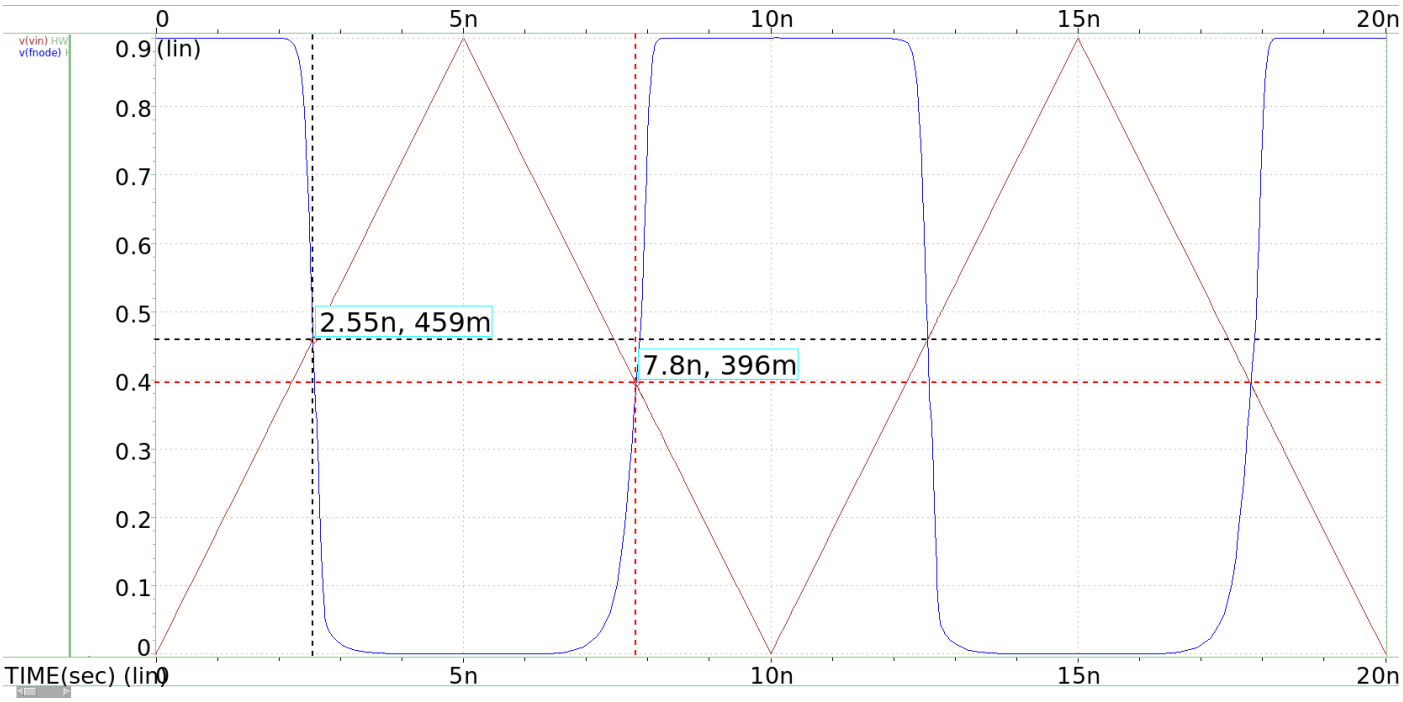
Input / Output	Input Capacitance (aF)	Output capacitance (fF)
0 / 1	1.0316	2.0250
1 / 0	758.6994	2.0024

由 SPICE 的模擬結果可以發現，Input 與 Output 的變化會影響到 NMOS 與 PMOS 的操作狀態，再不同的操作狀態，等效的電容值都不太一樣，而這些值也會受到 Area (AS, AD)與 Sidewall perimeter (PS, PD)的影響，因此在設計電路時，也需要將 Input / Output 的變化、AS, AD, PS, PD 的大小納入考量。

(ii) With inputs like a triangular waveform with the duration of (I) 10ns and (II) 2ns (T0) respectively, run spice to get the timing waveform like that shown in the following figure:

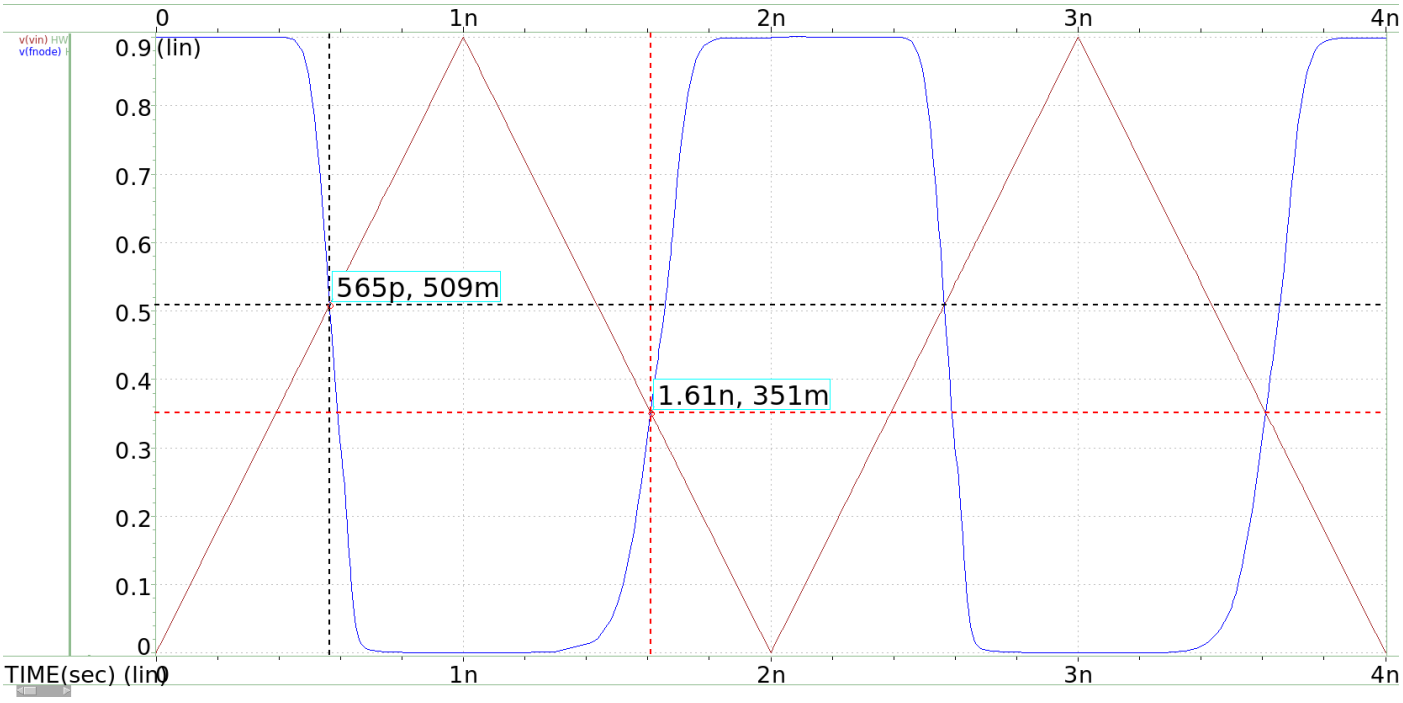
(a) (10%) List the V+ and V- and tdf and tdr of the first stage Schmitt trigger for cases (I) and (II), Discuss the difference of these V+ /V- with that of HW 1.

- Case (I): 10ns




```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tdr= 361.4936p  targ=  17.8615n   trig=  17.5000n
tdf=  55.0957p  targ=  12.5551n   trig=  12.5000n
```

- Case (II): 2ns




```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tdr= 138.9369p  targ=   3.6389n   trig=   3.5000n
tdf=  73.9858p  targ=   2.5740n   trig=   2.5000n
```

通過 SPICE 的模擬，可以得到考慮 AD, AS, PD, PS 與後面有兩級 Schmitt trigger 作為負載的模擬結果。結果如下表：

	V+		V-		tdr	tdf
	HW1	HW2	HW1	HW2		
Case (I): 10 ns	0.415 V	0.459 V	0.386 V	0.396 V	361.4936p	55.0957p
Case (II): 2ns		0.509 V		0.351 V	138.9369p	73.9858p

經過這次的實驗可以發現，HW1 與 HW2 所模擬出來 V+與 V-的結果並不相同。從表中可以看到 V+再考慮了 AD, AS, PD, PS 的效應與後面有負載的情況，V+有明顯的上升，也代表閾值變大，意味著輸入訊號必須超過更高的值才能將訊號翻轉；而 V-在 Case (I) 的情況上升了一些，使原本設計的 Schmitt Trigger 更容易將訊號翻轉，而在 Case (II) 的情況下降了一些，輸入訊號需要更低的值才能將訊號翻轉。tdr 與 tdf 在兩種不同 case 的模擬結果也不相同。由此可知，訊號的頻率也會影響 tdr, tdf 的大小。

(b) (20%) Get the power waveform and the average power dissipation of the first stage of the schmitt trigger. Compare the average power dissipation with the dynamic power equation. Discussion your observation.

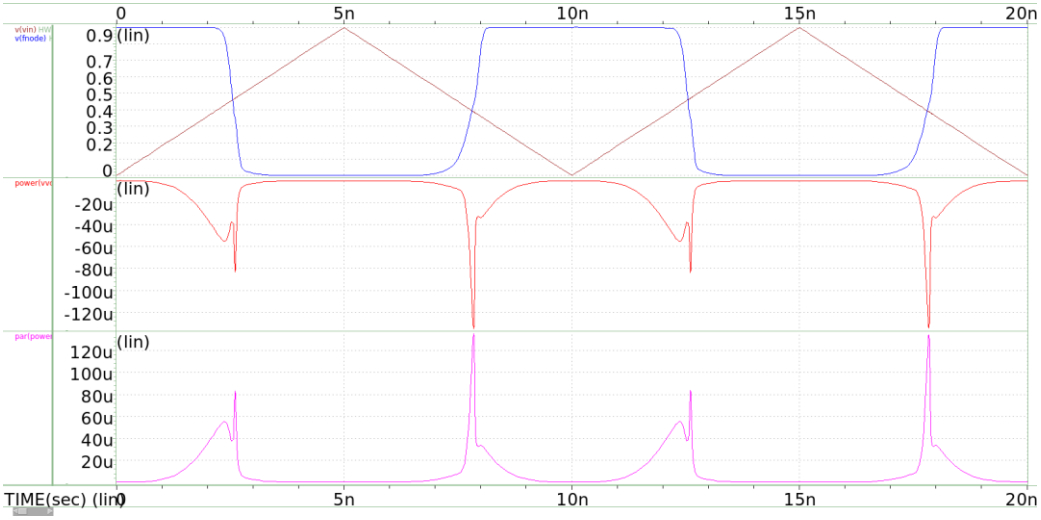
$$Average\ \ Power\ \ Dissipation: P_{avg} = \frac{Re(\boldsymbol{VI}^*)}{2} \tag{2.1}$$

$$Dyanmic\ \ Power\ \ Equation:\ P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt = \frac{V_{DD}}{T}[Tf_{sw}CV_{DD}] = CV_{DD}{}^2 f_{sw} \tag{2.2}$$

平均功率消耗與輸入訊號的變化無關，是針對電路在一段時間內平均消耗的功率來衡量。
動態功率消耗是因為輸入 Switching、電容充電放電而消耗的功率，與電容、電壓平方、切換頻率成正比。因此，由公式 2.2 可以得知，Case (II) 輸入的頻率較 Case (I)高，在 VDD、等效電容差不多的情況下，可以預期 Case (II)的 dynamic power dissipation 會比較高。

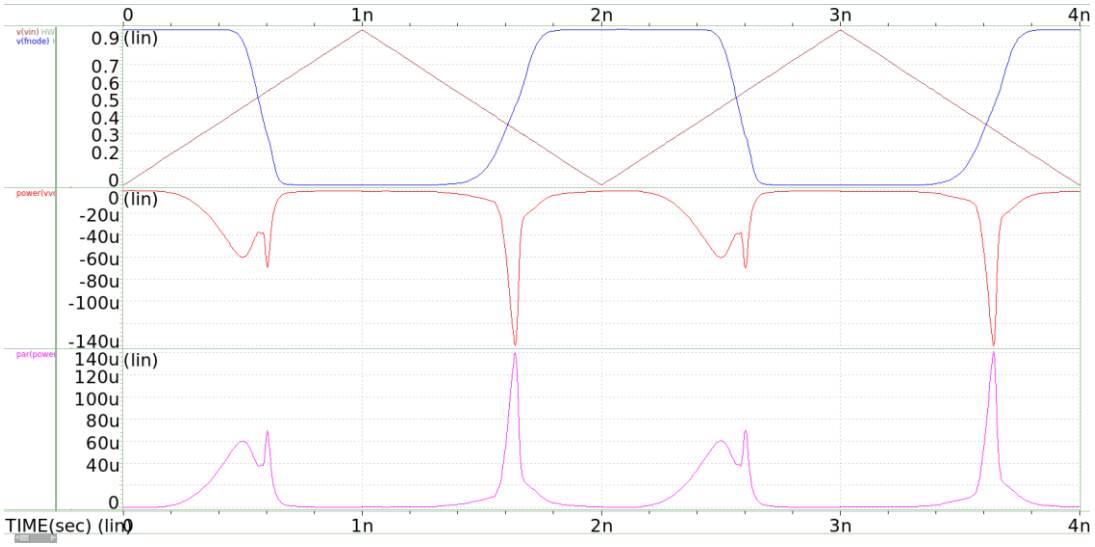
由 hspice 模擬的結果可得知:

- Case (I): 10ns



Average power = 10.0831u W

- Case (II): 2ns



Average power = 12.6920u W

由本次模擬可以發現，Case (II)的 switching frequency 較高，繪製出來的 dynamic power 的曲線(粉紅色曲線)下面積大於 Case (I) 曲線下的面積，代表 Case (II)的動態功耗較高，也驗證了公式(2.2)的所評估的預期結果是符合的。在 Average power 的部分，Case (II) 也是相相於 Case (I) 高了一些。

(c) (10%) Get the leakage power of Schmitter trigger when input is logic 1 and logic 0 respectively.

```
.alter
Vinn vin gnd 0.0
.meas tran leakagepwr0 AVG power from=0.01n to=5n
```

```
.alter
Vinn vin gnd 0.9
.meas tran leakagepwr1 AVG power from=0.01n to=5n
```

- Case (I)
  - Logic 0
  - Logic 1

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepwr0= 123.2915n  from=  10.0000p     to=   5.0000n
```

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepwr1= 166.1014n  from=  10.0000p     to=   5.0000n
```

- Case (II)
  - Logic 0
  - Logic 1

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepwr0= 166.1014n  from=  10.0000p     to=   4.0000n
```

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepwr1= 166.1014n  from=  10.0000p     to=   4.0000n
```

	Logic 0	Logic 1
Case (I): 10ns	123.2915 nW	166.1014 nW
Case (II): 2ns	166.1014 nW	166.1014 nW

由 hspice 的模擬可以發現，logic 1 在兩個 case 中的 leakage power 是相同的，而在 logic 0 的情況並不相同。