

Digital Integrated Circuits

#Homework 3 2023.03.24 (Due: 03.31, 13:20)

/* Using 7 nm CMOS FiFFT devices with VDD= 0.75 V, FF process corner and medium Vt CMOS process*/

/*Rise time and fall time of input signals and clock are 0.02ns (0V-0.75V)*/

1. MOS and Inverter (30%)
 - a) Run SPICE to draw the I-V DC curves (like the one in **Fig.2.7 of page A2-2 with Vgs of 0.75, 0.55, 0.35**) for PMOS and NMOS with Fin n=1. **In table form**, mark Ids_max (Vgs=Vds= Vdd). Discuss the results.
 - b) Keep a unit size inverter with NMOS n=1 and choose the n of PMOS for n=1 and 2 to show the logic threshold voltage. Run SPICE to verify your results by showing simulated waveforms.
2. Ring oscillator (20%)

According to the results of 1(b), design a 3-stage inverter-based ring oscillator with unit size inverter with better logic threshold voltage. Set the initial voltage of each node so that it can oscillate. **Show in table form**, the SPICE simulation results of oscillation frequency and power consumption.
3. (50%) Design a dynamic D register as shown in Fig.1 with propose size of NMOS and PMOS to have better tsetup, tpcq, tpdq and thold time. Both D and CLK has rise time and fall time of 0.1ns (0V-0.75V).
 - a) Explain your sizing principle of each MOS to have least tsetup, tpcq, tpdq and thold time for register 1 and 0.
 - b) Run SPICE to verify your results and list the results in table form for part (b).

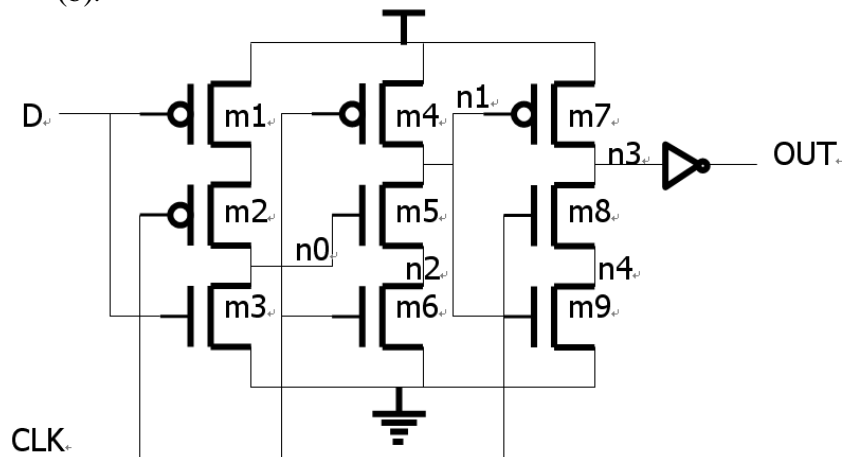


Fig.1