Digital Integrated Circuits

#Homework 1 2023.02.24 (Due:03.08 15:30; in the class)

/* Using 32 nm CMOS devices with VDD= 0.9 V, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, medium Vt and low Vt CMOS*/

(1) Inverter (40%)

a) Keep L equal Lmin, design the W of each device (**in table form**) using medium Vt and high Vt (two cases) such that the logic threshold of the inverter is at 0.5 VDD. Discuss your design procedures and the way you choose your MOS dimension.

b) Run SPICE to verify your results.

(2) Design a CMOS Schmitt trigger shown at Fig.1 using medium Vt such that Vout=0.5 VDD when V^+ = 0.46-0.49 VDD, V^- = 0.44~0.41 and both rising and falling △V are the same. Using medium Vt in your design(60%)

a) Give the W/L of each device and V^+ , V^- (**in table form**) of Fig.1. Discuss your design procedures to determine the size of each transistor. (40%)

b) Run SPICE to verify your results. Your report must have the figures of VTC and Isc (current from Vdd to GND) vs Vin (20%)

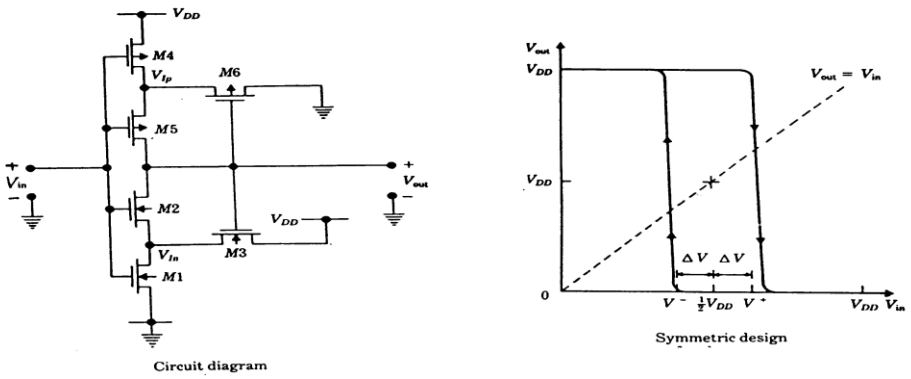

Fig.1 Schmitt Trigger circuit