Digital Integrated Circuits

#Home Work 6 2023.05.5 (Due:05.12 13:20)

Reference to the class note: B4 SRAM and Shifter

1. An embedded SRAM contains 512 words with 32-bit/word.

(a) Plan A: Draw the memory array architecture like that shown in Fig.12.2(a) of class note page 2. **Mark necearry inputs, outputs and signals** (20%)
(b) Plan B: If it is physically arranged in a square fashion like that shown in Fig.12.2 (b) with proper k address bits used in the column decoder, draw the memory architecture and block diagram. Indicate the number of inputs to each column multiplexer. **Mark necearry inputs, outputs and signals (20%)**
(c) **List in table form** for Design A and B of the following items: (10%)
    (i) The number of Worldline and the the number of memory cell in a Wordline,
    (ii) The number of Bitline and the the number of memory cell in a Bitline
(c) Which Plan is better? Compare from **Area** (the row /column decoder size), **Speed** (Worldline and Bitline loading) and **Power** point of view. You shall describe the factors and facts (30%)
(d) Propose using hierarchical bitlines to improve the performance. You shall **describe the circuits** and explain the factor and facts about **area, power and delay time**. (20%)

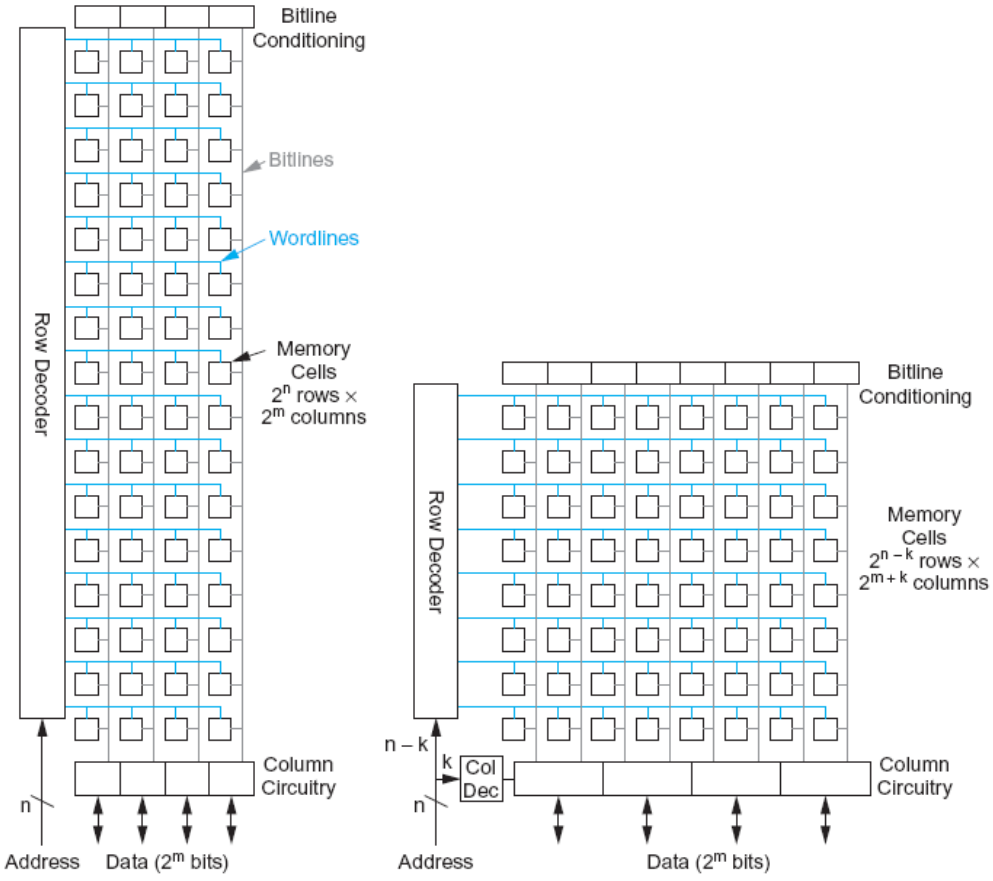

Fig.12.2 (a) and (b)