2023 Spring NYCU-EE Digital Integrated Circuits – Homework4

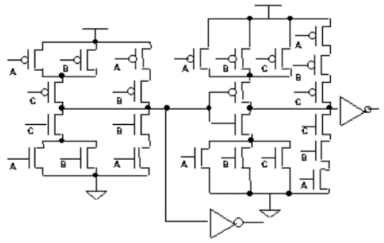
IEE 陳冠瑋 310510221 / Apr. 24, 2023

/* Using 32 nm CMOS devices with VDD= 1.0 V, Wmin=64 nm, Lmin=32nm; using standard Vt CMOS */

/* Rise time and fall time of input signals are 0.04ns */

/* Do not forget to include reasonable AD, AS, PD and PS in your simulation */

1. A 4-bit ripple adder is designed with a Fully Complementary Static Logic Gate for FA as shown in Fig.1 . Input signals are A[3:0], B[3:0], and Cin which are provided by a unit size inverter (PMOS is sized to be 2 times of the minimum sized NMOS) and outputs are Sum[3:0] with the loading of 4 unit size inverters connected in parallelism (FO4). You shall provide SPICE simulation results of timing and power waveforms.



(1) Try your best to design the fastest adder at VDD=1.0V. First, show your block diagrams in terms of the 1-bit Full-Adder(FA). Second, show the circuit schematic of each block. Use logic effort concepts (you do not have to write down the procedure) to design transistor widths. Describe your design concept. (40%)

Ans:

參考講義 B2 p2-2, 2-3，使用 4 個 full adder bar 來組成 4-bit ripple adder。此架構的 ripple adder 可以有比較短的 critical path，因為 critical path 上的 inverter 都被拿掉，所以能比原本 4 個 full adder 所組成的 ripple adder 還來的快。

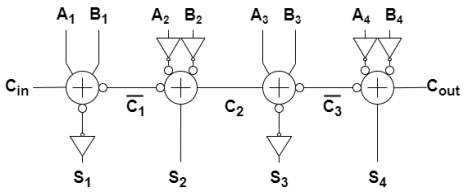


Fig 1. 4-bit carry-ripple adder

Block diagram of the 1-bit $\overline{FA}$

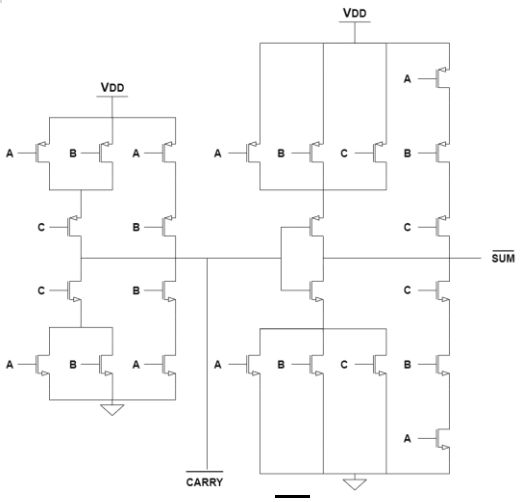


Fig 2. 1-bit $\overline{FA}$ schematic

Circuit schematic of each block

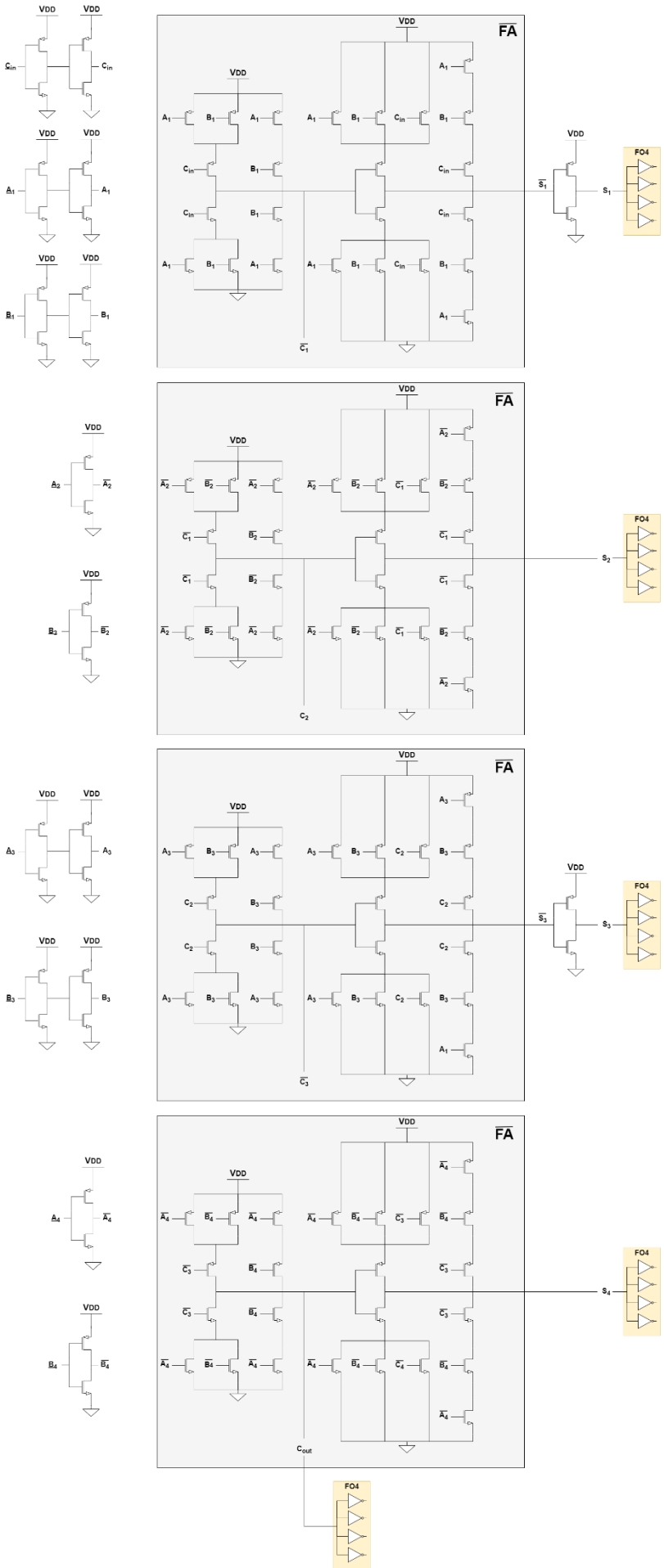


Fig 3. 4-bit ripple adder schematic

Design concept

Logic effort computation:

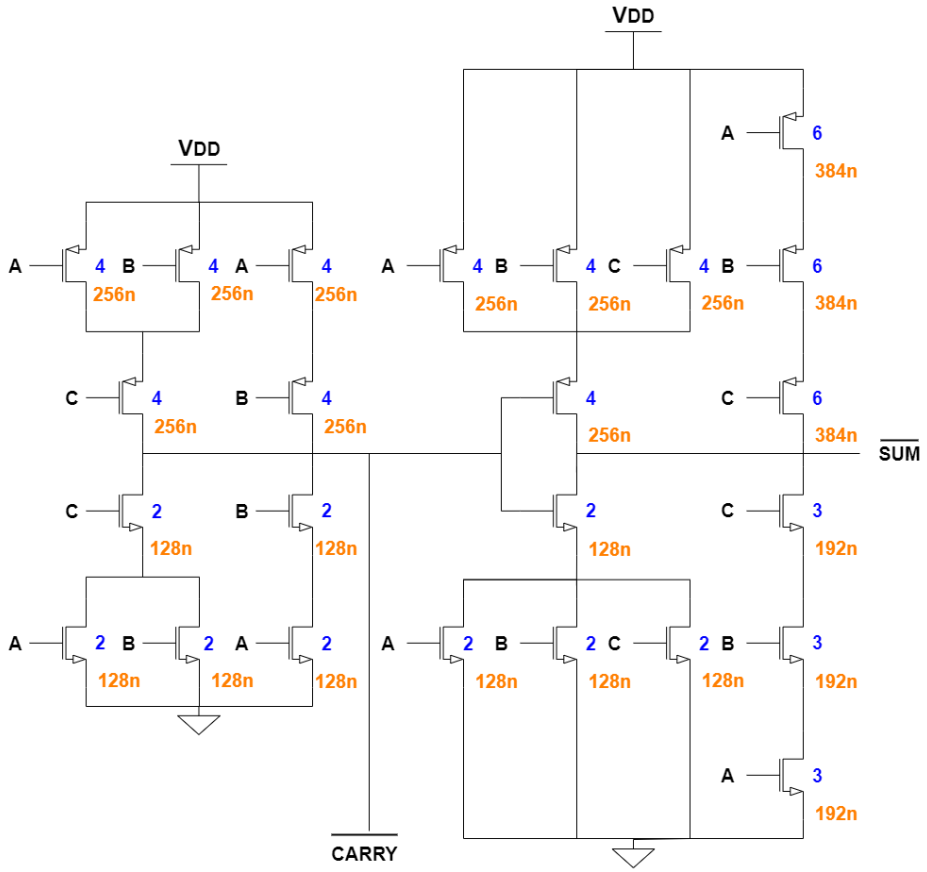


Fig 4. Use logic effort concept to design transistor width

$$g_A = \frac{12}{3} = 4, g_B = \frac{12}{3} = 4, g_C = \frac{6}{3} = 2$$

$$g_{avg} = \frac{4+4+2}{3} = \frac{10}{3}$$

$$g_A = \frac{15}{3} = 5, g_B = \frac{15}{3} = 5, g_C = \frac{15}{3} = 5$$

$$g_{avg} = \frac{5+5+5}{3} = 5$$

$$G = 1 \times 4 \times 2^4 = 64$$

$$B = 1 \times (\frac{6+6}{6})^3 \times 1 = 8$$

$$H = \frac{4}{1} = 4$$

$$F = GBH = 64 \times 8 \times 4 = 2048$$

$$f = (2048)^{\frac{1}{6}} = 3.5636$$

	g	Loading	Size	wp/wn
Stage1	1	16.3	5.43	wp = 128n, wn = 64n (default)
Stage2	4 (ga/gb)	8.56+6	16.3	wp = 690n, wn = 345n
Stage3	2 (gc)	9.26+6	8.56	wp = 366n, wn = 183n
Stage4	2 (gc)	10.5+6	9.26	wp = 394n, wn = 197n
Stage5	2 (gc)	6.735+12	10.5	wp = 448n, wn = 224n
Stage6	2 (gc)	12	6.735	wp1 = 280n, wn1 = 140n, wp2 = 430n, wn2 = 215n

(2) Based on the design of (1), run SPICE to find the propagation delay time (with the pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin). Determine the minimum propagation of a clock with the delay time estimated by SPICE for VDD=1.0 V. (20%)

Ans:

Pattern: 000011110 →000011111

Propagation delay time 是 C_{in} 從 0→1 (50%)到 S_4 從 1→0 (50%)的時間。其中，在本次模擬中 C_{in} 前面有接兩級的 inverter 作為 buffer 來滿足題目 spec 所要求，可以更貼近實際電路所遇到的 input 情況。另外，S1~S4 與 C_{out} 都分別接了一個 FO4 作為負載，以滿足題目的描述，透過 Measure Tool 量測可以得到 propagation delay 為 74.5 ps。

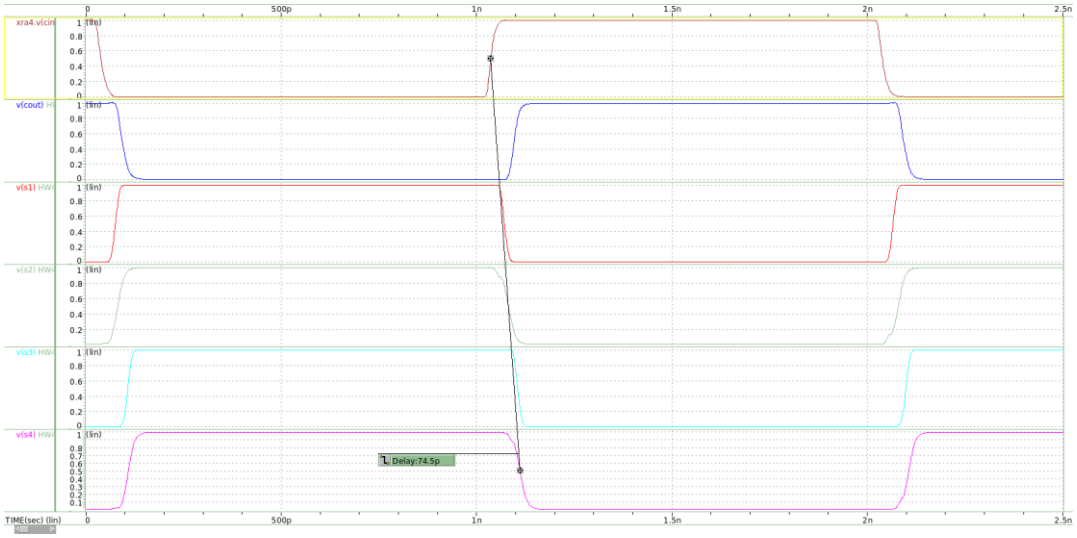


Fig 5. Propagation delay time

Propagation delay = 74.5 ps

$$\text{Max frequency} \approx \frac{1}{\text{propoagation delay}} = \frac{1}{74.5\ ps} = 13.4\ \text{GHz}$$

(3) Run SPICE for VDD=1.0V to get the average, peak, and leakage power dissipation and energy/bit, respectively of this adder with loading (FO4) when working at the maximum working frequency. (20%)

Ans:

Average and peak power	Leakage power
A[3:0] is from 0000 to 1111	A[3:0] is 0000
B[3:0] is from 1111 to 0000	B[3:0] is 1111
Cin is 0/1 by turns	Cin is 0

/*You should provide the SPICE input description, timing and power waveforms*/

Pattern: 000011110 → 111100001

Period = 2ns 時，propagation delay = 75ps

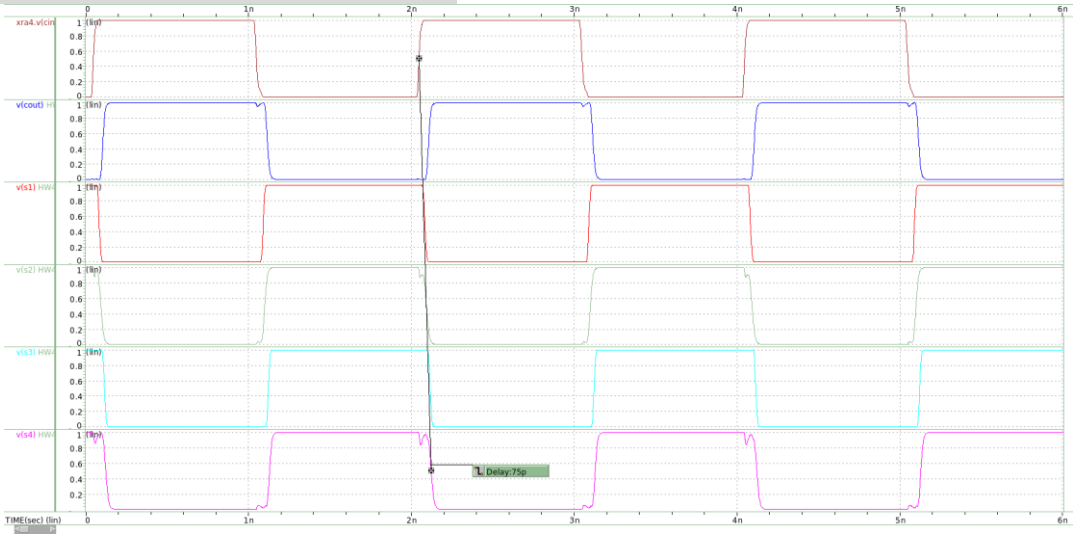


Fig 6. Propagation delay time (period = 2ns)

推估理想上的 maximum frequency 可以到 13.3 Ghz。但題目設定的 input signal 的 rise/fall time 為 0.04ns，在方波佔了很大的比例。所以實際上的 period 會比 75ps 還要大，經過 trial and error 測出來的結果大約為 250ps。

Period = 250ps 時，propagation delay = 80.7ps

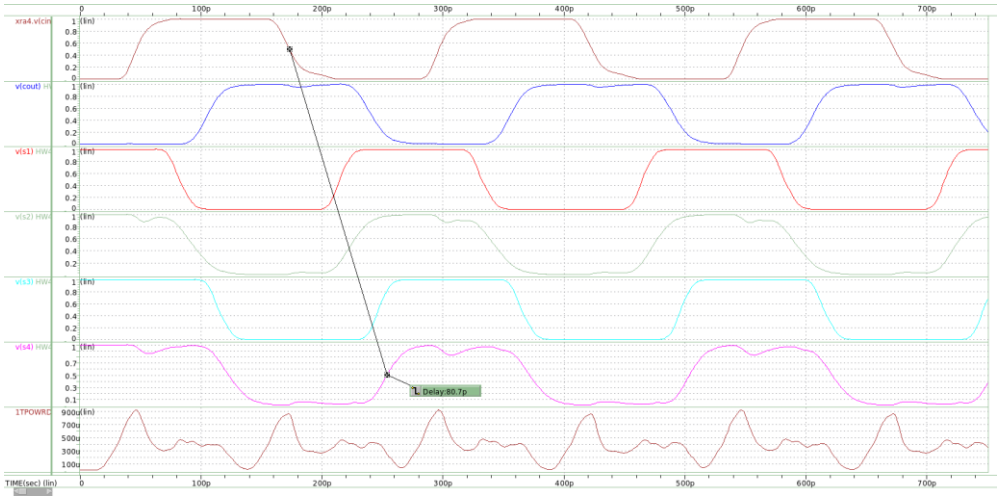


Fig 7. Propagation delay time (period = 250ps)

Maximum frequency ≈ 4 GHz

在 4 GHz frequency 下的 average, peak, and leakage power dissipation and energy/bit 如下：

Pattern: 000011110 → 111100001

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
avgpower= 382.4053u  from=   0.            to= 750.0000p
peakpower= 924.7756u    at= 296.4077p
           from=   0.           to= 750.0000p

         ***** job concluded
```

- Average power = 382.4053 uW
- Peak power = 924.7756 Uw
- Energy / bit = (avg_power * sim_time) / bit = (382.4053uW * 750ps) / 9 = 31.9fJ

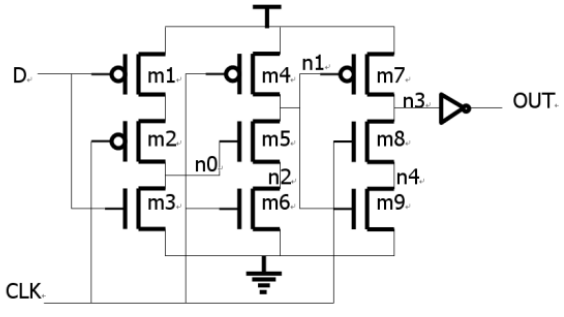
Pattern: 000011110

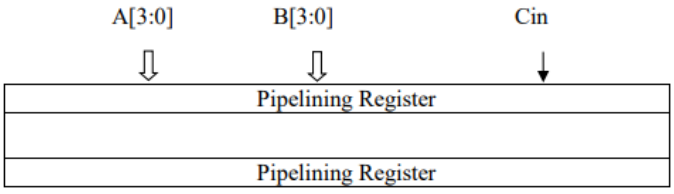
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepower=   4.0709u  from=   0.            to= 750.0000p

         ***** job concluded
```

- Leakage power = 4.0709 uW

(4) Add one pipelining stage using the designed D register into the 4-bit ripple adder as shown in Fig.1(b). Run SPICE to find the propagation delay time (with the pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin) between pipelining stages to determine the maximum working frequency of the clock with the delay time estimated by SPICE for VDD=1.0 V. (20%)





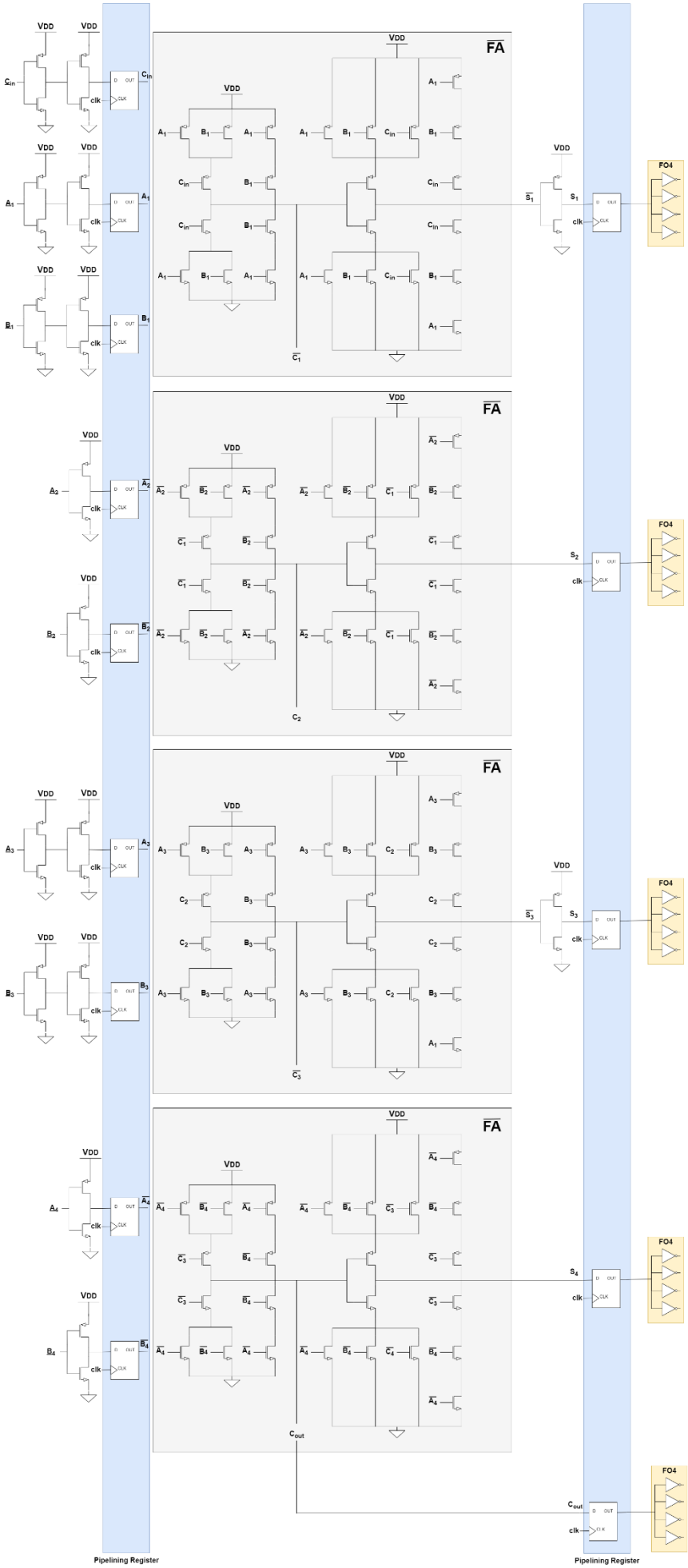


Fig 8. 2-stage pipelining 4-bit ripple adder schematic

先以 clock period = 2ns 並用 spice 來模擬 2-stage pipeline 的 4-bit ripple adder 的功能是否正確。

1. 模擬一開始值不符合預期的可能的原因是 DFF 並未 reset。

2. A_1~A_4, B_1~B_4 與 C_{in} 在 posedge 觸發存入第一級 DFF，並經過 4-bit ripple adder 計算出對應的 S_1~S_4 與 C_{out}。

3. 下一個 posedge 時，Input 維持不變，S_1~S_4 與 C_{out} 存入第二級 DFF，得到最終的 Output。

Fig 9. 2-stage pipelining 4-bit ripple adder spice simulation (period = 2ns)

Propagation delay time 會是 C_{in}_ff 到 C_{out} 或 C_{in}_ff 到 S_4 的 delay，看誰比較久就是 Propagation delay。

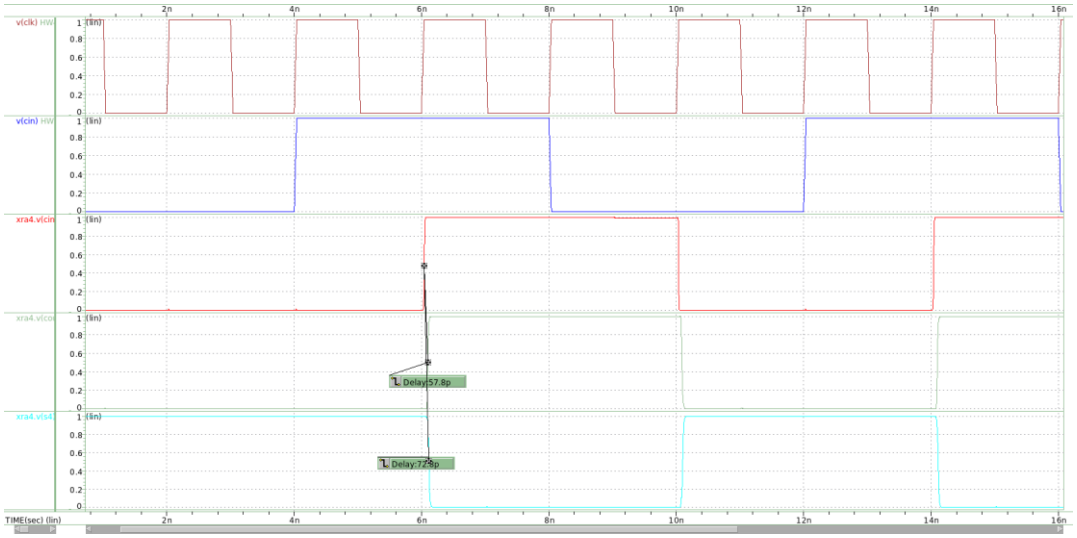


Fig 10. 2-stage pipelining 4-bit ripple adder propagation delay

Propagation delay = 72.8ps。

Max frequency $\approx \frac{1}{\text{propoagation delay}} = \frac{1}{72.8\ ps} =$ 13.7 GHz

推估理想上的 maximum frequency 可以到 13.7Ghz。但因為 input signal 的 rise/fall time 在方波佔了很大的比例。所以經過 trial and error 測出來的結果大約為 150ps。Maximum working frequency 大約落在 6.7GHz。

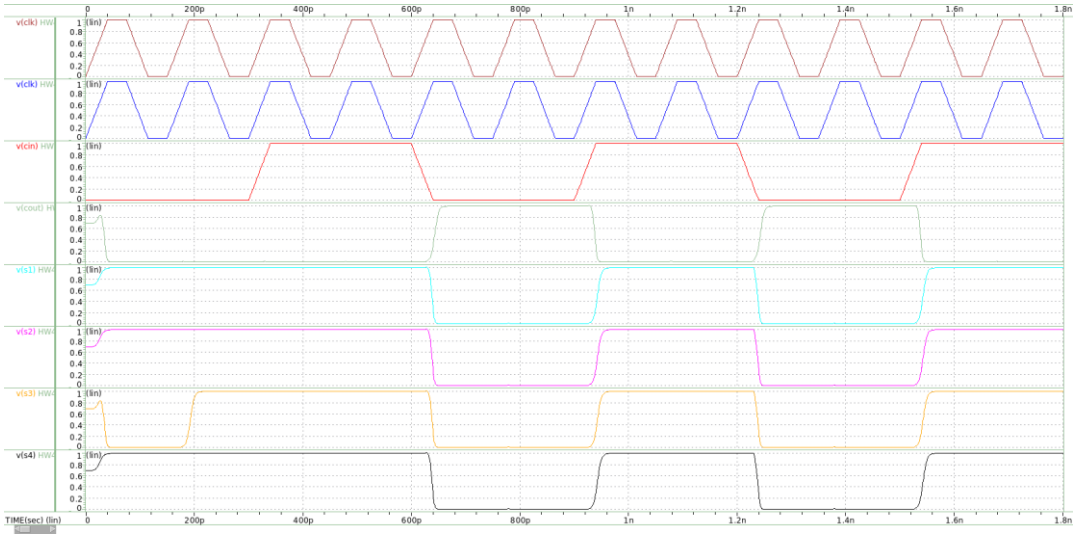


Fig 10. 2-stage pipelining 4-bit ripple adder propagation delay