2023 Spring NYCU-EE Digital Integrated Circuits – Homework5

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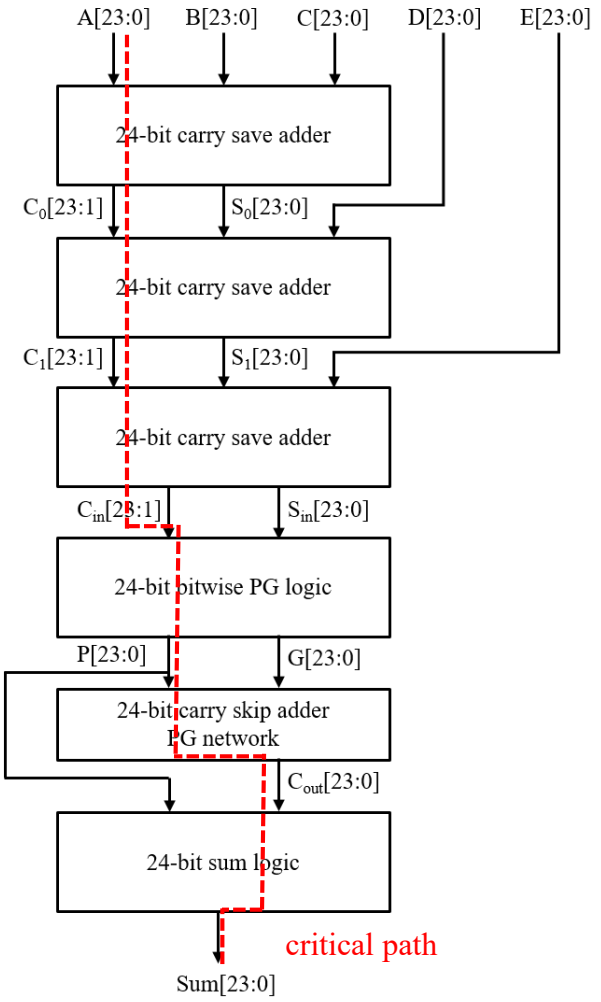
1.

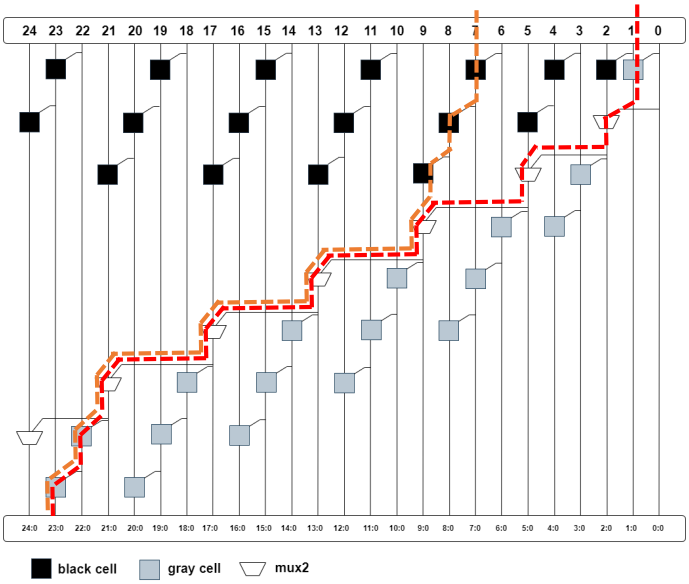
(a)

Block Diagram



Design Concept

1 個 24-bit Carry Save Adder (CSA) 可以讓 3 個數相加，並輸出兩個數 C 和 S。題目總共有 5 個數要相加，分別為 A~E，所以設計 3 層的 CSA 來完成。經過 3 層的 CSA，會得到 2 個數，再用 Carry skip adder 將這兩個數相加，就可以得到最後的 Sum。



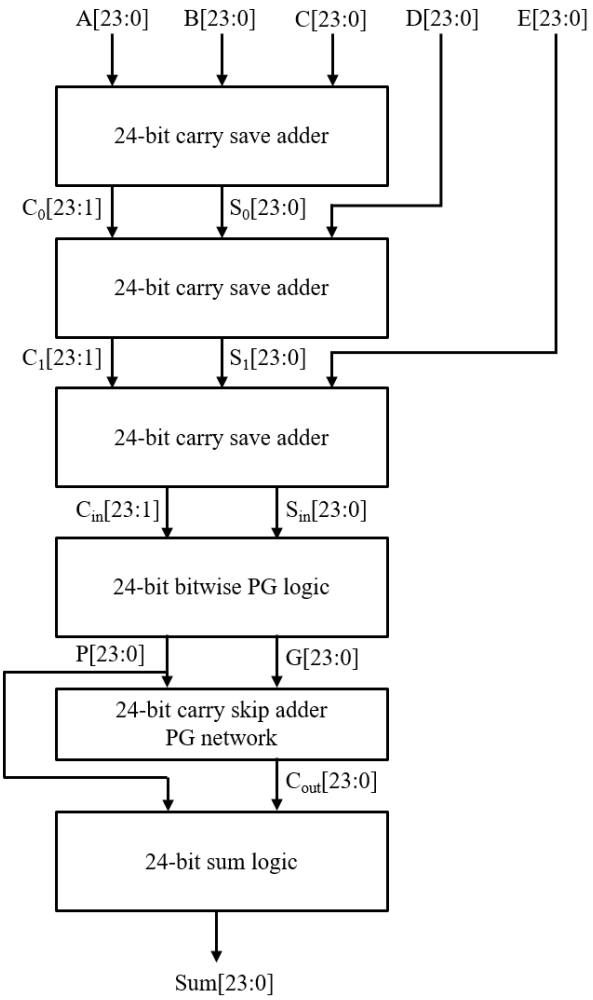
(1) If $t_{mux2} > t_{valency-2}$:

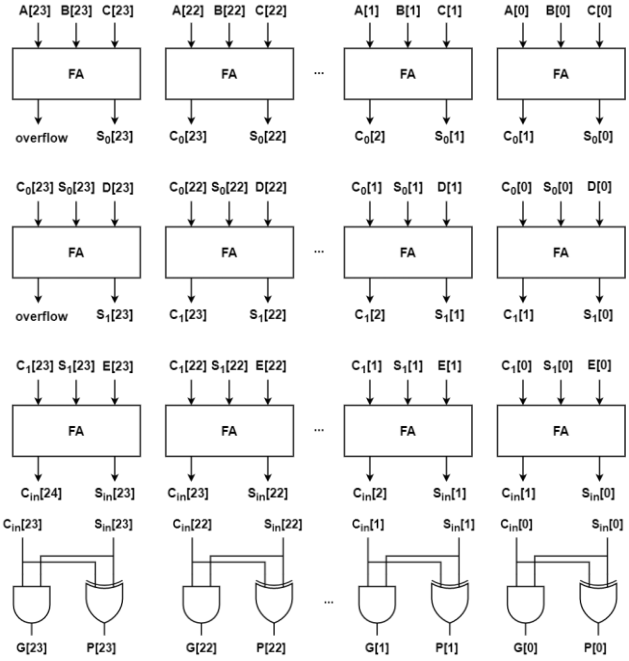
$T_{delay} = 3*t_{1\text{-bit FA}} + t_{1\text{-bit PG}} + 3*t_{valency-2} + 6*t_{mux2} + t_{xor2}$

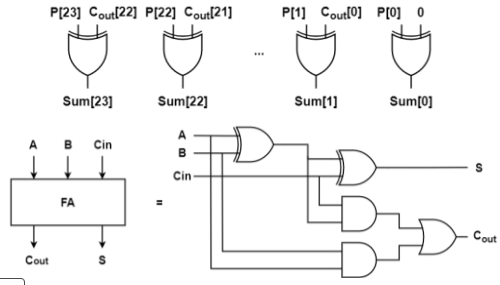
(2) If $t_{mux2} < t_{valency-2}$:

$T_{delay} = 3*t_{1\text{-bit FA}} + t_{1\text{-bit PG}} + 5*t_{valency-2} + 4*t_{mux2} + t_{xor2}$

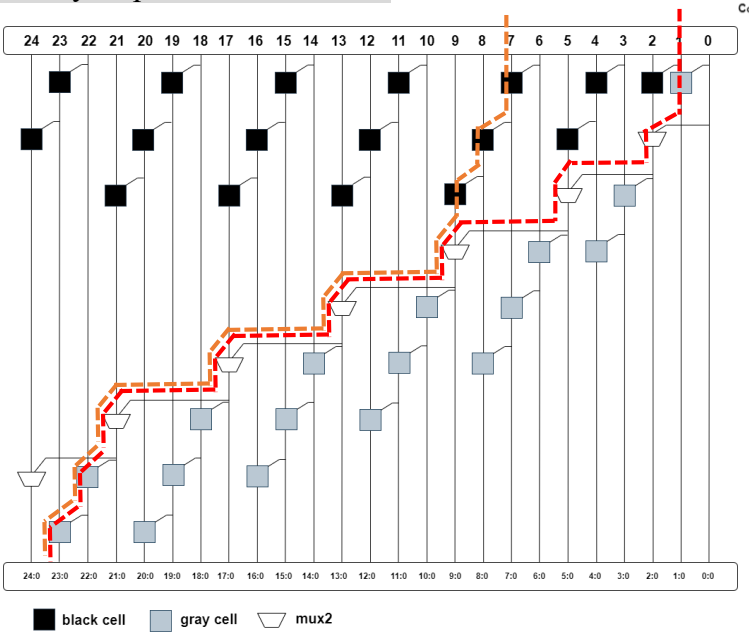
(b)

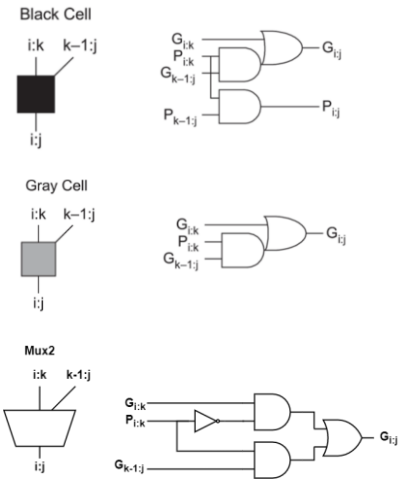






24-bit carry skip adder PG network





Design Concept

Carry skip adder 在 critical path 上第一個 group 和最後一個 group 是以 ripple 的方式傳遞過去的。所以縮短第一個 group 與最後一個 group 可以降低 delay time。而中間的 group 越長，可以讓 skip 數變多，使 group 的數量變少，delay 也會變少。但如果 group 之間一次增加超過 1 bit，會使真正的 carry in 到達時 P 還來不及產生，反而使 delay 變大。

最後的 PG network 設計成[2, 3, 4, 4, 4, 4, 3]，共 7 個 group 來達到最小 delay。

(c) Critical path delay

假設每個 gate delay 的時間相差不大，下表以單位 gate delay 來計算。

module	Case1: $T_{mux2} > T_{valency\text{-}2\ cell}$	Case2: $T_{valency\text{-}2\ cell} > T_{mux2}$
1-bit FA	3*3 = 9 gate delay	3*3 = 9 gate delay
1-bit PG	1*1 = 1 gate delay	1*1 = 1 gate delay
Mux2	6 * 2 = 12 gate delay	4 * 2 = 8 gate delay
Valency-2	3 * 2 = 6 gate delay	5 * 2 = 10 gate delay
XOR2	1*1 = 1 gate delay	1*1 = 1 gate delay
Total	29 gate delay	29 gate delay

(d) Overall module

module	number
1-bit FA	24 * 3 = 72
1-bit PG	24
Mux2	7
Valency-2	34
XOR2	24

2.

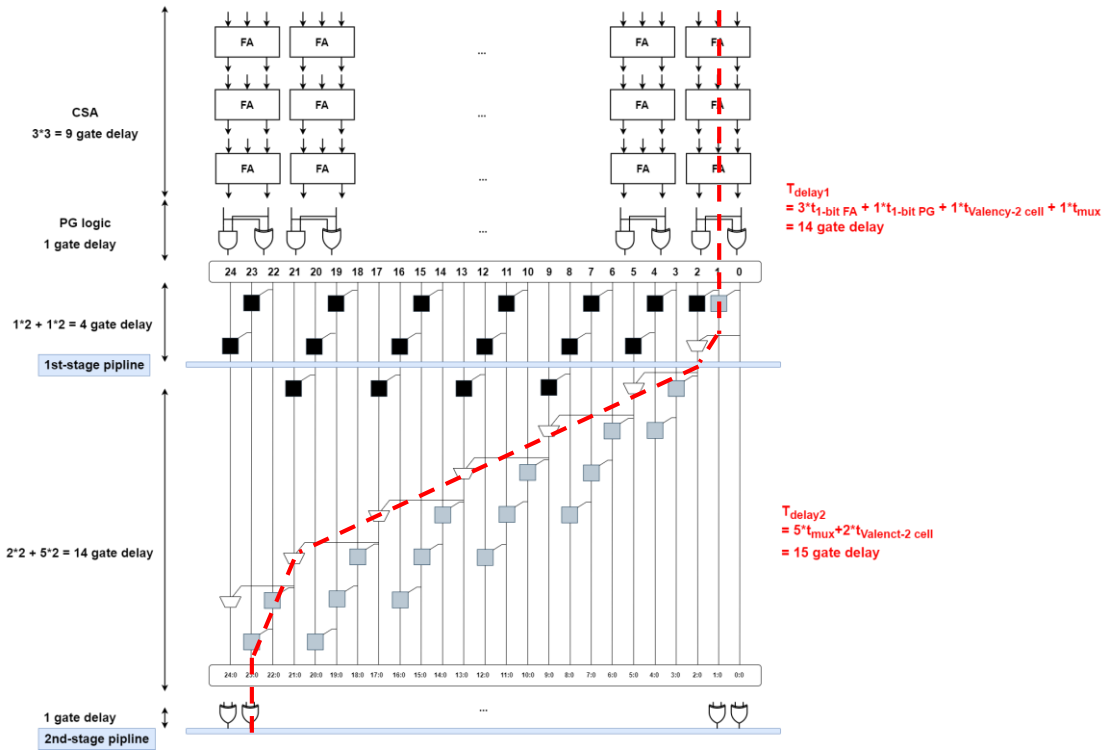
(a)

假設每個 gate delay 的時間差異不大，並假設 $t_{mux2} > t_{valency\text{-}2}$，根據上一題的設計 critical path 總共為 29 個 gate delay。為了使 pipeline 的效益最大化，並最小化 delay time，若要切兩級 pipeline 最好的情況是可以將 critical path 的 delay time 平均分攤(14+15 or 15+14)。所以，我選擇將 1st-stage pipeline 切在 carry skip adder 第二級與第三級的位置，2nd-stage pipeline 切在 XOR 之後 output 的位置。

如此一來:

$$T_{delay1} = 3 * t_{1-bit\ FA} + 1 * t_{1-bit\ PG} + 1 * t_{Valency-2\ cell} + 1 * t_{mux} = 14\ \ gate\ \ delay\ \ (1st - stage)$$

$$T_{delay2} = 5 * t_{mux} + 2 * t_{Valency-2\ cell} = 15\ \ gate\ \ delay\ \ (2nd - stage)$$



critical path

(b)

	Number of DFF
1st-stage pipeline	**24** (bitwise P) + **24** ($G_{x:0}$) + **6** (P) = **54**
2nd-stage pipeline	**24** ([23:0]Sum)
Total	**78**

- 1st-stage pipeline
  24 個 bitwise P、24 個 $G_{x:0}$、6 個 P ($P_{23:22}$, $P_{20:19}$, $P_{16:15}$, $P_{12:11}$, $P_{8:7}$, $P_{5:4}$)
- 2^{nd}-stage pipeline
  24 個 Sum

(c)

$T_C \geq t_{pd} + (t_{setup} + t_{pcq})$

Case1: $T_{mux2} > T_{Valency\text{-}2\ cell}$

$$\begin{cases} T_C \geq 3T_{FA} + T_{PG} + T_{valency-2\ cell} + T_{mux2} + t_{setup} + t_{pcq} \\ T_C \geq 5T_{mux2} + 2T_{valency-2\ cell} + T_{XOR2} + t_{setup} + t_{pcq} \end{cases}$$

Case2: $T_{Valency\text{-}2\ cell} > T_{mux2}$

$$\begin{cases} T_C \geq 3T_{FA} + T_{PG} + 2T_{valency-2\ cell} + t_{setup} + t_{pcq} \\ T_C \geq 5T_{mux} + 2T_{valency-2\ cell} + T_{XOR2} + t_{setup} + t_{pcq} \end{cases}$$