Digital Integrated Circuits

#Home work 2 2023.03.08 (Due:03.15, 15:30)

/* Using 32 nm CMOS devices with VDD= 0.9 V, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, medium Vt and low Vt CMOS*/

1. (50%) Draw the layout (in a standard cell layout style like the NAND3) of the schmitt trigger that you design at HW1 using the design rules of table 3.3 with a scale factor of 32/65 for 32nm case for all rules. Use the style as shown in Fig.1.39 to show each layer. You should include substrate contact in your layout. List the square area (? um by ? um) of your rectangular cell. Also, in your layout, mark at least five rules as that shown in Fig.3.19. (Do your best to have a compact layout and list the X and Y size. The size of the area will not affect your score)

2. Do the power and timing analysis of the schmitt trigger which has two fanouts of the same Schmitt trigger.

(i) (10%)Run SPICE to get the input and output capacitance of the Schmitt trigger when input and output are in 0/1 and 1/0 respectively (Be careful to indicate the Ad, AS, PD, PS)

(ii) With inputs like a triangular waveforms with duration of (I) 10ns and (II) 2ns (T0) respectively, run spice to get the timing waveform like that shown in the following figure:

(a)(10%)List the V+ and V- and tdf and tdr of the first stage schmitt trigger for case (I) and (II), Discuss the difference of these V+ /V- with that of HW 1.

(b)(20%)Get the power waveform and the average power dissipation of the first stage of the schmitt trigger. Compare the average power dissipation with the dynamic power equation. Discussion your observation

(c)(10%)Get the leakage power of schmitter when input is logic 1 and logic zero respectively.

Your report must have the figure of waveform and SPICE input file.

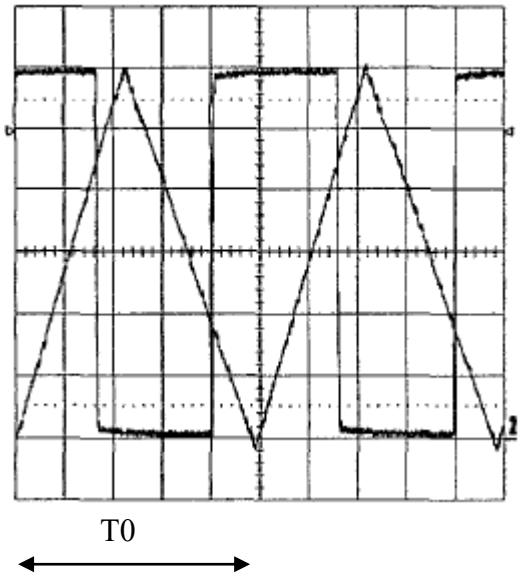

Table 3.1 65 nm CMOS process

Layer	Rule	Description	65 nm Rule (μm)
Well	1.1	Width	0.5
	1.2	Spacing to well at different potential	0.7
	1.3	Spacing to well at same potential	0.7
Active (diffusion)	2.1	Width	0.10
	2.2	Spacing to active	0.12
	2.3	Source/drain surround by well	0.15
	2.4	Substrate/well contact surround by well	0.15
	2.5	Spacing to active of opposite type	0.25
Poly	3.1	Width	0.065
	3.2	Spacing to poly over field oxide	0.10
	3.2a	Spacing to poly over active	0.10
	3.3	Gate extension beyond active	0.10
	3.4	Active extension beyond poly	0.10
	3.5	Spacing of poly to active	0.07
Select	4.1	Spacing from substrate/well contact to gate	0.15
	4.2	Overlap of active	0.12
	4.3	Overlap of substrate/well contact	0.12
	4.4	Spacing to select	0.20
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.08
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.10
	5.4	Spacing to gate	0.07
Metal1	7.1	Width	0.09
	7.2	Spacing to well metal1	0.09
	7.3, 8.3	Overlap of contact or via	0.01
	7.4	Spacing to metal for lines wider than 0.5 μm	0.30
Via1–Via6	8.1, 14.1, …	Width (exact)	0.10
	8.2, 14.2, …	Spacing to via on same layer	0.10
Metal2–Metal7	9.1, …	Width	0.10
	9.2, …	Spacing to same layer metal	0.10
	9.3, …	Overlap of via	0.01
	9.4, …	Spacing to metal for lines wider than 0.5 μm	0.30
Via7–8		Width	0.20
		Spacing	0.20
Metal8–9		Width	0.40
		Spacing to same layer metal	0.40
		Overlap of via	0.10
		Spacing to metal for lines wider than 1.0 μm	0.50

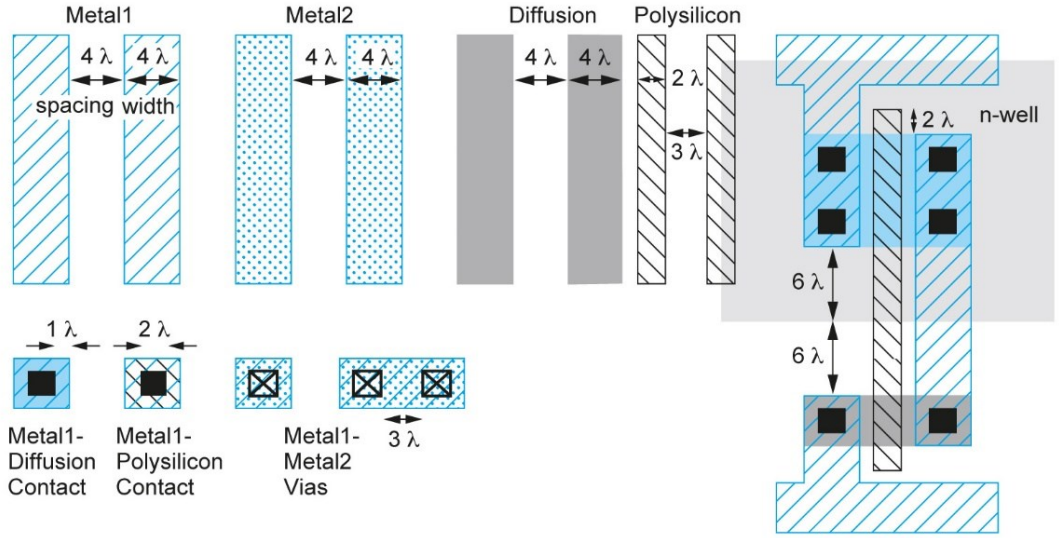

FIGURE 1.39 Simplified λ-based design rules