Digital Integrated Circuits

#Home work 4 2023.04.21(Due: 04.28, 13:20)

/* Using 32 nm CMOS devices with VDD= 1.0 V, Wmin=64 nm, Lmin=32nm; using standard Vt CMOS*/ /*Rise time and fall time of input signals are 0.04ns */
/*Do not forget to include reasonable AD, AS, PD and PS in your simulation*/

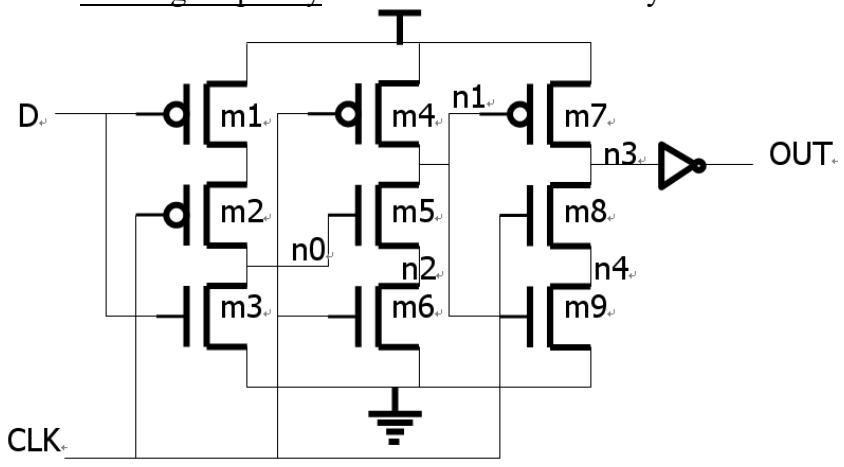
1. A 4-bit ripple adder is designed with Fully Complementary Static Logic Gate for FA as ahown at Fig.1 . Input signals are A[3:0], B[3:0] and Cin which are provided by a unit size inverter (PMOS is sized to be 2 times of the minimum sized NMOS) and outputs are Sum[3:0] with loading of 4 unit size inverters connected in parallelism (FO4). You shall provide SPICE simulation results of timing and power waveforms.

(1) Try your best to design the fastest adder at VDD=1.0V. First, show your block diagrams in terms of the 1-bit Full-Adder(FA). Second, show the circuit schematic of each block. Use logic effort concepts (you do not have to write down the procedure) to design transistor widths. **Describe your design concept.** (40%)

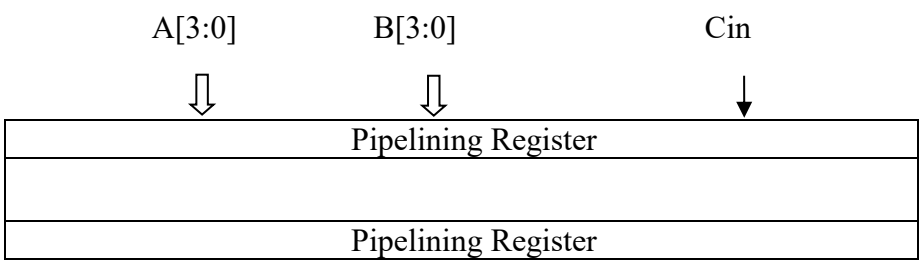
(2) Based on the design of (1), run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin). Determine the maximum propagation of a clock with the delay time estimated by SPICE for VDD=1.0 V. (20%)

(3) Run SPICE for VDD=1.0V to get the average, peak and leakage power dissipation and energy/bit, respectively of this adder with loading (FO4) when working at the maximum working frequency. (20%)

(4) Add one pipelining stage using the designed D register into the 4-bit ripple adder as shown at Fig.1(b). Run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin) between pipelining stages to determine the maximum working frequency of the clock with the delay time estimated by SPICE for VDD=1.0 V. (20%)



(a)



(b)

Fig.1 (a) TSPC register (b) pipeline design of 4 bit adder.

(When running SPICE simulation in (3), use the follwing input patterns)

Average and peak power	Leakage power
A[3:0] is from 0000 to 1111	A[3:0] is 0000
B[3:0] is from 1111 to 0000	B[3:0] is 1111
Cin is 0/1 by turns	Cin is 0

/*You should provide the SPICE input description, timing and power waveforms*/