2023 Spring NYCU-EE Digital Integrated Circuits – Homework3

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/* Using 7 nm CMOS FinFET devices with VDD= 0.75 V, FF process corner and medium Vt CMOS process*/
/* Rise time and fall time of input signals and clock are 0.02ns (0V-0.75V) */

1. MOS and Inverter (30%)
   a) Run SPICE to draw the I-V DC curves (like the one in **Fig.2.7 of page A2- 2 with Vgs of 0.75, 0.55, 0.35**) for PMOS and NMOS with Fin n=1. **In table form**, mark Ids_max (Vgs=Vds= Vdd). Discuss the results.
   b) Keep a unit size inverter with NMOS n=1and choose the n of PMOS for n=1 and 2 to show the logic threshold voltage. Run SPICE to verify your results by showing simulated waveforms.

Ans:

a)

(1) I-V DC curves

PMOS:

```
.dc vdsp 0 -0.75 -0.01   sweep vgsp -0.35 -0.75 -0.2
```

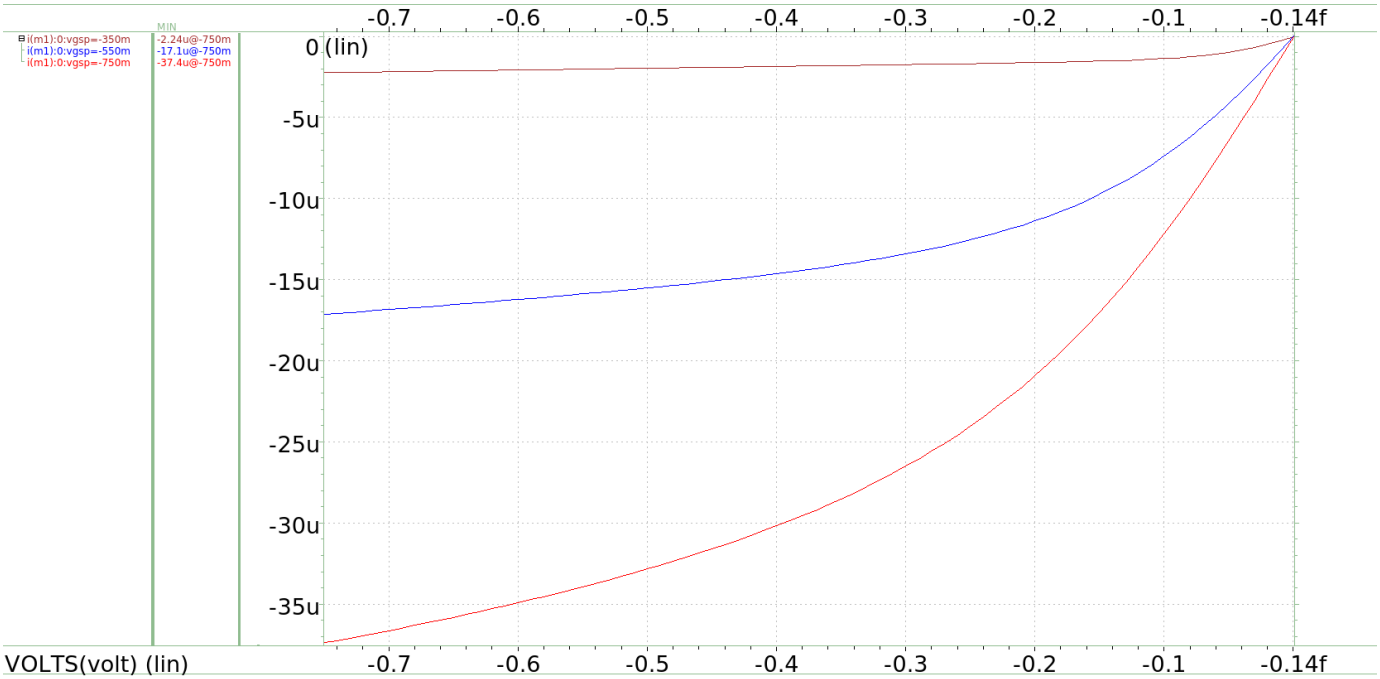

Fig1. PMOS I-V DC curves with |Vgs| of 0.75, 0.55, 0.35

NMOS:

```
.dc vdsn 0  0.75  0.01   sweep vgsn 0.35 0.75 0.2
```

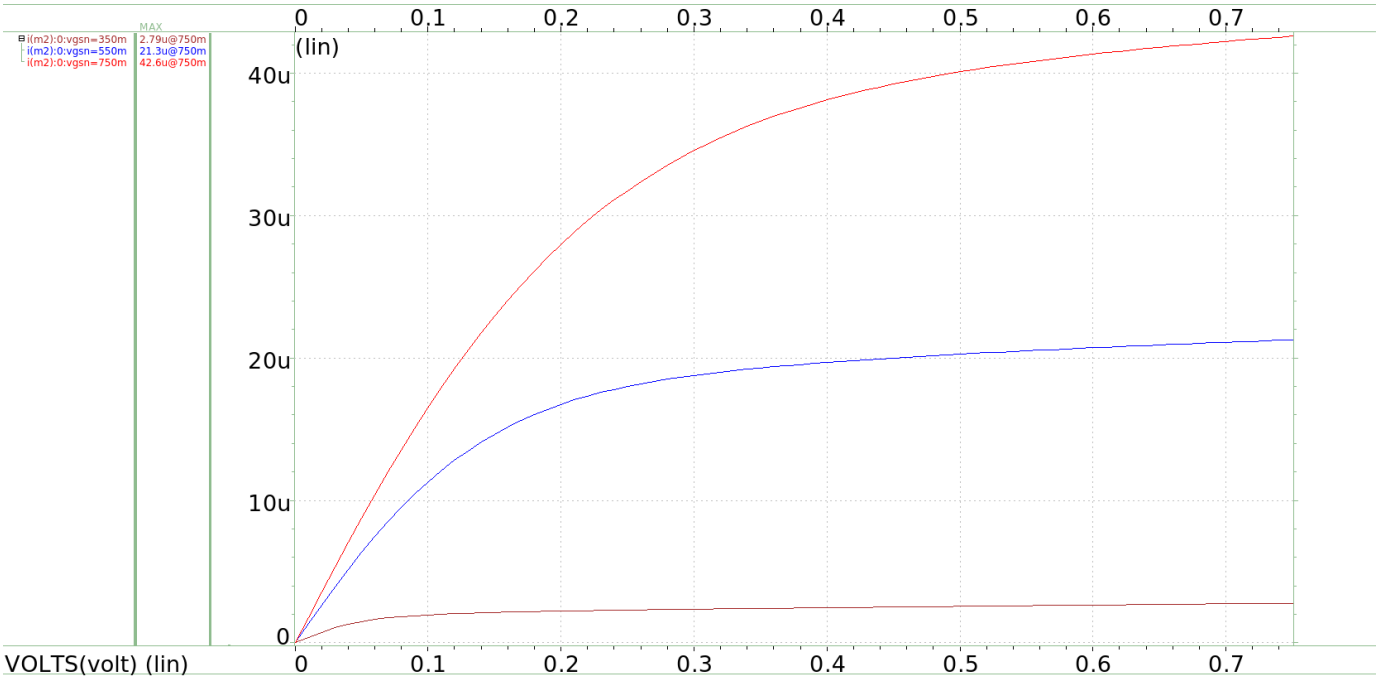

Fig2. NMOS I-V DC curves with Vgs of 0.75, 0.55, 0.35

(2) Ids_max in table form

	Ids_max (μA)		
	$\|V_{gs}\| = 0.75\ V$	$\|V_{gs}\| = 0.55\ V$	$\|V_{gs}\| = 0.35\ V$
PMOS	-37.4	-17.1	-2.24
NMOS	42.6	21.3	2.79

Table1. Ids_max ($\|V_{gs}\| = 0.75, 0.55, 0.35\ V$)

(3) Discuss the results

透過模擬結果可以發現，7nm FinFET 製程下 NMOS 的 Ids_max 只比 PMOS 的 Ids_max 大約大了 1.14 ~ 1.25 倍左右。比起傳統 32nm Planar 的製程 NMOS 與 PMOS 的最大電流會差兩倍以上，FinFET 製程的 NMOS 與 PMOS 的 Ids_max 相對接近。在過去 CMOS 的製程中，為了平衡 MOS 的 mobility，wp 會設 wn 的兩倍左右，而在 FinFET 製程，NMOS 與 PMOS 的電流驅動能力差不多，可以猜測 nfin 的大小可以設的差不多。

b)

(1) NMOS n=1 / PMOS n=1

logic threshold voltage = 0.365 V

```
.subckt inverter in out vdd vss
m1 out in vdd vdd pmos_rvt nfin = 1
m2 out in vss vss nmos_rvt nfin = 1
.ends

xinv in out vdd vss inverter
```

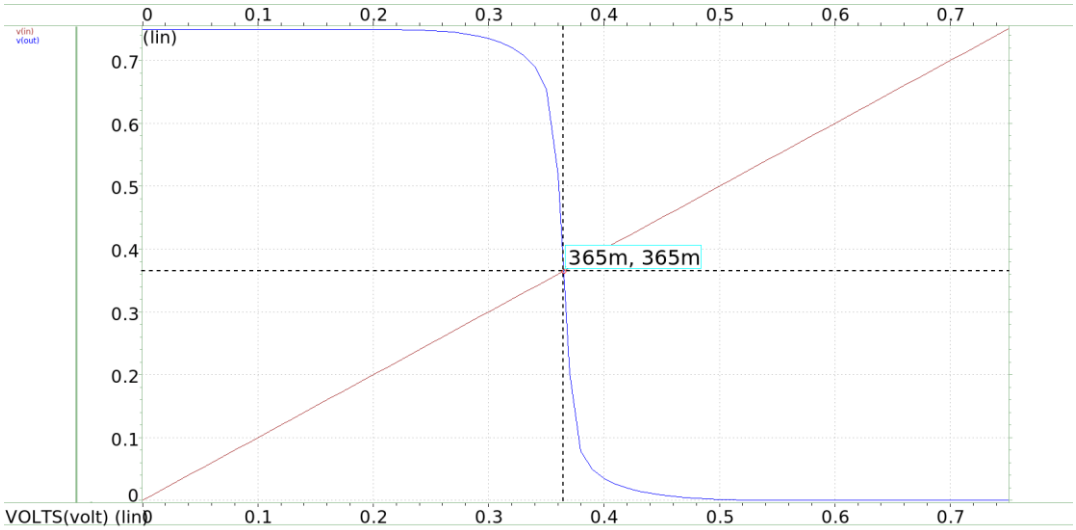

Fig3. 7nm FinFET inverter with NMOS n=1 and PMOS n=1

(2) NMOS n=1 / PMOS n=2

logic threshold voltage = 0.386 V

```
.subckt inverter in out vdd vss
m1 out in vdd vdd pmos_rvt nfin = 2
m2 out in vss vss nmos_rvt nfin = 1
.ends

xinv in out vdd vss inverter
```

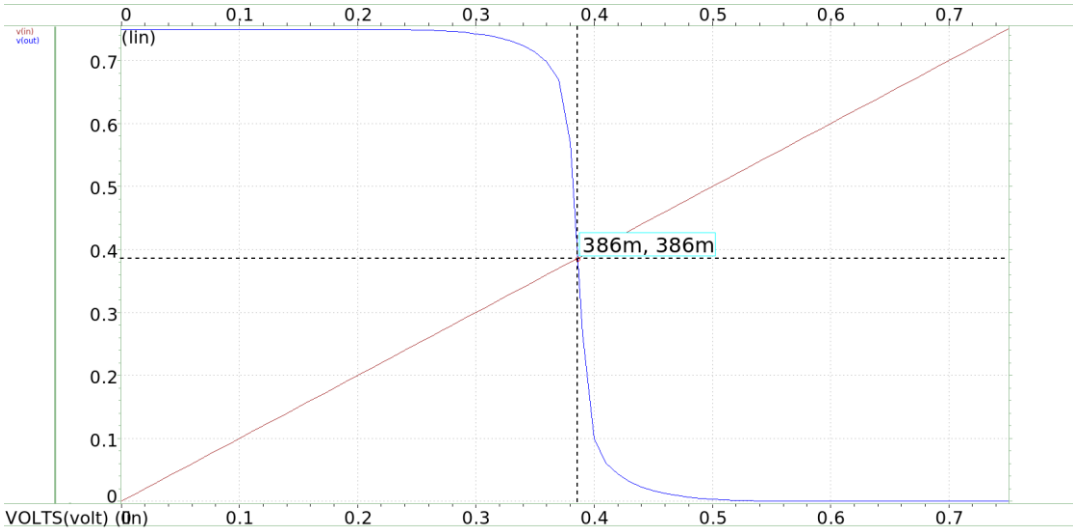

Fig4. 7nm FinFET inverter with NMOS n=1 and PMOS n=2

由模擬結果可以發現，PMOS n = 1 的情況比 PMOS n = 2 的情況，logic threshold voltage 更接近$0.5 * VDD = 0.375$ V，代表 n = 1 能設計出較理想的 inverter，也間接驗證剛剛 a 小題的討論，NMOS 與 PMOS 電流的驅動能力差不多，所以 nfin 可以設差不多。

2. Ring oscillator (20%)

According to the results of 1(b), design a 3-stage inverter-based ring oscillator with unit size inverter with better logic threshold voltage. Set the initial voltage of each node so that it can oscillate. Show in table form, the SPICE simulation results of oscillation frequency and power consumption.

Ans:

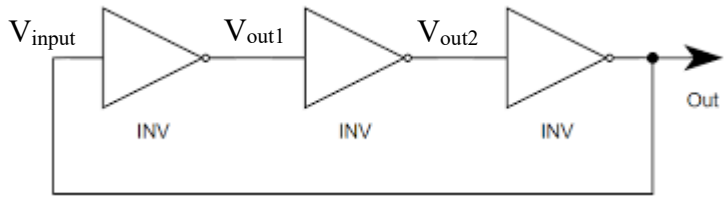

Fig5. 3-stage inverter-based ring oscillator

(1) Unit size inverter with better logic threshold voltage. Set the initial voltage of each node so that it can oscillate.

NMOS n=1 / PMOS n=1, logic threshold voltage = 0.365 V

利用.ic v(input) = 0 設定 V_{input} 的初始電壓，輸入訊號就會通過 3 級的 inverter 並開始震盪，波形結果中可以看到，V_{input} = low→high→low→high→…；V_{out1} = high→low→high→low→…；V_{out2} = low→high→low→high→…。由此可知，設計的 ring oscillator 是有正常在震盪的。

```
*********************************
**     Circuit description     **
*********************************
.subckt inverter in out vdd vss
m1 out in vdd vdd pmos_rvt nfin = 1
m2 out in vss vss nmos_rvt nfin = 1
.ends

xinv1 input out1  vdd vss inverter
xinv2 out1  out2  vdd vss inverter
xinv3 out2  input vdd vss inverter
```

```
*********************************
**     Power declaration       **
*********************************
vvdd        vdd        0     xvdd
vvss        vss        0     xvss

*********************************
**     Analysis setting        **
*********************************
*initial condition
.ic v(input) = 0
```

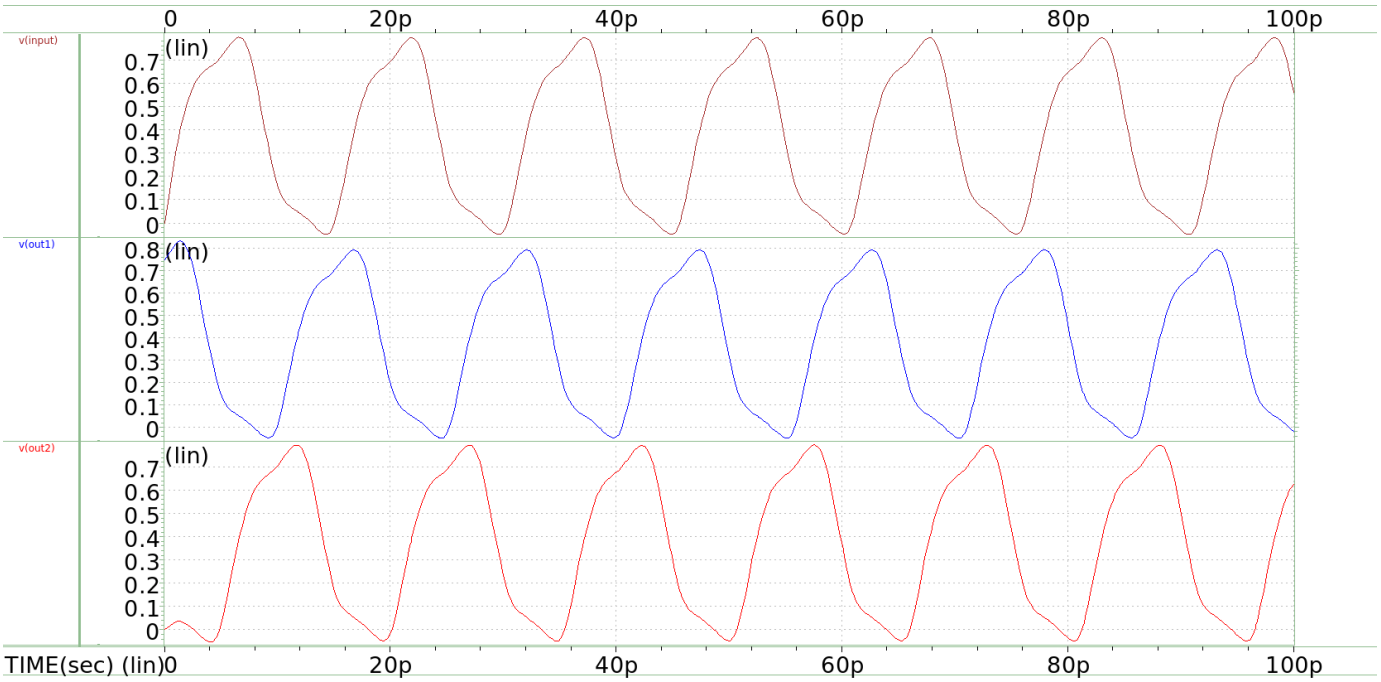

Fig6. ring oscillator 3-node voltage (V_{input} / V_{out1} / V_{out2})

(2) Show the SPICE simulation results of oscillation frequency and power consumption in table form.

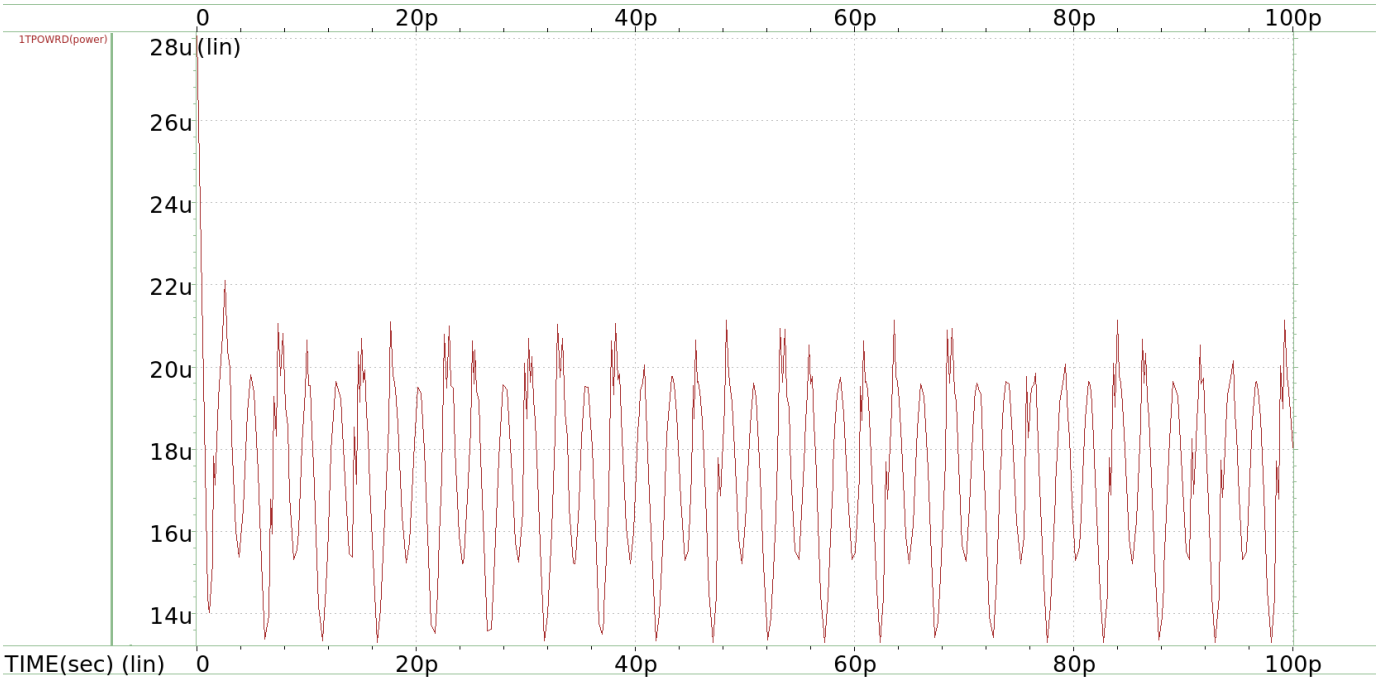

Fig7. Power trace of ring oscillator

```
**********************************
**          Measure             **
**********************************
.meas pavg AVG POWER
.meas pmax MAX POWER
.meas TRAN PERIOD TRIG V(input) VAL=0.386 RISE=1
+                 TARG V(input) VAL=0.386 RISE=2
```

```
pavg=  17.3241u  from=   0.            to= 100.0000p
pmax=  28.0433u    at=   0.
           from=   0.            to= 100.0000p
period=  15.4364p  targ=  16.7833p   trig=   1.3469p
```

利用 .meas pavg AVG POWER, .meas pmax MAX POWER 就可以分別模擬得到此電路的平均功率消耗(P_{avg})與最大功率消耗(P_{max})。

另外，透過

.meas TRAN PERIOD TRIG V(input) VAL=0.386 RISE=1

\+ TRAG V(input) VAL=0.386 RISE=2

可以藉由測量訊號一個週期的時間，藉由到得到電路震盪的週期，即可換算成震盪的頻率。

period = 15.4364 ps

frequency = 1/period = 64.7819 GHz

也可以直接在 HSPICE 中計算 frequency 的大小：

```
.print FREQ = 1/PERIOD
```

```
 95.00000p   64.7819g
 96.00000p   64.7819g
 97.00000p   64.7819g
 98.00000p   64.7819g
 99.00000p   64.7819g
100.00000p   64.7819g
```

最後整理成表格：

Oscillation Period	15.4364 ps
Oscillation Frequency	64.7819 GHz
Average Power	17.3241 uW
Maximum Power	28.0433 uW

Table2. SPICE Simulation results of 3-stage inverter-based ring oscillator

3. (50%) Design a dynamic D register as shown in Fig.1 with propose size of NMOS and PMOS to have better tsetup, tpcq, tpdq and thold time. Both D and CLK has rise time and fall time of 0.1ns (0V-0.75V).
   a) Explain your sizing principle of each MOS to have least tsetup, tpcq, tpdq and thold time for register 1 and 0.
   b) Run SPICE to verify your results and list the results in table form for part (b).

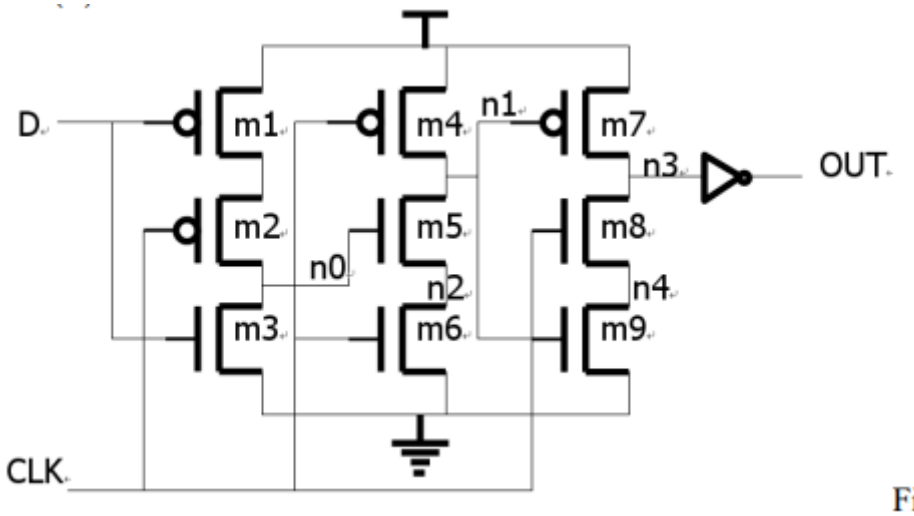

Fig.1

Ans:

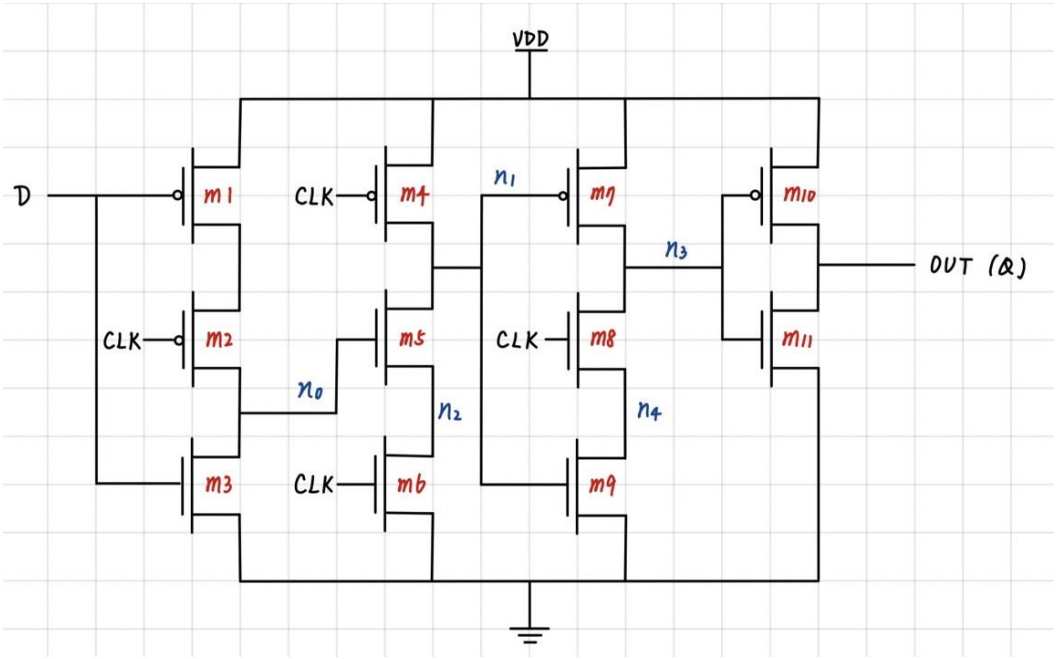

Fig8. Dynamic D register

X: previous state / ?: unknown state

a)

Register 0 (out=0)

CLK		D	n0	n1	n2	n3	n4	OUT (Q)
0	Initially	1	0	1	X	X	0	X
	Then	0	1	1	1	X	0	X
1	Initially	0	1	0	0	1	1	0
	Then	1	0	0	0	1	1	0

t_{setup}	t_{pcq}	t_{pdq}	t_{hold}
m1 + m2	m8 + m9 + m10	m5 + m6 + m7 + m11	m5 + m6 –m3
在 m2 被 CLK 關掉前，m1 與 m2 把 n0 充電至 1 的時間。	當 CLK 為 1 的時候，一開始 n1 = 1，n3 可能會暫時被 m8, m9 放電，所以 OUT 會被充電。因此，當 clock edge 觸發時，OUT 訊號不會立即穩定，需要一段時間才能完全穩定。	在 CLK 變成 1 之後，n1, n2 放電至 0，n3 要被充電至 1，OUT 要被放電至 0 所花的時間。	CLK 變成 1 之後，若 D 太快變化成 1，n0 會被 m3 放電至 0，導致 n1 不能被 m5, m6 放電，所以 D 需要維持一段時間才能變成 1，此時間為 m5, m6 放電的時間再扣 m3 放電的時間。

Table3. Timing specification for register 0 (D = 0)

Register 1(out=1)

CLK		D	n0	n1	n2	n3	n4	OUT (Q)
0	Initially	0	1	1	1	X	0	X
	Then	1	0	1	1	X	0	X
1	Initially	1	0	1	0	0	0	1
	Then	0	0	1	0	0	0	1

t_{setup}	t_{pcq}	t_{pdq}	t_{hold}
m3	m8 + m9 + m11	m8 + m9 + m11	0
在 CLK 變 1 前，n0 要放電到到 0，讓 n1 維持穩定。	在 CLK 變成 1 之後，n3 要放電才能讓 OUT 充電到 1。	在 CLK 變成 1 之後，n3 要放電才能讓 OUT 充電到 1。	CLK 變成 1 之後，D 變 0 不會影響 n0。

Table4. Timing specification for register 1 (D = 1)

Sizing Principle

(1) Stage 1: m1, m2, m3

這三顆 MOS 都會影響 register 0 (out = 0)或 register 1(out = 1)的 setup time (t_{setup})。因此，先將這三顆 MOS 放大 2 倍。因為 m1, m2 這兩顆 PMOS 串聯，為了維持良好的 Driving 能力，所以再將這兩顆 PMOS 放大兩倍。

→ $n_{m1} = 4$, $n_{m2} = 4$, $n_{m3} = 2$

(2) Stage 2: m4, m5, m6

m4 與 timing 無關，因此設計 $n_{m4} = 1$。m5 與 m6 會影響 register 0 的 t_{pdq} 跟 t_{hold}，因此將 m5 與 m6 放大 2 倍，且這兩顆 NMOS 串聯，因此再將這兩顆放大 2 倍。

→ $n_{m4} = 1$, $n_{m5} = 4$, $n_{m3} = 4$

(3) Stage 3: m7, m8, m9

m7 與 register 0 (out = 0)的 t_{pdq} 有關，因此將 m7 放大 2 倍。m8, m9 與 register 1 (out = 1)的 t_{pdq} 有關，因此將 m8, m9 放大兩倍，又因為這兩顆 NMOS 串聯，再將它們放大 2 倍。

→ $n_{m7} = 2$, $n_{m8} = 4$, $n_{m9} = 4$

(4) Stage 4: m10, m11

因為 m10, m11 要推動後面的 loading，因此將 m11, m12 放大 8 倍。

→ $n_{m10} = 8$, $n_{m11} = 8$

整理成表格：

	Stage 1			Stage 2			Stage 3			Stage 4	
MOS	m1	m2	m3	m4	m5	m6	m7	m8	m9	m10	m11
n	4	4	2	1	4	4	2	4	4	8	8

Table5. Sizing of each MOS

b) Run SPICE to verify your results and list the results in table form

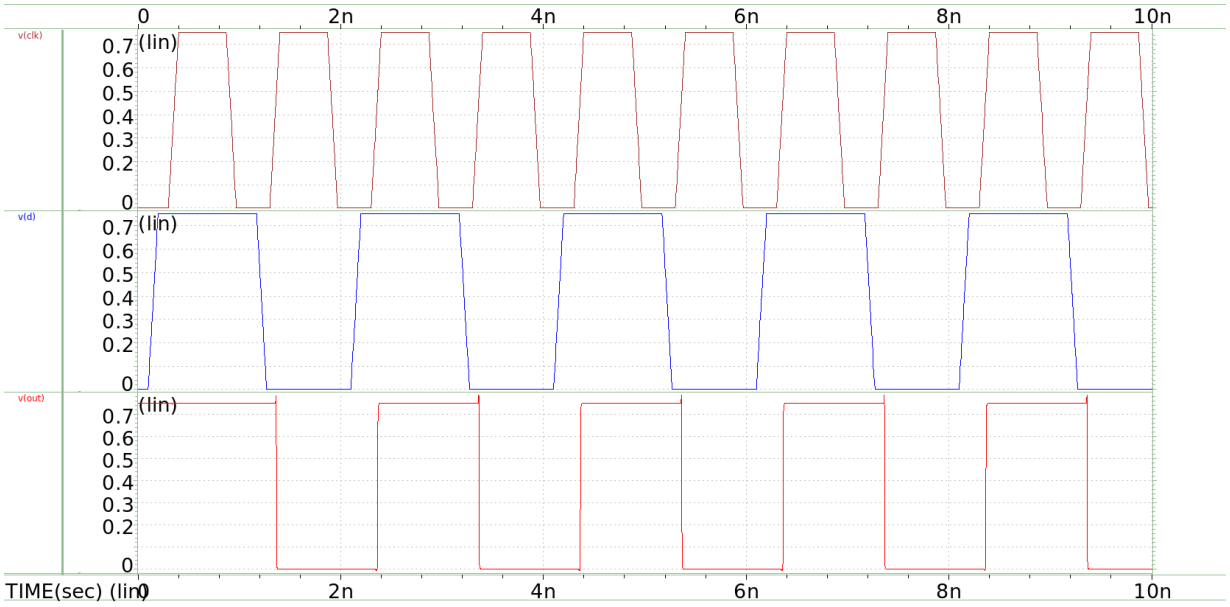

Fig9. SPICE Simulation of Dynamic D register (Pulse)

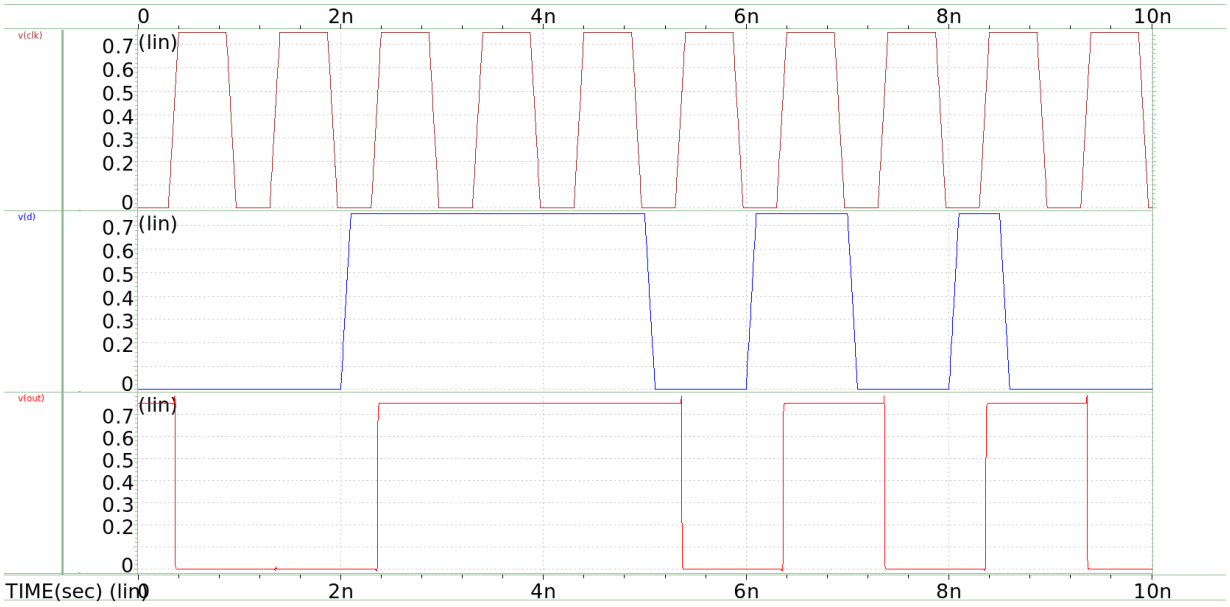

Fig10. SPICE Simulation of Dynamic D register (Piecewise Linear)

使用 Custom WaveView 上方的 Measure Tool 可以測量時間相關資訊。

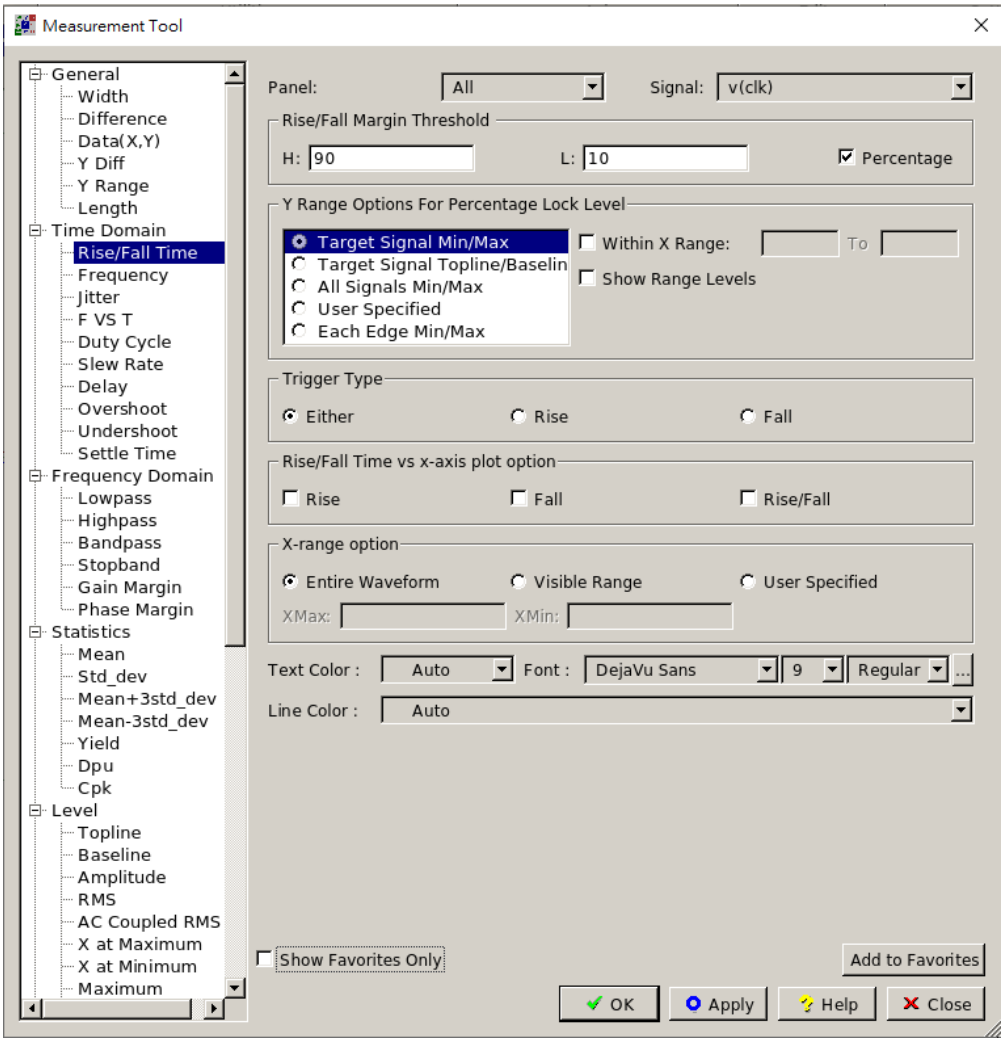

Fig11. WaveView Measure Tool

(1) t_{setup} (採用 10%, 90%)

t_{su0}: time for m1, m2 to charge n0 from 0 to 1 such that n0 becomes 1 before m2 is turned off by clk (m1 + m2)

t_{su0} = 13.2 ps

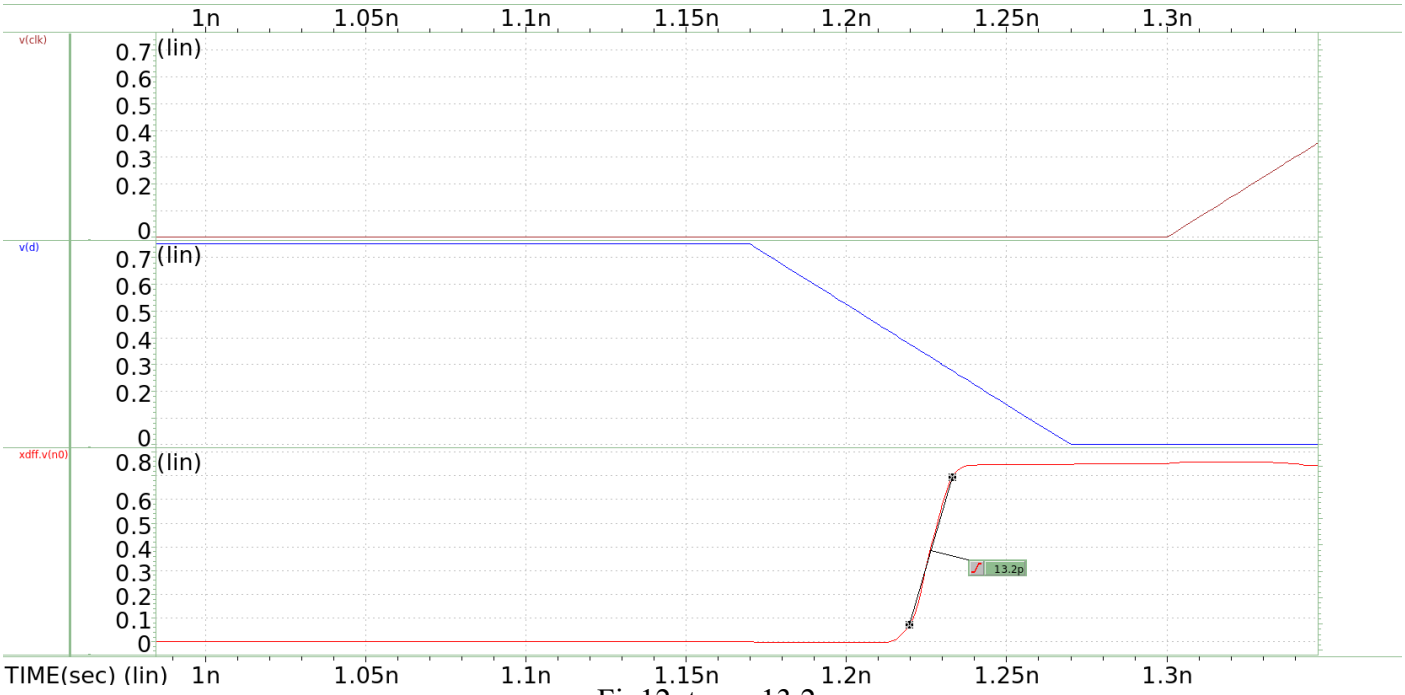

Fig12. t_{su0} = 13.2 ps

t_{su1}: n0 must be 0 before clk=1 such that n2 and n1 will not be discharged through m6 to 0 (m3)

t_{su1} = 14.2 ps

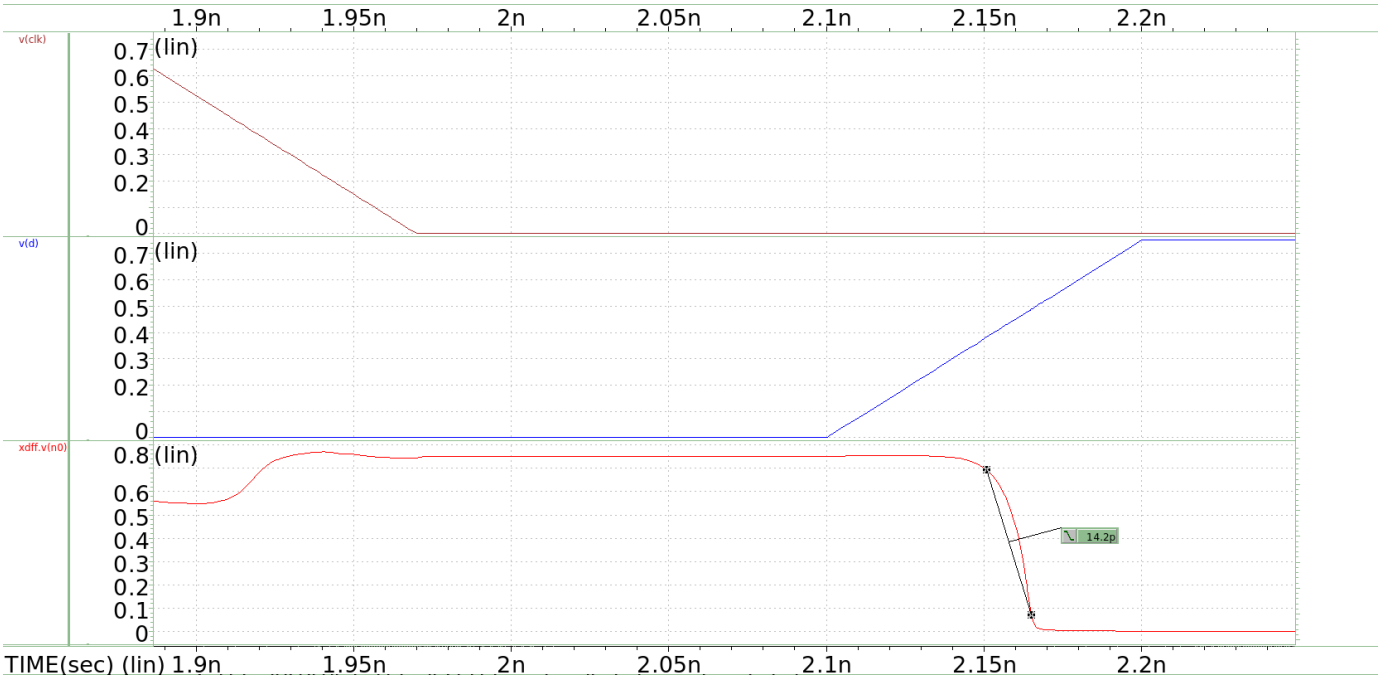

Fig13. t_{su0} = 14.2 ps

(2) t_{pcq} (clk to q propagation delay)

t_{pcq0} = 12.3 ps (Q from 0 to vdd)

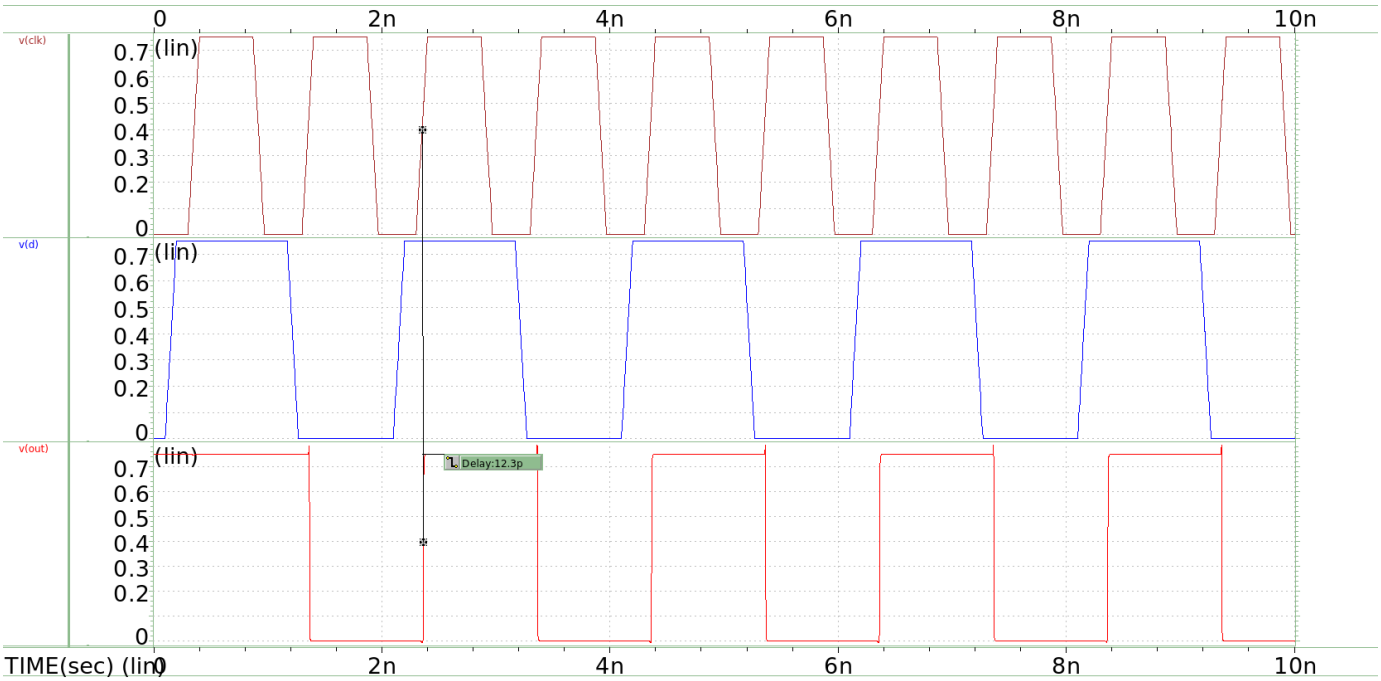

Fig14. t_{pcq} = 12.3 ps (Q from 0 to vdd)

t_{pcq1} = 12.9 ps (Q from vdd to 0)

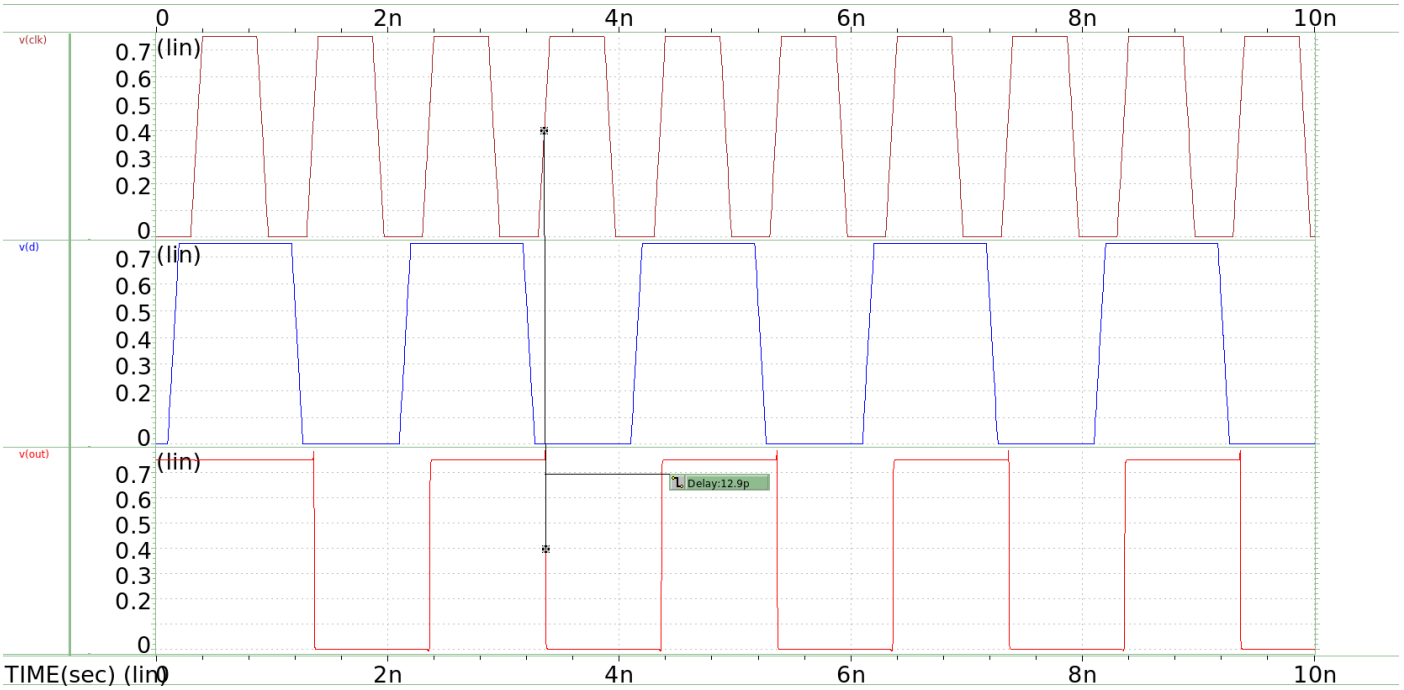

Fig15. t_{pcq} = 12.9 ps (Q from vdd to 0)

(3) t_{pdq}

t_{pd0}: After clk becomes 1, time for n1 and n2 to be discharged, n3 to be charged and then OUT to be discharged (m5 + m6 + m7 +m11)

t_{pd0} = 148 ps

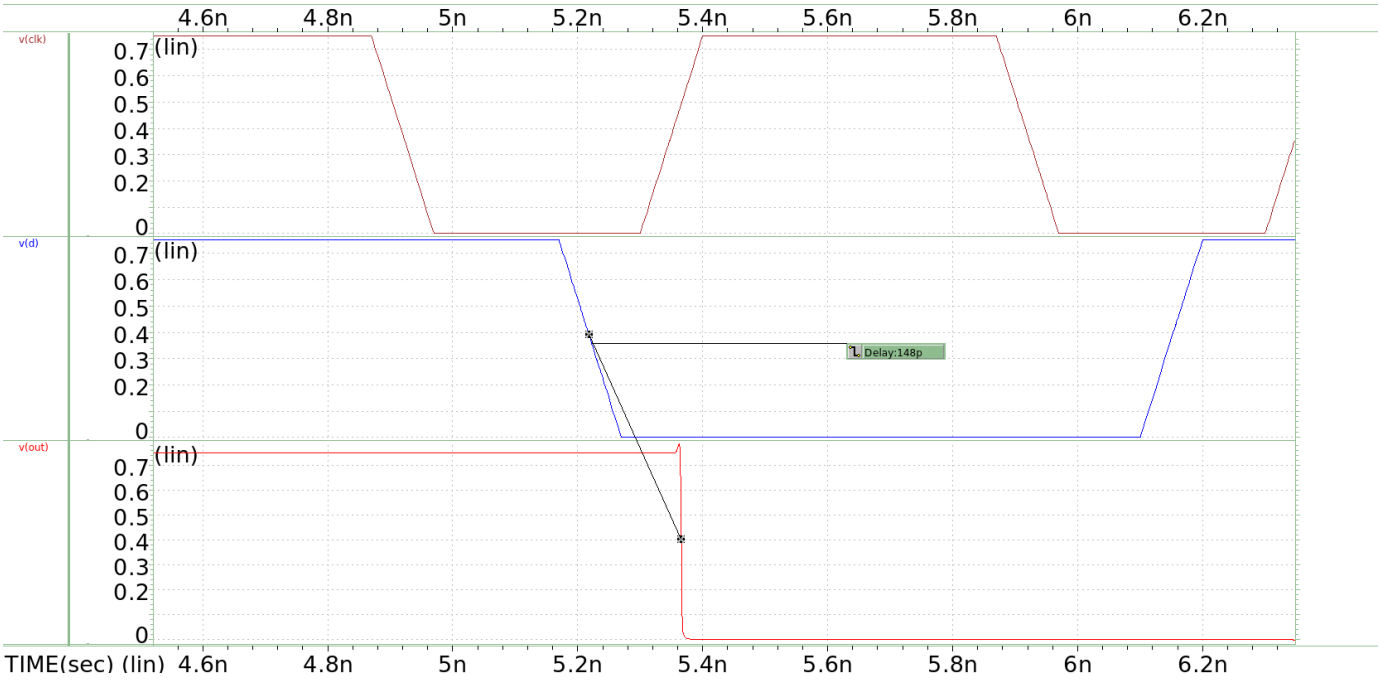

Fig16. t_{pd0} = 148 ps

t_{pd1}: After clk becomes 1, time for n3/OUT to be discharged/charged to 0/1 (m8 + m9 + m11)

t_{pd1} = 212 ps

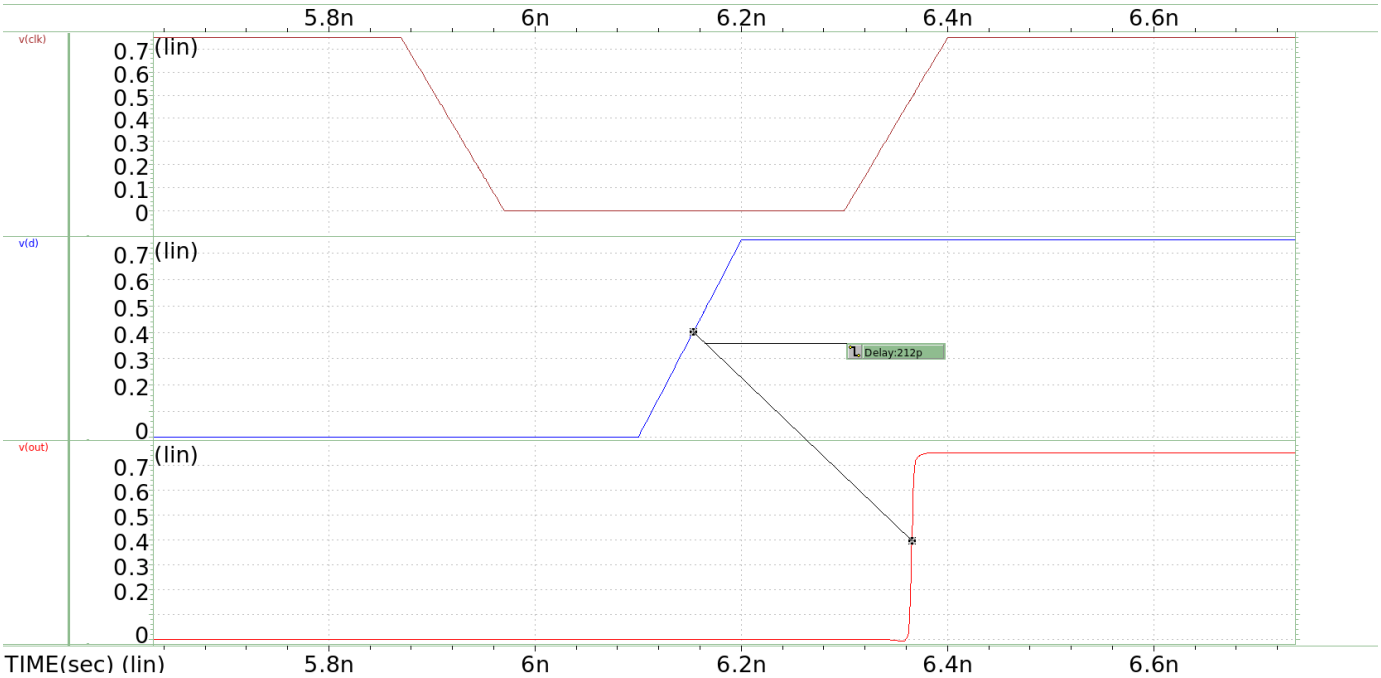

Fig17. t_{pd0} = 212 ps

(4) t_{hold}

t_{ho0}: D=1, n0=0, n1 can't be discharged through m5 and m6 (m5 + m6 – m3)

t_{ho0} = 12.7 ps

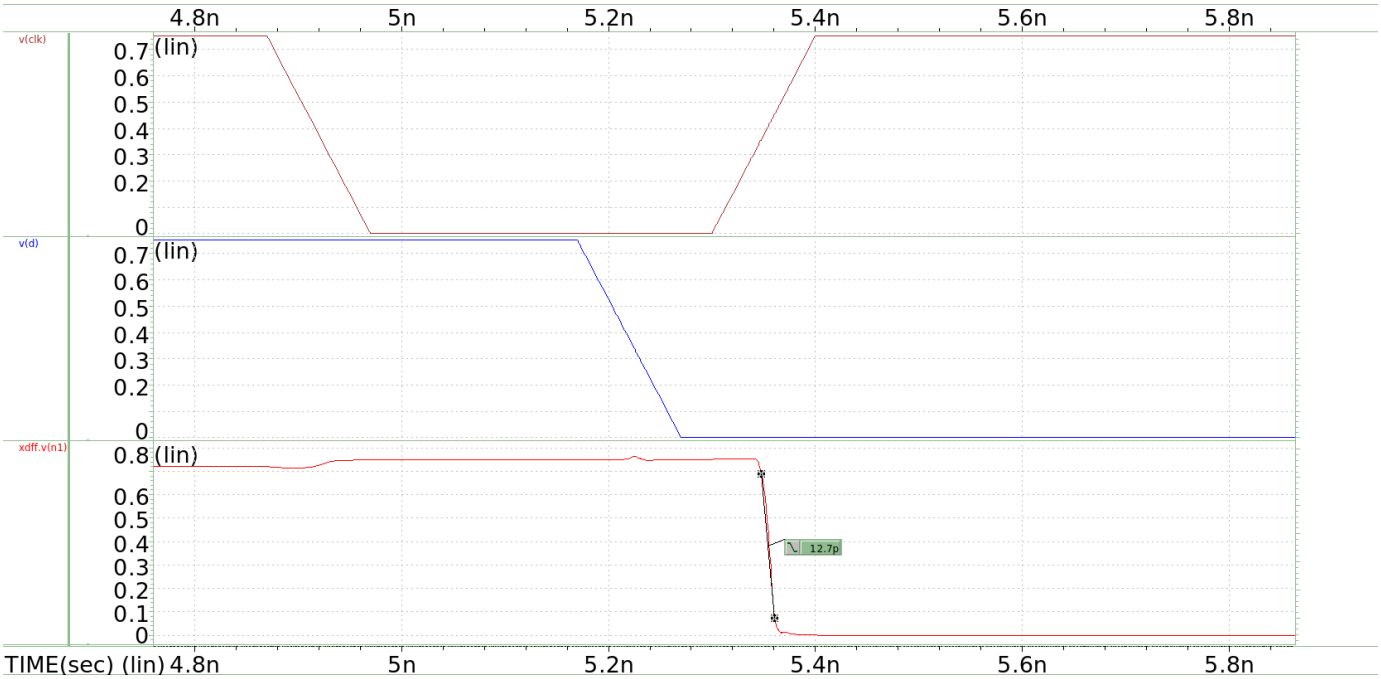

Fig18. t_{ho0} = 12.7 ps

t_{ho1}: D=0, n0=X

t_{ho1} = 0 ps

整理成表格:

t_{su0}	t_{pcq0}	t_{pd0}	t_{ho0}
13.2 ps	12.3 ps	148 ps	12.7 ps
t_{su1}	t_{pcq1}	t_{pd1}	t_{ho1}
14.2 ps	12.9 ps	212 ps	0 ps

Table6. Timing Results