Digital Integrated Circuits

#Home Work 8 2023.05.12 (Due:2023.05.26, 13:20)

Consider the circuit in Fig.7. Modules A and B have a delay of 20ns and 29.6 ns at 1.0 V (Vdd), and switch 20 pF and 35 pF (C) respectively. All the buses in Fig.8 are 20 bits. The register has a 0.4 ns delay and switches 0.05 pF. The clock rate of Fig.7 is thus 1/(50 ns) and the power dissipation is P0. The power dissipation can be estimated by $P= C \bullet Vdd^2 \bullet F$ and the delay with respect to Vdd can be approximated by k/(Vdd-Vt) with Vt equals 0.3 V. k is a constant and is different for A and B. You can use the information of delay time, Vdd and Vt to calculate k.

(a) Adding a pipeline register between A and B allows for reduction of the supply voltage (A and B can use different Vdd) while maintaining throughput (P1). Show the block diagram, explain the operation and calculate the power reduction ratio, P1/P0 (30%)

(b) Assume that a 2-to-1 multiplexer has a delay of 0.4 ns at 1.0 V and switches 0.05 pF. Try parallel version with two copies (using two A and B modules) while maintaining date rate (P2). Show the block diagram, explain the operation and calculate power reduction ratio, P2/P0. (30%)

(c) Try to combine (a) and (b) to design a parallel-pipeline version while maintaining data rate(p3). Show the block diagram, explain the operation and calculate power reduction ratio, P3/P0 (40%)

Fig.7