



Lab2: Channel and Interface

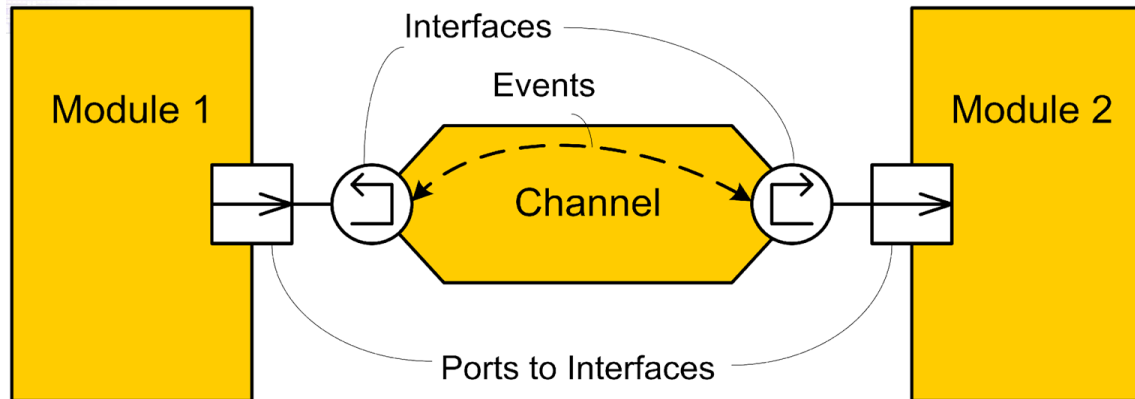
Kun-Chih (Jimmy) Chen 陳坤志

kcchen@nycu.edu.tw

*Institute of Electronics,
National Yang Ming Chiao Tung University*



Channel and Interface



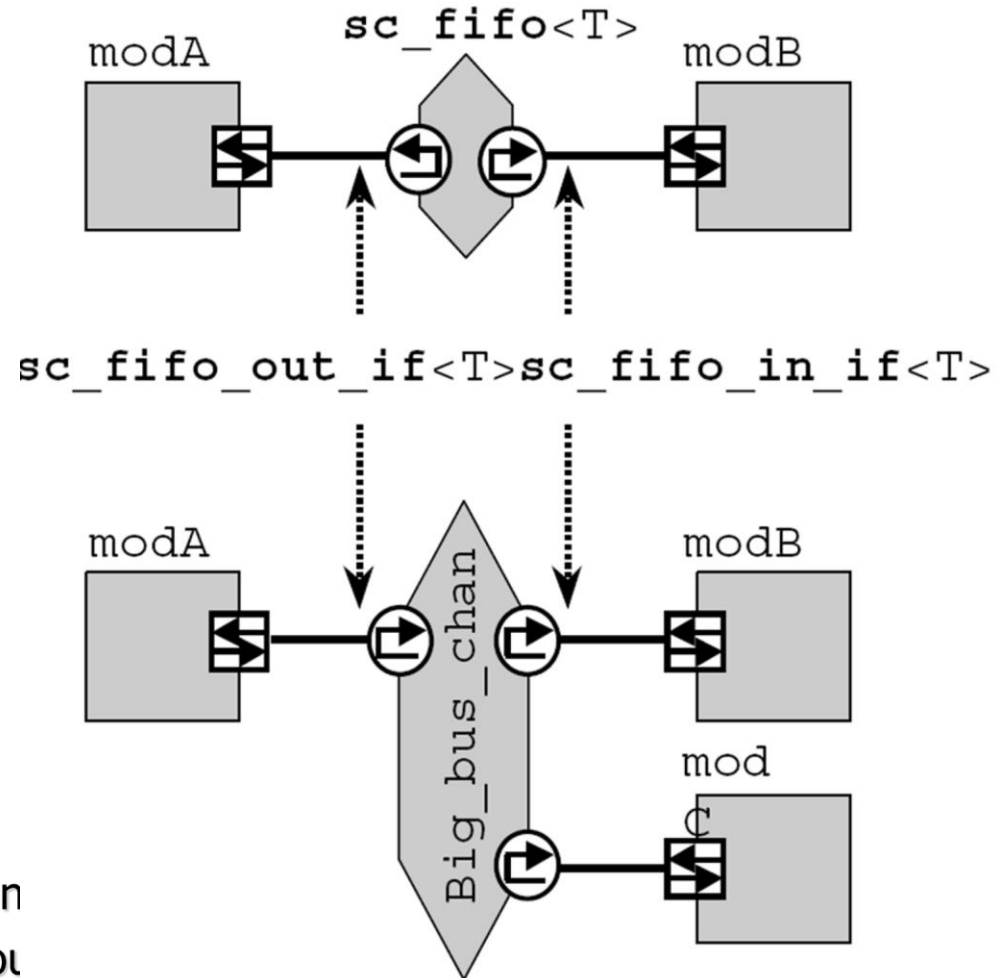
❖ Channel

- ❖ `sc_signal<T>`
- ❖ `sc_signal_resolved`
- ❖ `sc_signal_rv<W>`
- ❖ `sc_buffer<T>`
- ❖ `sc_fifo<T>`
- ❖ `sc_mutex`
- ❖ `sc_semaphore`

❖ Interface

- ❖ `sc_fifo_in_if`
- ❖ `sc_fifo_out_if`
- ❖ `sc_mutex_if`
- ❖ `sc_semaphore_if`
- ❖ `sc_signal_in_if`
- ❖ `sc_signal_out_if`

Example: FIFO Interface



sc_port <interface> portname;

Example:

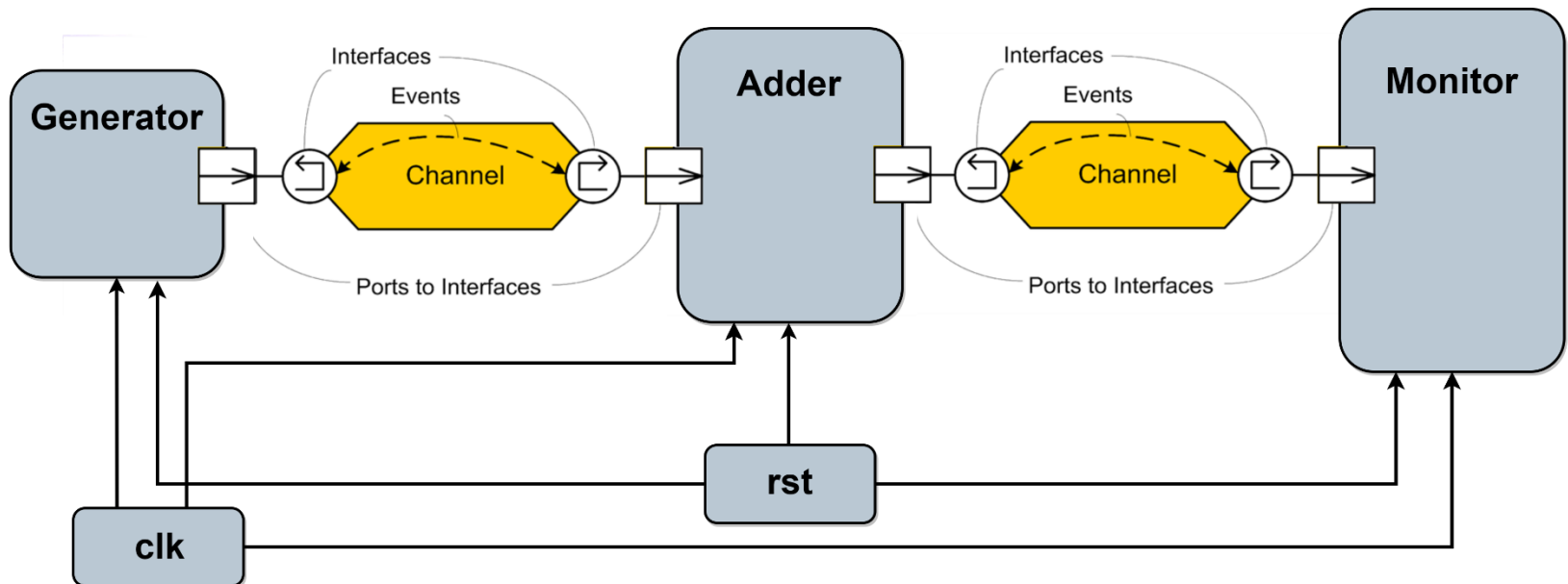
```
SC_MODULE(stereo_amp) {
    sc_port<sc_fifo_in_if<int> > soun
    sc_port<sc_fifo_out_if<int> > sol
    ...
};
```

space
↓

Lab2: Adder with channel interface

❖ Three modules

- ❖ Random number generator (random seed = $i+1$)
 - Generate 100 random numbers, and the range is between 0~99
- ❖ Adder
 - Compute the sum of the two inputs
- ❖ Monitor
 - Check the correctness of the addition results



Lab Requirement

- ❖ Due in one week (2023/05/31)
 - ❖ Complete the three modules.
 - ❖ Practice **sc_fifo**, **sc_signal**, and **sc_buffer** in this Lab
 - ❖ Use Platform Architecture and Terminal to simulate output results.
 - Without channels in the PA
 - With channels outside the PA
 - ❖ Upload compressed file which include source codes (all of your file, include PA project file, source code....) to E3@NYCU
 - File name rule: Student ID_Lab2