



# Lab1: Multiply Accumulation Unit Design with SystemC

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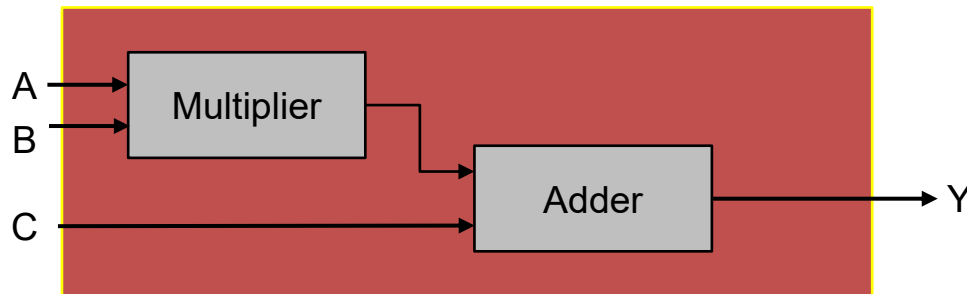
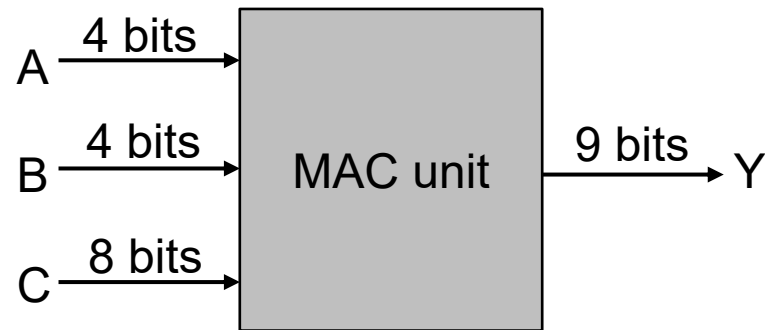
*Institute of Electronics,  
National Yang Ming Chiao Tung University*



# Lab1

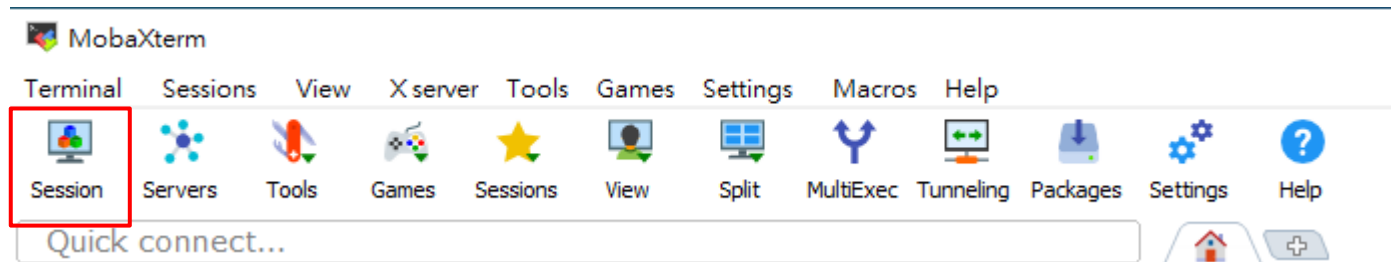
❖ Design a multiply accumulate unit

❖  $Y = A \times B + C$



# Start

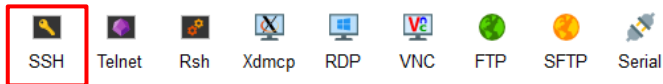
- ❖ Download MobaXterm
  - ❖ <https://mobaxterm.mobatek.net/>
- ❖ MobaXterm installation
- ❖ Create Session to connect server account



# MobaXterm

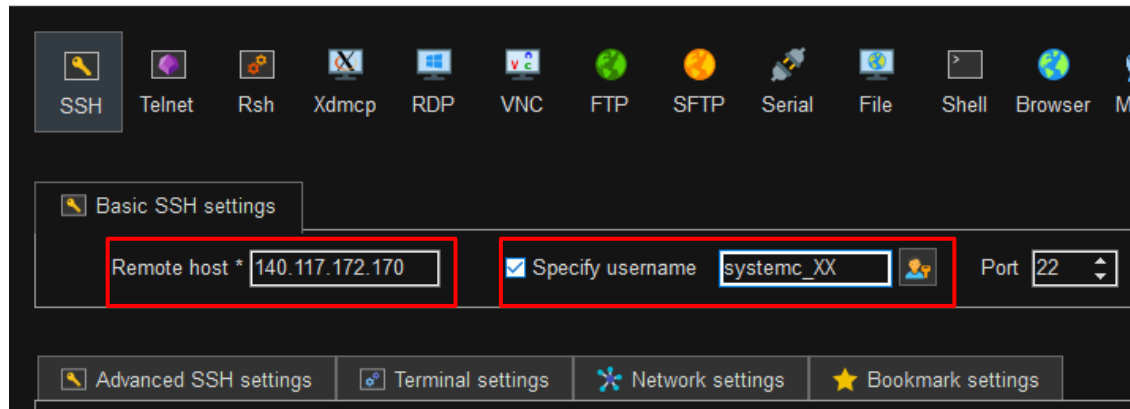
- ❖ SSH -> Remote host -> Specify username -> OK
  - ❖ Remote host : 140.117.172.170
  - ❖ Specify username : your account (Default is ML+your student ID)

Session settings



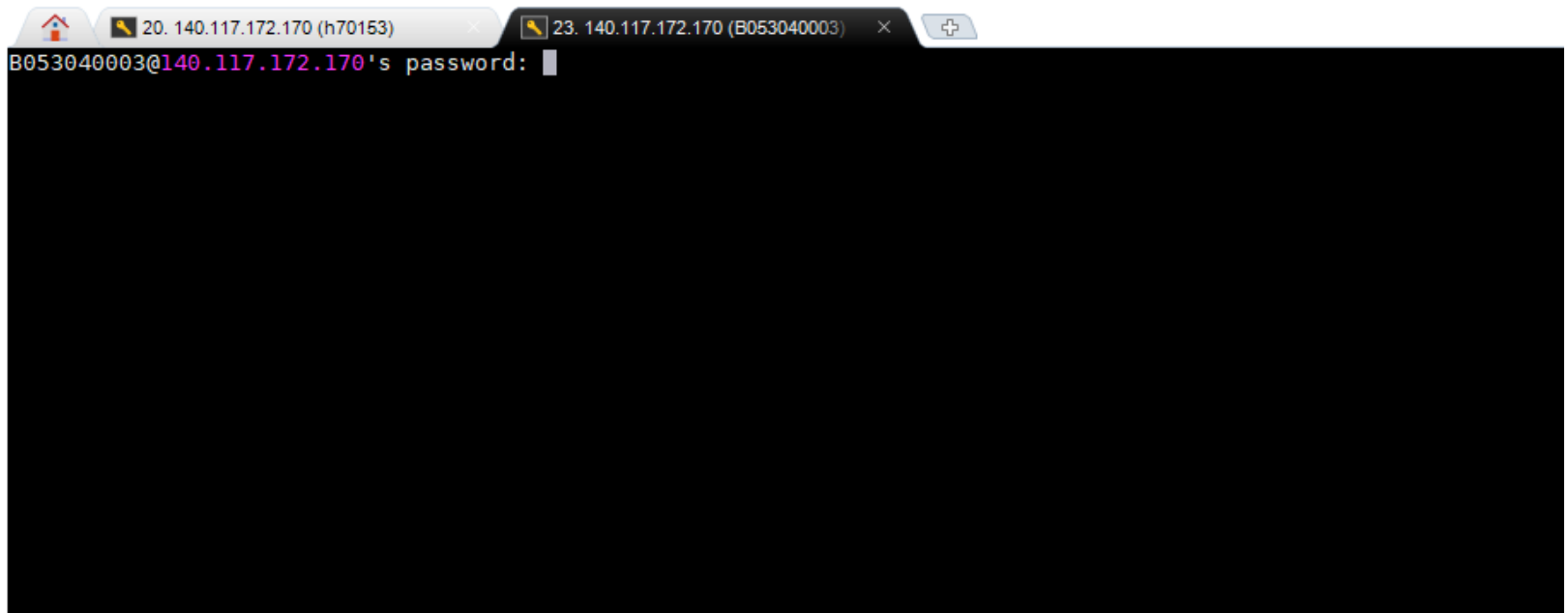
Choose a session t

Session settings

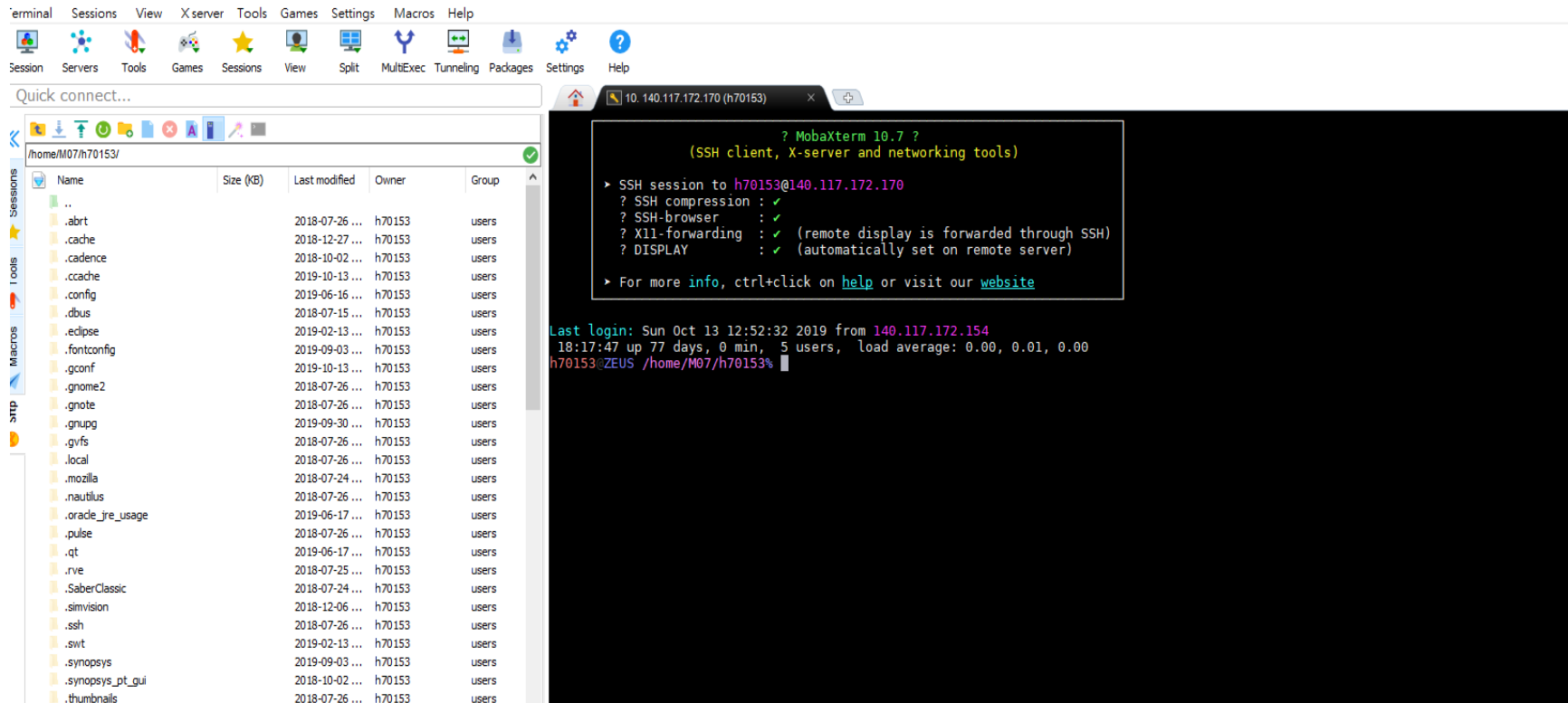
A screenshot of the MobaXterm session settings dialog. The 'SSH' tab is selected. The 'Basic SSH settings' section contains the following fields: 'Remote host \*' with the value '140.117.172.170', 'Specify username' checked with the value 'systemc\_XX', and 'Port' set to '22'. The 'Advanced SSH settings', 'Terminal settings', 'Network settings', and 'Bookmark settings' tabs are visible at the bottom. The 'Remote host' and 'Specify username' fields are highlighted with red rectangular boxes.

# MobaXterm

- ❖ Password (The password will not be displayed on the screen)
  - ❖ Default is your student ID

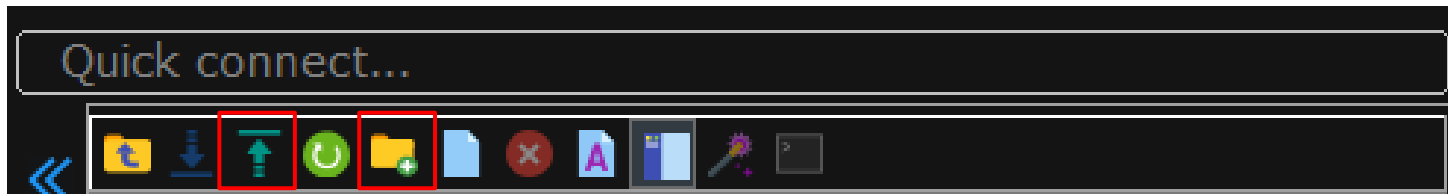


# MobaXterm



# MobaXterm

- ❖ Create folder required for systemC course
- ❖ Upload file to current folder



Name	Size (KB)	Last modified
..		
dockreset.cpp	1	2021-10-29 ...
dockreset.h	1	2021-10-29 ...
MAC.h	1	2021-10-29 ...
main.cpp	1	2021-10-29 ...
Monitor.cpp	1	2021-10-29 ...
Monitor.h	1	2021-10-29 ...
Pattern.cpp	1	2021-10-29 ...
Pattern.h	1	2021-10-29 ...

# SystemC

## ❖ %tool

- ❖ Choose 17 to source the license
- ❖ Use enter to return to the menu, then type 0 to quit

```
User : localhost:10.0
*****
*                               EDA TOOL SELECTION MENU                               Ver 2.0 Oct, 2018 *
*****
--- Cadence -----
[ 1] Cosmos Scope(64bit)      2015.03
[ 2] SoC Encounter           ISR4_14.24.000
[ 3] Virtuoso IC             51.41.151
      MMSIM                  10.11.412
[ 4] Incisive Enterprise Simulator
      (NC-verilog)           14.10.005
[ 5] Innovus                 2017.11
--- Mentor Graphics -----
[ 6] ModelSim                10.6a
[ 7] Calibre                  2017.4 19.14
--- Synopsys -----
[ 8] PrimeTime-PX            2018.06
[ 9] HSPICE                  2015.06
[10] Design Compiler         2013.03-sp5
[11] IC Compiler             2017.09-sp2
[12] CostomSim (xa)          2017.12
[13] NanoSim                 2013.03
[14] VCS                     2017.03
[15] Verdi (nWave)           2018.09
[16] Platform Architecture 2017.06
*****
*                               OTHERS                               *
*****
--- Libraries -----
[17] System C                 2.3.1
*****
Please make your selection (0 to quit) ==> █
```



# SystemC

## ❖ Source file

- ❖ xxx.h
- ❖ xxx.cpp
- ❖ Main.cpp

## ❖ Makefile

- ❖ Compile the source file

```
LIB_DIR=/usr/systemc/lib-linux64
INC_DIR=/usr/systemc/include
LIB=-lsystemc -lm -DSC_INCLUDE_FX
#RPATH=-Wl,-rpath=/usr/local/systemc-2.3.1a/lib-linux64

O = LAB → output file name
C = *.cpp

all:
    g++ -I . -I $(INC_DIR) -L . -L $(LIB_DIR) -o $(O) $(C) $(LIB)

clean:
    rm -rf $(O)
```

# SystemC

- ❖ Edit your source code by editor (e.g., notepad++,...)
- ❖ MAC.h

```
SC_MODULE( Adder ) {  
    sc_in < sc_uint<8> > in1,in2;  
    sc_out < sc_uint<9> > out;  
  
    void run() {  
        // vvvvvv put your code here vvvvvv  
  
        // ^^^^^ put your code here ^^^^^  
    }  
  
    SC_CTOR( Adder ) {  
        SC_METHOD( run );  
        sensitive << in1 << in2;  
    }  
};
```

```
SC_MODULE( Multiplier ) {  
    sc_in < sc_uint<4> > in1,in2;  
    sc_out < sc_uint<8> > out;  
  
    void run() {  
        // vvvvvv put your code here vvvvvv  
  
        // ^^^^^ put your code here ^^^^^  
    }  
  
    SC_CTOR( Multiplier ) {  
        SC_METHOD( run );  
        sensitive << in1 << in2;  
    }  
};
```

# SystemC

- ❖ Edit your source code by editor (e.g., notepad++,...)
- ❖ MAC.h

```
SC_MODULE( MAC ) {  
    sc_in < sc_uint<4> > in1, in2;  
    sc_in < sc_uint<8> > in3;  
    sc_out < sc_uint<9> > out;  
  
    Adder *ADD_1;  
    Multiplier *MUL_1;  
  
    // vvvvvv put your code here vvvvvv  
  
    // ^^^^^ put your code here ^^^^^  
  
    SC_CTOR( MAC )  
    {  
        // vvvvvv put your code here vvvvvv  
  
        // ^^^^^ put your code here ^^^^^  
    }  
};
```

# SystemC

- ❖ `cd < file path >`
- ❖ `%make`

```
h70153@ZEUS /home/M07/h70153/sys% make
g++ -I . -I /usr/systemc/include -L . -L /usr/systemc/lib-linux64 -o test *.cpp -lsystemc -lm -DSC_INCLUDE_FX
h70153@ZEUS /home/M07/h70153/sys% █
```

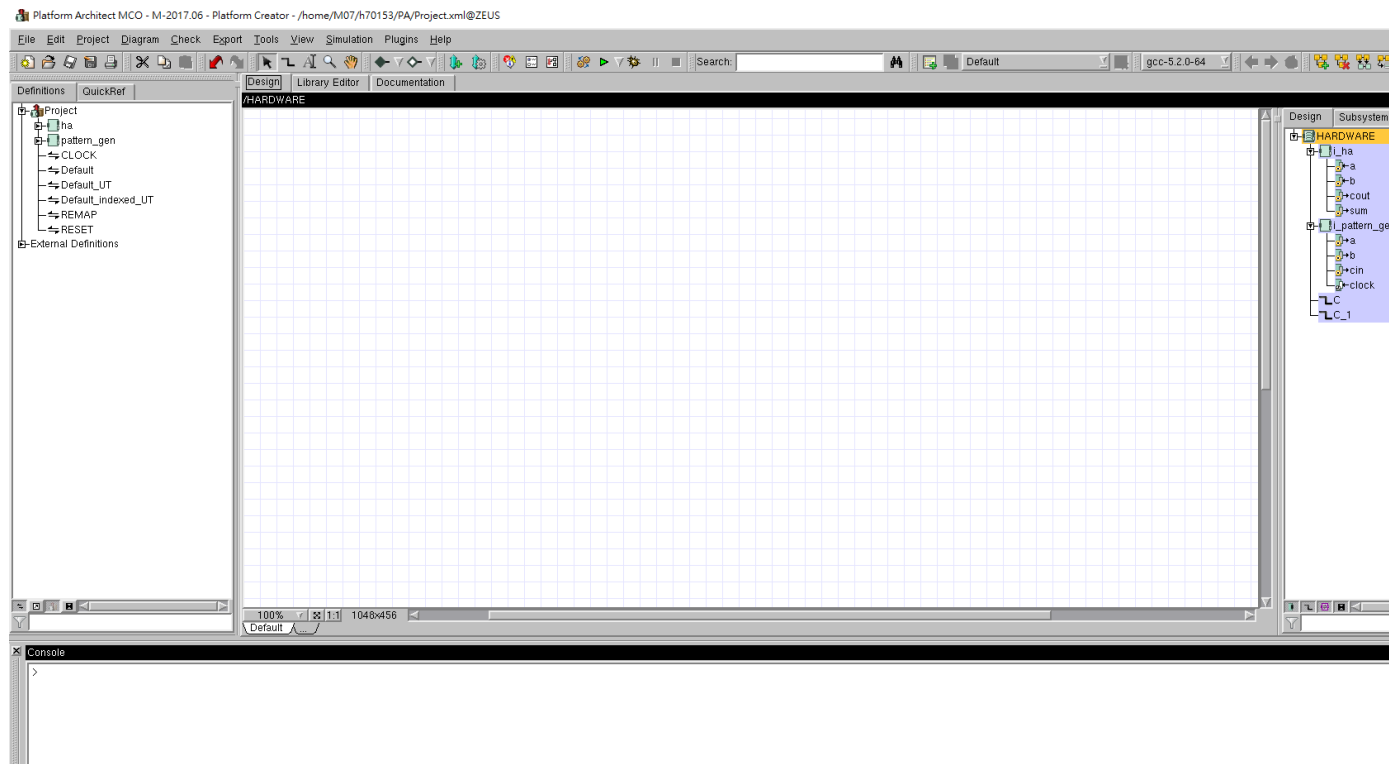
- ❖ `%< output file name >`
  - ❖ Execute the systemC code

```
SystemC 2.3.1-Accellera --- Jun 22 2017 17:44:29
Copyright (c) 1996-2014 by all Contributors,
ALL RIGHTS RESERVED
A      B      C      Y
7      6      105    147
3      1      255    258
10     12     41     161
13     10     171    301
2      11     227    249
6      12     194    266
4      8      27     59
8      7      141    197

Info: /OSCI/SystemC: Simulation stopped by user.
```

# Platform Architect

- ❖ Provides the simulation performance and analysis insight for designers to validate the architecture in SystemC at the transaction level



# Platform Architect

- ❖ %tool
  - ❖ Choose 16 to source the license
  - ❖ Use enter to return to the menu, then type 0 to quit
- ❖ %pct & (run on the background)

```
User : localhost:12.0
*****
*                               EDA TOOL SELECTION MENU           Ver 2.0 Oct, 2018 *
*****
--- Cadence -----
[ 1] Cosmos Scope(64bit)      2015.03
[ 2] SoC Encounter            ISR4_14.24.000
[ 3] Virtuoso IC              51.41.151
      MMSIM                  10.11.412
[ 4] Incisive Enterprise Simulator
      (NC-verilog)           14.10.005
[ 5] Innovus                  2017.11
--- Mentor Graphics -----
[ 6] ModelSim                  10.6a
[ 7] Calibre                   2017.4_19.14
--- Synopsys -----
[ 8] PrimeTime-PX             2018.06
[ 9] HSPICE                   2015.06
[10] Design Compiler          2013.03-sp5
[11] IC Compiler              2017.09-sp2
[12] CostomSim (xa)           2017.12
[13] NanoSim                  2013.03
[14] VCS                      2017.03
[15] Verdi (nWave)            2018.09
[16] Platform Architecture    2017.06
*****
*                               OTHERS                             *
*****
--- Libraries -----
[17] System C                  2.3.1
*****
Please make your selection (0 to quit) ==> 16
...Source Platform Architecture

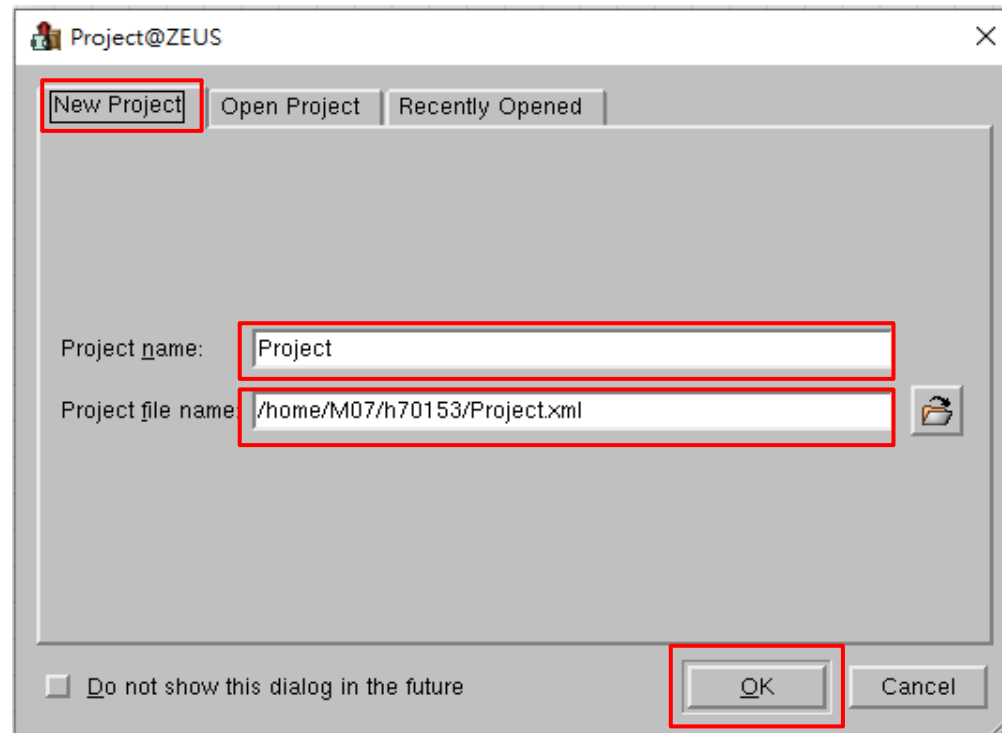
Note: COWARE_CXX_COMPILER is set to gcc-5.2.0-64.

Setup is complete for Synopsys Platform Architect

% pct
█
```

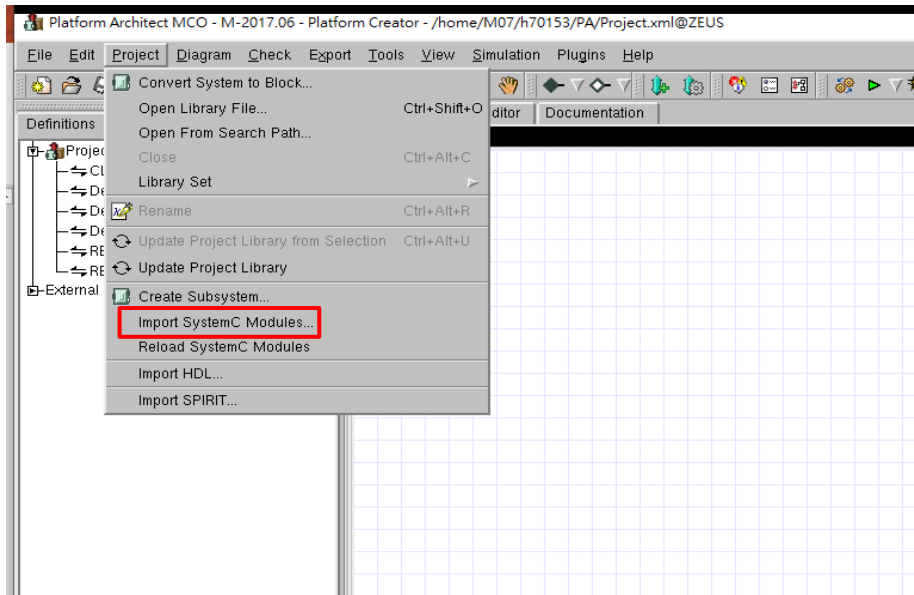
# Platform Architect

- ❖ Create project -> Project name -> Project file name -> OK



# Platform Architect

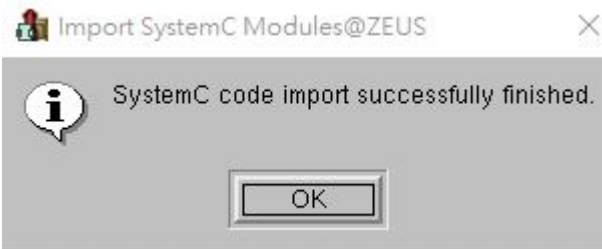
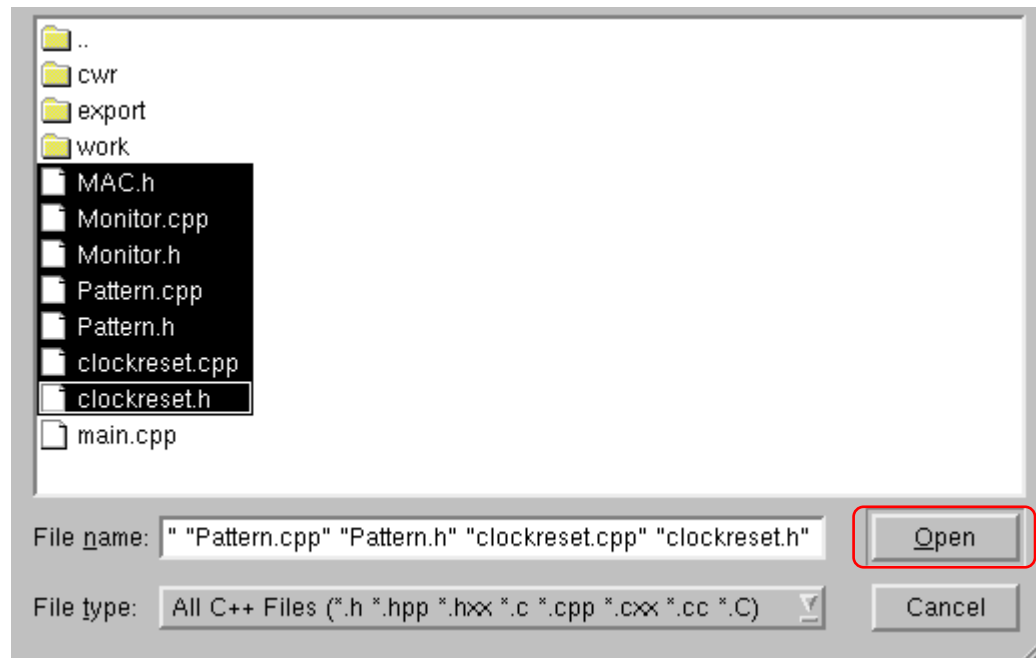
## ❖ Import SystemC Modules -> Add





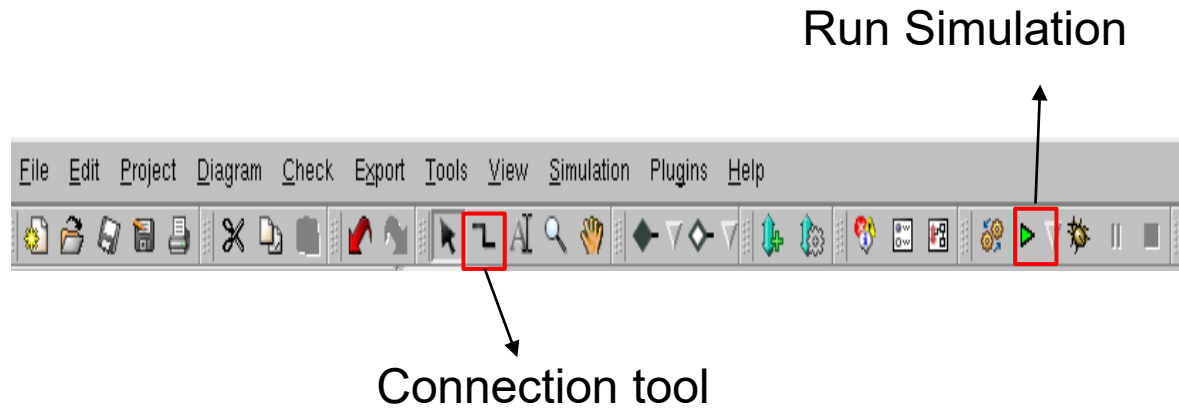
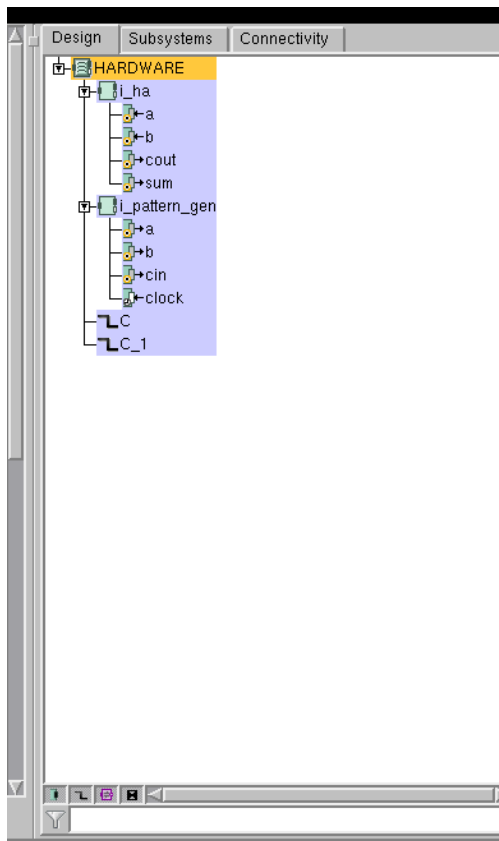
# Platform Architect

## ❖ Add required files



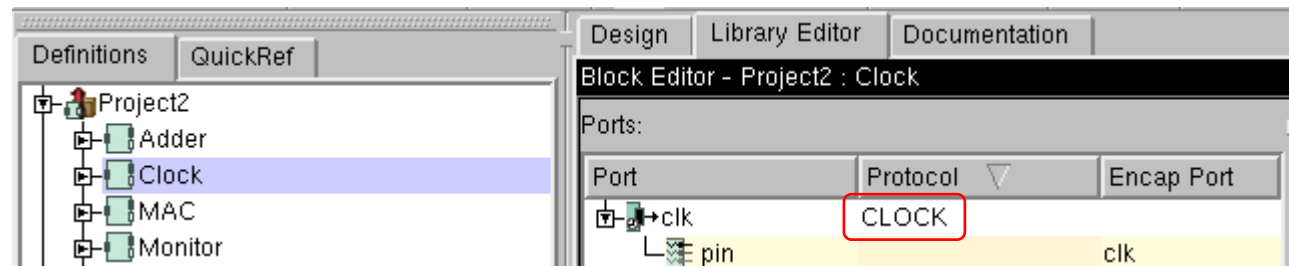
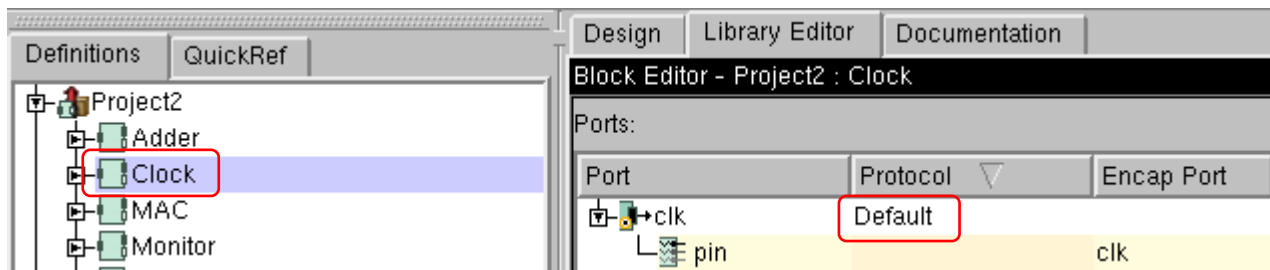
# Platform Architect

## Design Browser



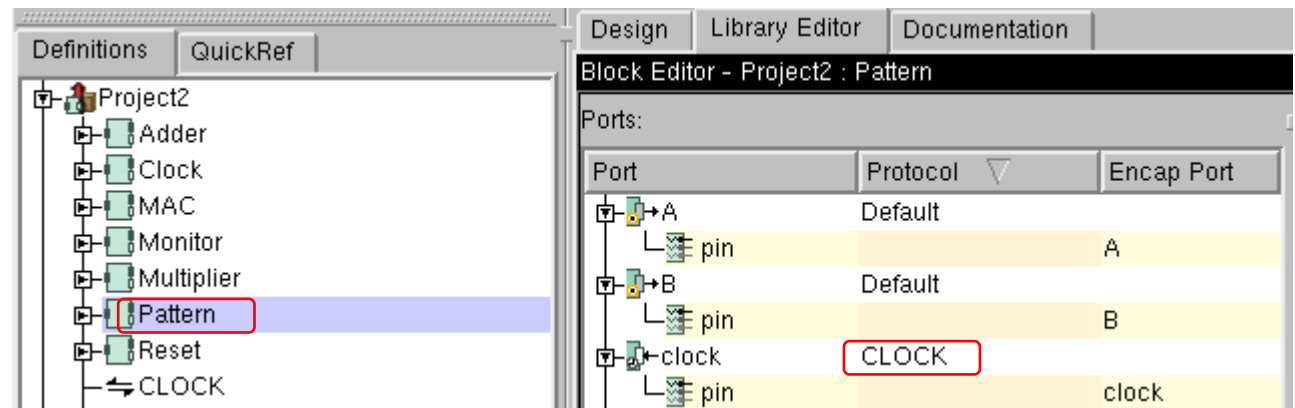
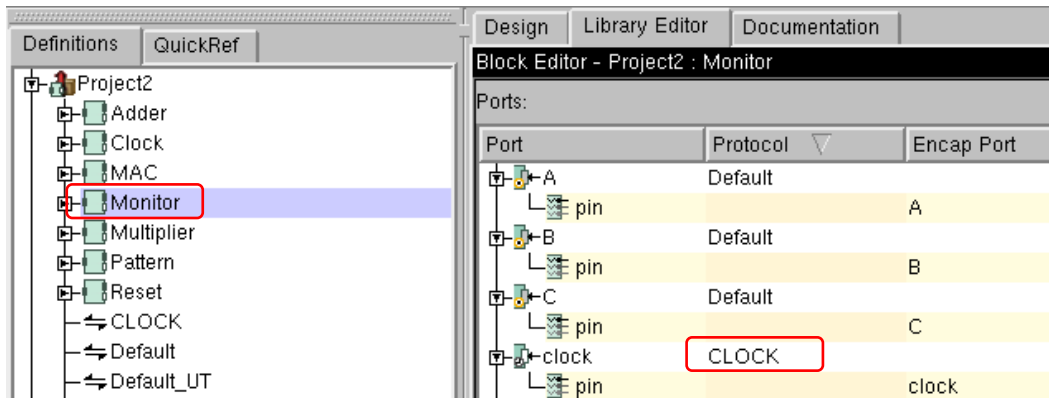
# Platform Architect

- ❖ Change protocol of clock port
- ❖ Double click Clock -> Click Default -> Choose CLOCK



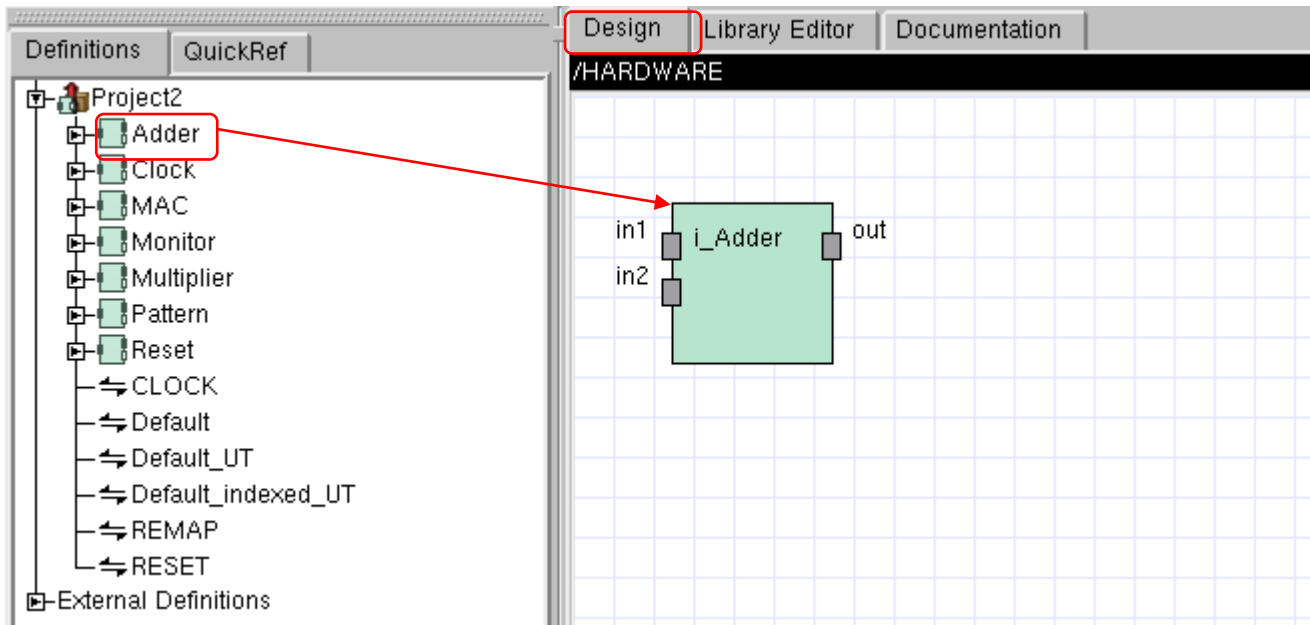
# Platform Architect

- ❖ Repeat the same action to change the clock protocol of Pattern and Monitor block



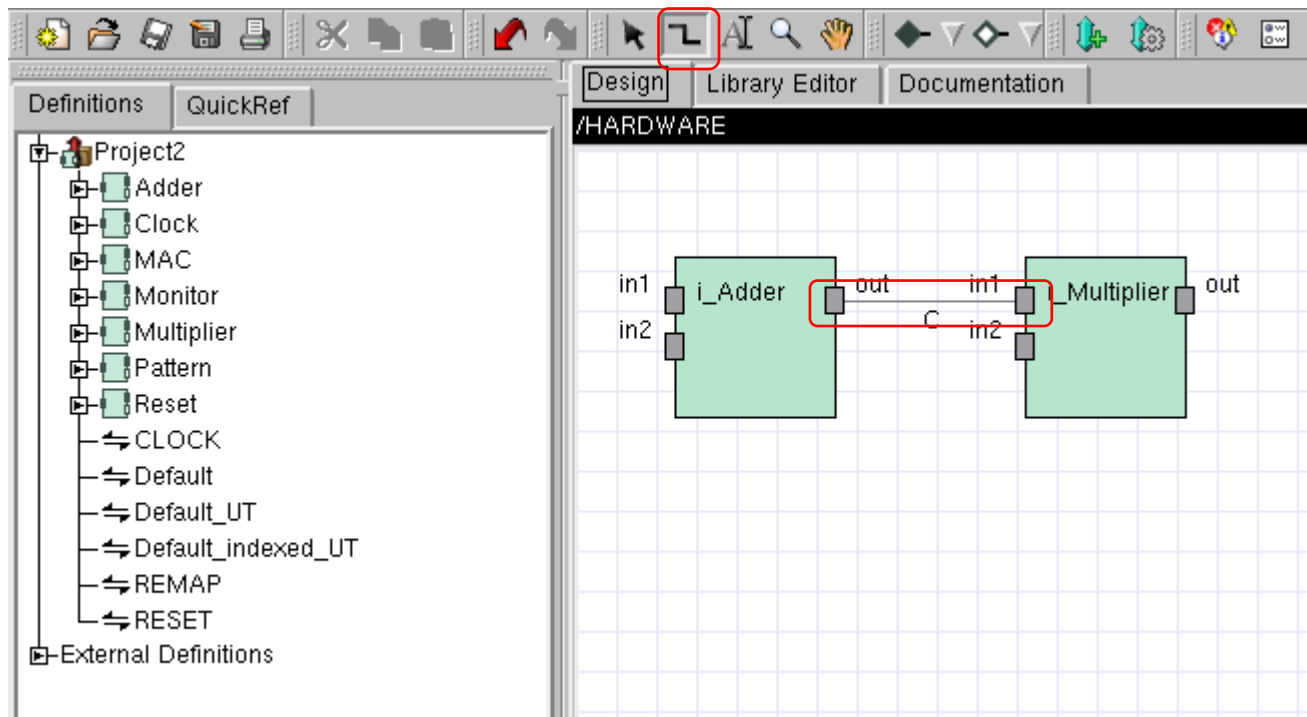
# Platform Architect

- ❖ Create the block
  - ❖ Click and drag to the design window



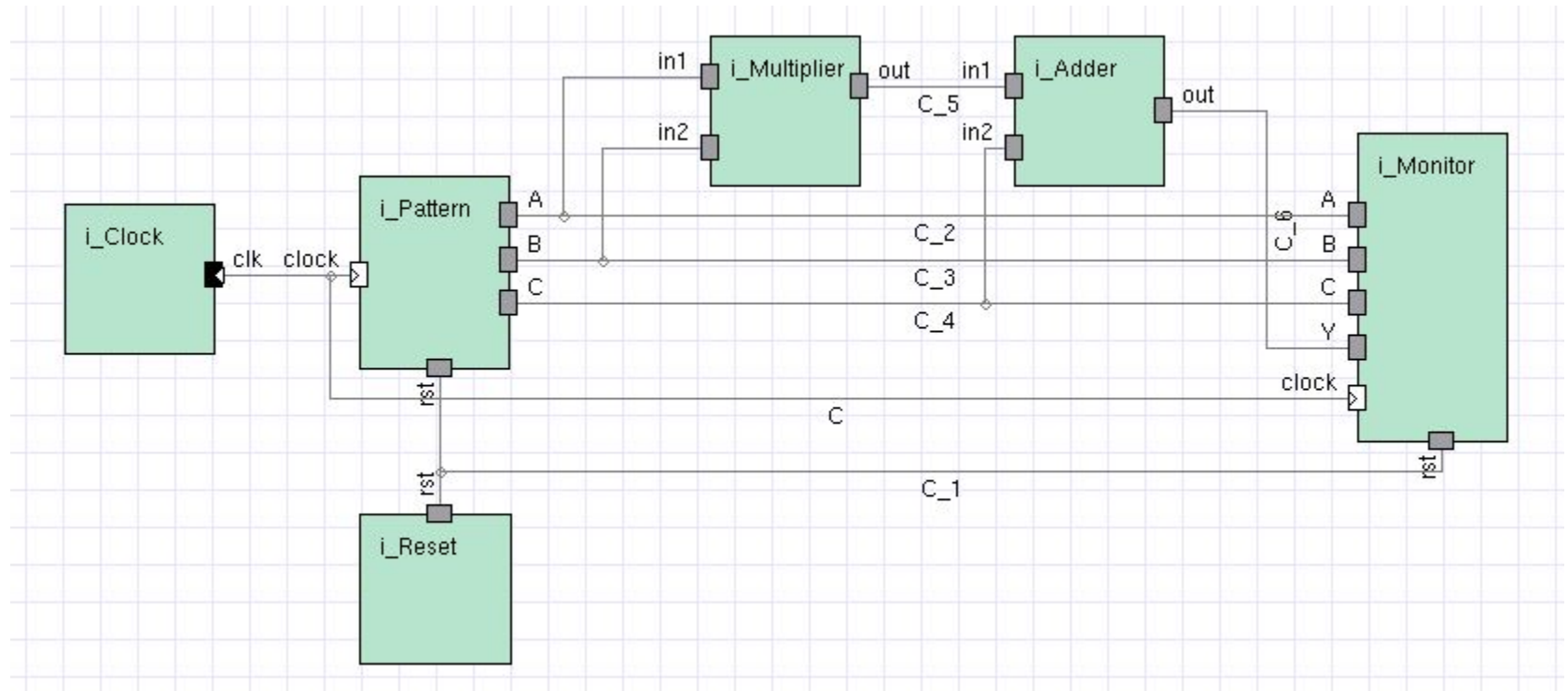
# Platform Architect

- ❖ Use connection tool to connect the block



# Platform Architect

## ❖ Block diagram



# Platform Architect

❖ Click Clock block -> Set clock period

❖ division -> 5

❖ cycle -> 40

The screenshot displays the Platform Architect software interface. At the top, a toolbar contains various icons, with a mouse cursor icon highlighted by a red box and labeled '1'. Below the toolbar, a green block labeled 'i\_Clock' is placed on a grid, with a red dashed selection box around it labeled '2'. A line connects the 'i\_Clock' block to a port labeled 'clk'. At the bottom, a 'Parameters - /HARDWARE/i\_Clock' window is open, showing a table of parameters. The 'division' and 'cycle' parameters are highlighted with a red box and labeled '4'. The 'Parameter Editor' tab is selected in the bottom toolbar, labeled '3'.

Name	Value	Configuration	Visibility	Editability
<b>Block properties</b>				
Name	i_Clock			
<b>Constructor Arguments</b>				
division	5	Default	Visible	Until Simulation Start
cycle	40	Default	Visible	Until Simulation Start



# Platform Architect

- ❖ Click Reset block -> Set reset period
  - ❖ `_ticks` -> 10

Parameters - /HARDWARE/i_Reset				
Name	Value	Configuration	Visibility	Editability
Block properties				
└ Name	i_Reset			
Constructor Arguments				
└ <code>_ticks</code>	10	Default	Visible	Until Simulation Start

# Platform Architect

## ❖ Run simulation



```
SystemC 2.3.1 --- May 12 2017 20:20:38  
Copyright 1996-2017 by all Contributors,  
ALL RIGHTS RESERVED
```

A	B	C	Y
6	9	115	169
1	15	74	89
12	9	205	313
10	11	242	352
11	3	70	103
12	2	84	108
8	11	232	320
7	13	118	209

```
SystemC: simulation stopped by user.
```

# Lab Requirement

- ❖ Due in one week (2023/05/10)
  - ❖ Complete MAC unit.
  - ❖ Use Platform Architecture to simulate output result.
  - ❖ Upload compressed file which include source codes ( all of your file, include PA project file, source code.... ) to E3@NYCU
    - File name rule: Student ID\_Lab1