Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring '2016-2017

Lab 1

Due date: 12 March 2017, Sunday, 23:59

1 Introduction

This laboratory aims to get you familiar with basic logic gates and combinational circuit design. You will simplify the circuit that is explained below and draw the circuit using Logisim tool with the given gates.

2 IC Pool

- 74LS00 (NAND)
- 74LS02 (NOR)
- 74LS04 (NOT)
- 74LS08 (AND)
- 74LS32 (OR)
- 74LS86 (XOR)

3 Lab Work

In this assignment, you are expected to perform the operations described in the following section.

3.1 Specifications

Suppose A and B are 2-bit binary input numbers and C is a 2-bit binary output number. Your circuit will take A and B and give the output C with the following instructions:

- C = A = B if A is equal to B.
- C = |A - B| otherwise.

Each 2-bit binary numbers A, B, and C are represented with A2, A1, B2, B1, C2, and C1 bits respectively where A2, B2, and C2 are the most significant bits and A1, B1, and C1 are the least significant bits of the relevant number. A2, A1, B2, and B1 are used as the input bits and C2 and C1 are used as the output bits.

You have to use "pins" for your inputs and outputs. Set their labels correctly using the following names. **Please, only set "label" property of the "pin" objects, do not add a "label" object in Logisim part.**

Input pins: A2, A1, B2, B1.
Output pins: C2, C1.

Each pin corresponds to a digit in a 2-bit binary number. If it is set, then the value of the digit is 1 if reset, then the value of the digit is 0.

3.2 Input Output Examples

1. Suppose A=01 and B=01. In this case, the input bits: A2=0, A1=1, B2=0, and B1=1. Since A is equal to B, the output C=01. Therefore, the output bits: C2=0 and C1=1.
2. Suppose A=11 and B=01. These numbers are given as inputs with A2=1, A1=1, B2=0, and B1=1 to the circuit. Since A is not equal to B, C is the absolute value of (A - B). The result is 10 which makes the output bits: C2=1 and C1=0.
3. Suppose A=00 and B=10. A2=0, A1=0, B2=1, and B1=0 are the representation of A and B as input bits. Since A is not equal to B, C = |A - B| = |00 - 10| = |-10| = 10. The output bits: C2=1 and C1=0.

4 Free Session

There will be a free session week after the week which the lab is announced. You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard by using IC components, and you will practice how to handle possible problems related to physical circuit.

5 Demo Session

There will be a 2-hour-long demo session week following the free session week. In demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard.
- You will show that the circuit drawn in Logisim works as specified.

6 Deliverables

1. Submit the circuit named `lab1.circ` prepared in Logisim, which is your preliminary work, via COW until the specified deadline. The evaluation of the submission will be a black-box test. **You should use CENG version of Logisim which is available on COW. Circuits designed with other tools or not named properly will not be graded!**

2. In demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in lab. Please note that submission of a working circuit is a must to attend DEMO lab sessions.

7 What to Bring in the Lab

- Print-out submitted file of the circuit.
- Lab materials and data-sheets of chips. www.alldatasheet.com
- Pencil and eraser, as you will have a quiz at the very beginning of the DEMO lab.

8 Cheating Policy

All the lab work should be individual and there is zero tolerance policy for cheating. See the course website for further information about cheating policy.

9 References

CENG Logism Version.