Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring 2016-2017

Lab Assignment 2

Due date: Sunday, March 26, 2017, 23:55hrs

1 Introduction

This laboratory aims to get you familiar with some of the most important IC components like multiplexers and decoders. You will draw the circuit using Logisim tool with the given gates.

2 IC Pool

- 74LS08 (AND)
- 74LS32 (OR)
- 74LS04 (Inverter)
- 74LS02 (NOR)
- 74LS00 (NAND)
- 74LS153 (Multiplexer)
- 74LS86 (XOR)
- 74LS138 (Decoder)

3 Lab Work

In this lab, you will be given three 2-bit numbers, A, B, S as input and you will produce the 3-bit output X. Requirements are given as follows:

- The digits of input "A" should be labelled as A1 and A0 where A0 is the least significant digit and A1 is the most significant digit.
- The digits of input "B" should be labelled as B1 and B0 where B0 is the least significant digit and B1 is the most significant digit.
- The digits of input "S" should be labelled as S1 and S0 where S0 is the least significant digit and S1 is the most significant digit.
- Your output X is a 3-bit number which should be labelled as X2, X1 and X0 where X0 is the least significant digit and X2 is the most significant digit.
- You are expected to perform the following 4 tasks depending on the value of S:
  - If S is 0 the output will be 6.
  - If S is 1 the output will be 2*A.
  - If S is 2 the output will be 2*B+1.
  - If S is 3 the output will be A+B.

4 Free Session

There will be a free session week after your homework is announced. You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard by using IC components, and you will practice how to handle possible problems related to physical circuit.

5 Demo Session

There will be a 2-hour-long demo session week following the free session week. In demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard.
- You will show that the circuit drawn in Logisim works as specified.

6 Labelling Specifications

- You have to use "pins" for your inputs and outputs. Only set "label" property of the "pin" objects, do not add a "label" object.
- Your input pins should be labelled as A1, A0, B1, B0, S1 and S0.
- Label properties are case-sensitive. Note that all labels consist of an uppercase letter followed by a number. Please be very careful on correct naming of labels.
- Your output pins should be labelled as X2, X1 and X0.
- If you need to feed any input with a constant value, you can use a constant gate. This gate is under CENG232 gates. We will only set values for A1, A0, B1, B0, S1 and S0.

7 Deliverables

1. Submit the circuit named **lab2.circ** prepared in Logisim, which is your preliminary work, via COW until the specified deadline. The evaluation of the submission will be a black-box test.
2. In demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in lab.
   Submission of a working circuit is a must to attend DEMO lab sessions. **You should use CENG version of Logisim which is available on COW. Circuits designed with other tools or not named properly will not be graded!**

8 What to Bring in the Lab

- Print-out of submitted file of the circuit.
- Chips and their data-sheets. www.alldatasheet.com
- Pencil, as you will have a quiz at the very beginning of the DEMO lab.

9 Cheating Policy

All the lab work should be individual and there is zero tolerance policy for cheating. See the course website for further information about cheating policy.

10 References

CENG Logisim Version