

# Audio Amplifier Design

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**Abstract**— This report presents the design, analysis, and implementation of an audio amplifier with specific performance criteria, including a gain of 500, an input signal range of 10–20 mV peak-to-peak, and an output power of 1.5 W within the audible frequency range (20 Hz–20 kHz). The system consists of multiple stages, including a pre-amplifier, gain stage, filter stage, and a class AB power amplifier.

**Keywords**— Audio Amplifier, Pre-Amplifier, Common-Emitter Amplifier, Gain Stage, Band-Pass Filter, Class AB Amplifier, Total Harmonic Distortion (THD), Slew Rate, Signal Processing, Noise Reduction, Frequency Response, Power Amplification, Circuit Design, Distortion Analysis, High-Gain Amplifier

## I. INTRODUCTION

Audio amplification is a fundamental aspect of signal processing in various electronic applications, including communication systems, music playback devices, and public address systems. The objective of this project is to design and implement a high-gain audio amplifier capable of amplifying small input signals while preserving audio quality and minimizing distortion.

The amplifier consists of four key stages:

1. Pre-Amplifier Stage- A common-emitter differential amplifier is used to amplify the input signal while maintaining high input impedance and low noise.
2. Gain Stage- A common-emitter amplifier configuration provides the necessary voltage amplification to achieve the desired overall gain of 500.
3. Filter Stage- An active band-pass filter is employed to restrict the signal within the audible frequency range and eliminate unwanted components.
4. Power Amplifier Stage- A class AB amplifier is chosen to deliver sufficient output power to the load while minimizing distortion and maximizing efficiency.

Key performance parameters, including total harmonic distortion (THD) and slew rate. The implementation of resistive-capacitive (RC) filters helps in reducing unwanted harmonics, thereby improving the audio quality.

We have decided to get a gain of 5 from the first stage and a gain of 33–35 from the gain stage. We could achieve this in LTSpice, however, due to the change in the values of the components based on availability in the lab and to ensure impedance matching, we got a gain of 430 – 450 (mentioned a range as the resistor and capacitor values fluctuate) which was accepted by the Tas. Also, the -3dB frequency of the

bode plot correspond to the 20Hz and 20kHz cutoff frequencies.

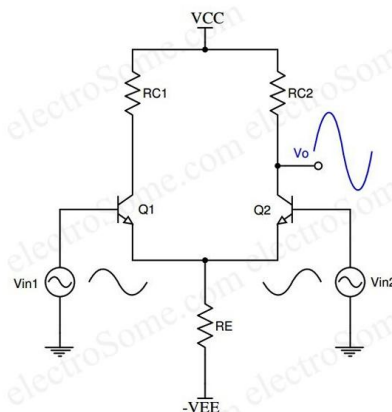
1. Supply Voltage = -5 to 5 V
2. Input small signal voltage = 10–20 mV peak-to-peak
3. Gain =  $G_1 \times G_2 \geq 500$  (Pre-amp and Gain stage)
4. Frequency = Audible Range (20 Hz to 20 kHz)
5. Power  $\geq 1.5$  W
6. Filter **should not** attenuate the input signal
7. Power Amplifier **should not** provide voltage gain
8. Load = 10  $\Omega$

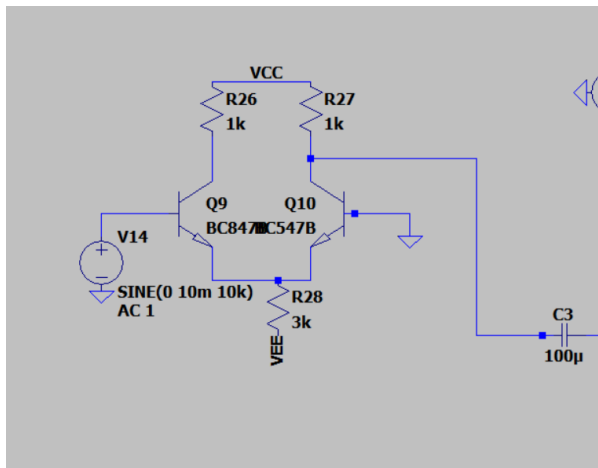
## II. PRE-AMPLIFIER STAGE

The pre-amplifier stage is essential for initial signal amplification. The common-emitter differential amplifier is used due to its high input and low output impedance, along with good noise performance. The input can be applied to either transistor's base, with the choice of either grounding the other transistor's base or applying an equal and opposite input, effectively doubling the amplification.

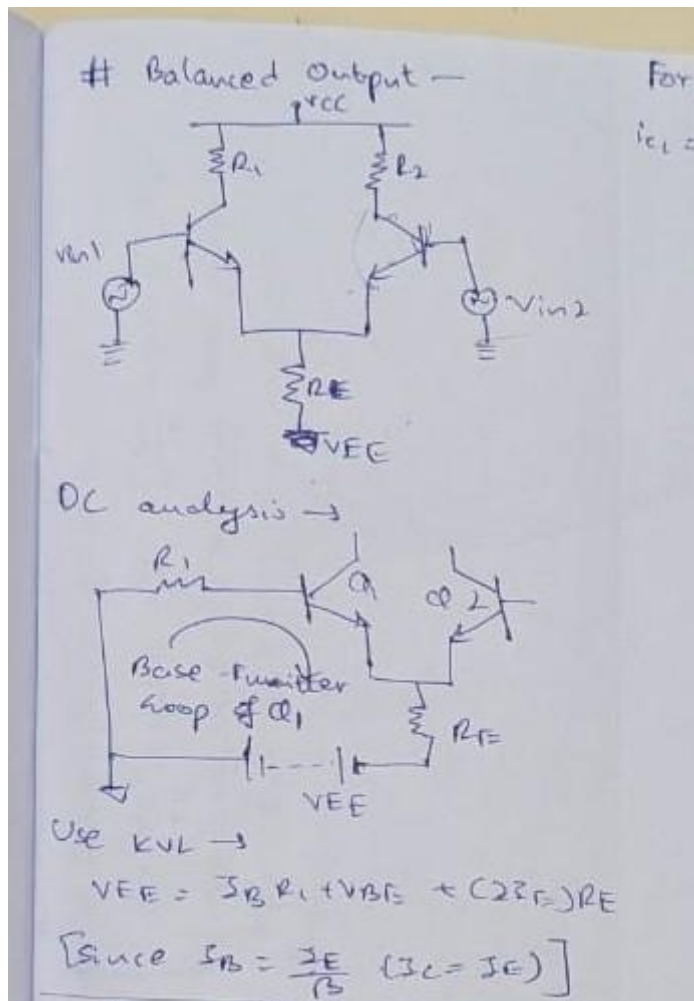
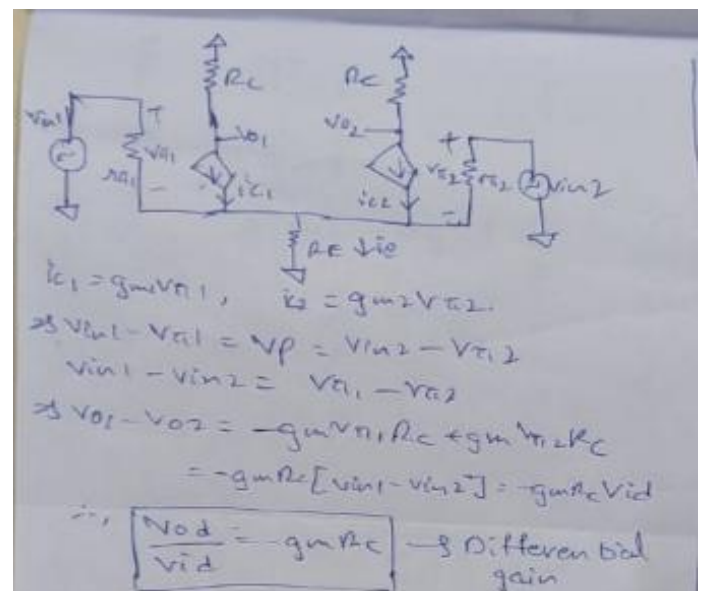
The biasing ensures that the two NPN BJTs remain in active mode- Base-Emitter junction: Forward bias and Base-Collector junction: Reverse bias. The input can be applied to either transistor's base with the choice of either grounding the other transistor's base or applying an equal and opposite input to the other transistor's base (effectively twice amplification). In this case, a resistor is used instead of an independent current is the current that flows through it.

### A. Circuit Diagram





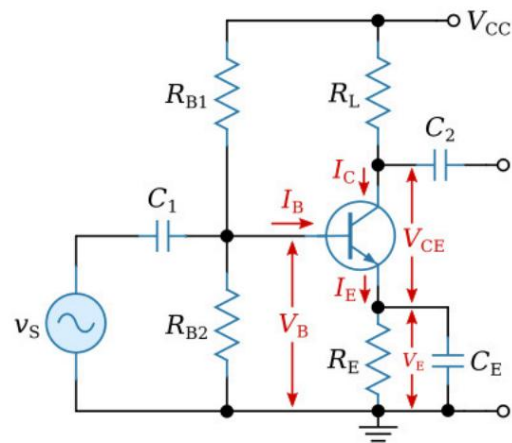
## B. Small Signal Analysis



### C. Calculations

$gain = g_m R_E = \frac{I_C R_E}{V_T}$ ,  $I_C = 375 \mu A - 400 \mu A$   
 We would like to get a gain of 15 with this stage  
 $\Rightarrow 15 = \frac{375 \times 10^{-6} R_E}{25 \times 10^{-3}}$   $R_E = 1 K \Omega$   
 $R_E = \frac{V_{CC} - V_{BE}}{2 I_E} \Rightarrow R_E = \frac{5 - 0.7}{2 \times 375 \times 10^{-6}} = 5.3 K \Omega$   
 But with adjustments and to match impedance, we choose  $R_E = 3 K \Omega$  in hardware.

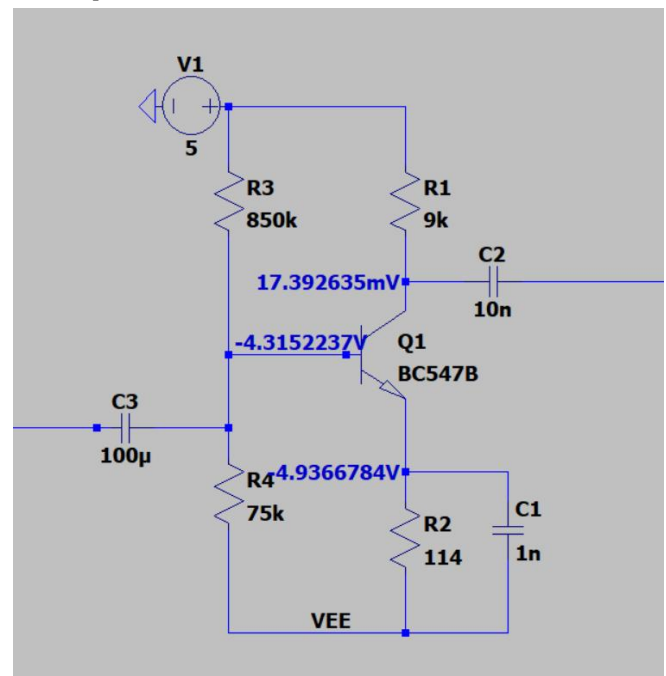
### A. Circuit Diagram



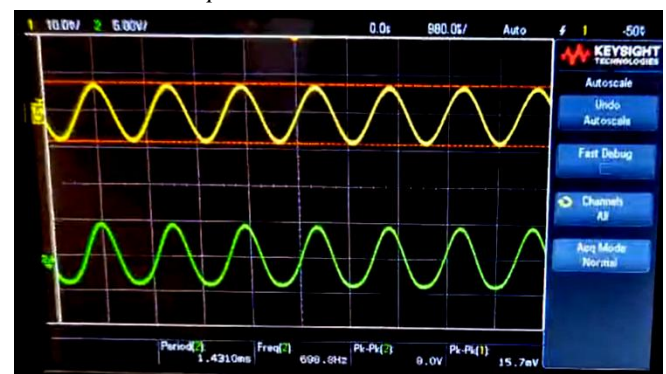
### D. Observations

- We have decided to get a gain of and the majority of the gain from the next stage.
- We ensure that  $R_{C1}$  and  $R_{C2}$  are symmetric so that when both input are given, the noise gets cancelled from the differential output. But if we give only 1 input, then we ensure that  $A_{cm} < 1$  and fix the values of the components.
- Thus, the pre amplifier is used to remove the noise and amplify the input for the next stages.
- The capacitor after the pre amp stage acts like an AC coupling capacitance to block the DC from the incoming signal and send the AC signal to the gain stage.
- The current source has been replaced by emitter resistance.
- Pre-amplifier matches the impedance of input impedance of power amplifier and the input impedance of the mic.
- Differential amplifiers amplify the difference between two input signals rejecting common mode signals arising from electromagnetic interference and radio frequency interference and power supply noise.
- Both Single Input Balanced Output (SISO) and Dual Input Balanced Output have been analyzed.

### B. LTSpice



### C. Hardware Output



### III. COMMON EMITTER AMPLIFIER

This is the second stage of the amplifier. It is very important to amplify the input signal. It provides the major part of the gain required.

A common emitter configuration is preferred because of its input impedance and low output impedance.

Here we use a Class AB Amplifier rather than Class A or Class B ones to increase power efficiency and eliminate crossover distortion (since it conducts between 180-360 degrees).

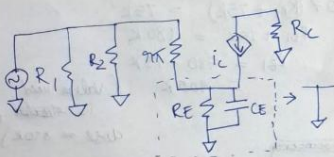


## D. Small Signal Analysis

COMMON EMITTER AMPLIFIER CALCULATIONS.

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

$$V_{BE} = \left( \frac{R_{B2}}{R_{B1} + R_{B2}} \right) V_{CC}$$

$$V_{CC} = +5 - (-5) = 10V$$


Capacitors get shorted in SS4 models and voltage sources grounded so,  $R_E \rightarrow 0$

$$Z_{IN} = R_1 \parallel R_2 \parallel \beta \pi (1 + g_m R_E)$$

$$g_m \pi = -\frac{V_o}{V_i} \Rightarrow V_o = -g_m V_i R_C$$

$$V_{in} = V_i + V_e$$

$$= V_i + I_E R_E = V_i + (I_B + I_C) R_E$$

$$= V_i + \frac{V_i}{\beta \pi} R_E + R_E g_m V_i$$

$$\frac{V_o}{V_{in}} = \frac{-g_m R_C}{1 + \left( \frac{1}{\beta \pi} + g_m R_E \right) R_E} = -g_m R_C \quad \beta \pi = \frac{\beta}{g_m} \quad R_E \rightarrow 0$$

## E. Calculations

Deriving values for the gain circuit,

Assume  $I_C \approx I_E = \frac{1.1 \times 10^{-3}}{2} A$

$V_{BE}$  must be also be close to zero but above cutoff for the transistor to be on so assume  $V_{BE} = 0.7V$

Taking  $R_{B2}$  to be 75K,

Calculating  $R_{B1}$ ,

$$V_{BE} = \left( \frac{R_{B2}}{R_{B1} + R_{B2}} \right) V_{CC}$$

$$0.7 = \left( \frac{75K}{R_{B1} + 75K} \right) 10$$

$$0.07 = \frac{75K}{R_{B1} + 75K}$$

$$0.07(R_{B1} + 75K) = 75K$$

$$R_{B1} + 75K = 980K$$

$$R_{B1} = 980 - 75K = 905K$$

(Value used is ~~905K~~ pretty close  $\approx 850K$ )

~~Assuming~~

The Voltage at the collector must be as close as possible to ~~the average~~ half of the supply voltage  $\pi$  to achieve max gain

Here its divided as +5 and -5, so it must be close to 0.

Assuming  $V_C \approx 0$ , we can calculate  $R_C$

$$5 - I_C R_C = 0$$

$$5 = \frac{1.1 \times 10^{-3}}{2} R_C$$

$$R_C = \frac{5000 \times 2}{1.1} \approx 9K \Omega$$

Finally, wing.

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

$$10 - I_C (R_C + R_E) - 5 = 0$$

$$\frac{1.1 \times 10^{-3}}{2} = \frac{5}{(9K + R_E)}$$

$$(9K + R_E) = \frac{10K}{1.1}$$

$$9K + R_E = 9099K$$

$$R_E \approx 99K \Omega$$

(Used value is 114K)

Slight variation in values as due to the next and previous stages' impedances.

$C_1$  must be large enough to block DC components  $\approx 100\mu$

$R_C$  introduces a pole.  $C_2$  must be chosen carefully to ensure sig. till 20K get transmitted but no further, so  $\frac{1}{2\pi R_C C_2} \leq 20K$  so  $C_2 \approx 10nF$

$R_{B1}$  introduces another pole  $\frac{1}{2\pi R_{B1} C_1} \geq 20$ , so  $C_1 \approx 1nF$

## F. Observations

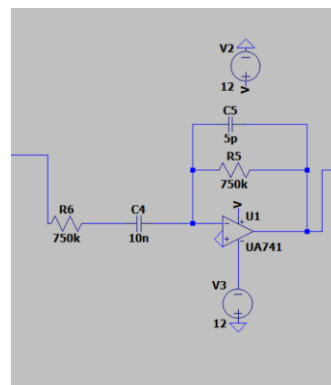
The input capacitor  $C_1$  blocks the DC components of the input signal and contributes a pole to the system.

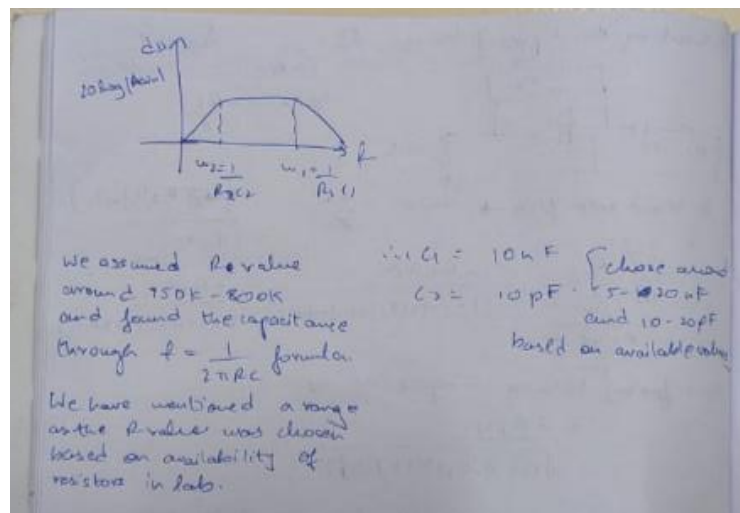
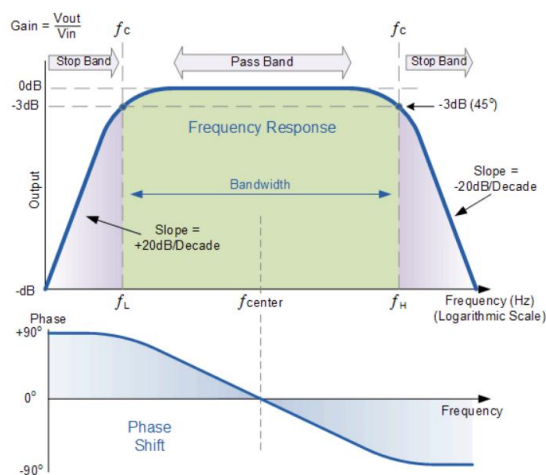
$C_e$  serves to block DC current flowing to ground. It provides the second pole to the system and provides AC coupling to the filtering stage.  $R_{B1}$  and  $R_{B2}$  are bias resistors, which form a voltage divider. This is used to bias the transistor (Base-emitter junction in forward bias and Base-Collector junction in negative bias).

$R_E$  mainly provides negative feedback to stabilize gain

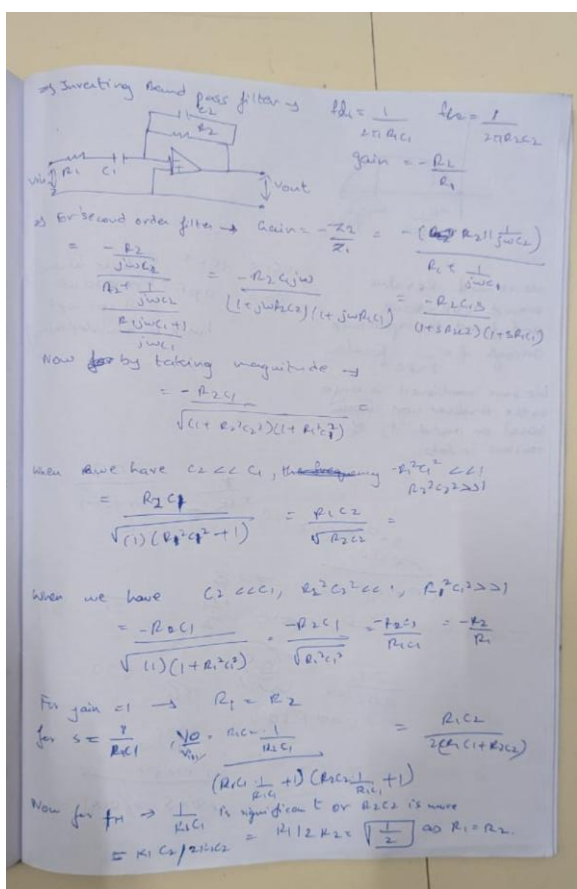
## IV. FILTER STAGE

Due to amplification the noise in the signal also gets amplified, so we use a bandpass filter. Human audible range is around 20Hz to 20kHz and our filter also has these cutoffs to eliminate the noise. Using a filter after gain stage leads to better recorded frequency response which is not interfered by any amplification of gain stage. We used an active filter because OpAmp takes high impedance input and gives low impedance output. OpAmp also helps in impedance matching of the input of mic to the power amplifier stage. Objective of unity gain can be achieved by using OpAmp thus not affecting the frequency ranges of the output thereby restricting them to the audio range.





## A. Derivations and calculations



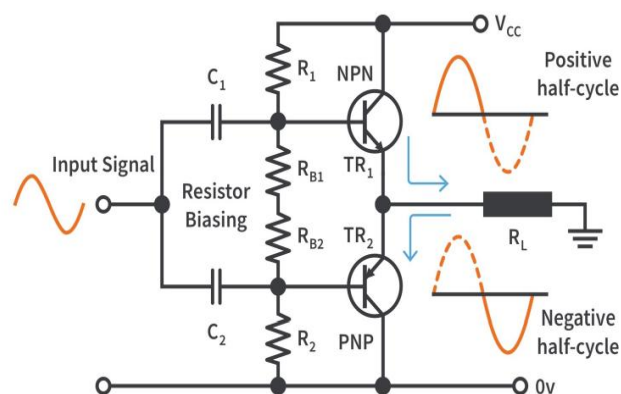
## V. POWER AMPLIFIER

A power amplifier **amplifies low-power electronic audio signals**. This is the fourth and final stage of the amplifier.

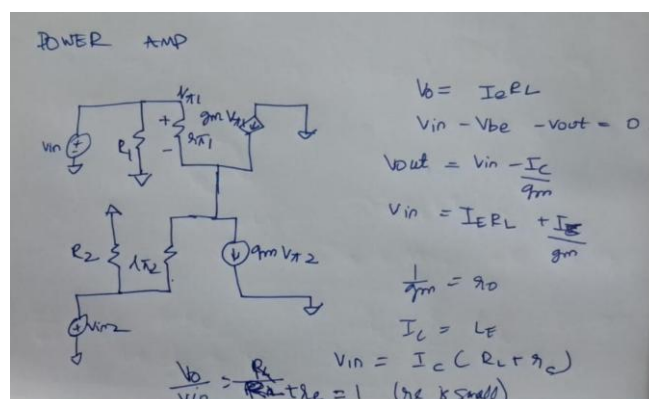
The previous stages took care of the Voltage amplification but there must be a minimum value of current to be able to drive the speaker. This stage does mainly that. There's no Voltage gain only Current gain here.

Here we use a Class AB Amplifier rather than Class A or Class B ones to increase power efficiency and eliminate crossover distortion (since it conducts between 180-360 degrees).

### A. Circuit Diagram

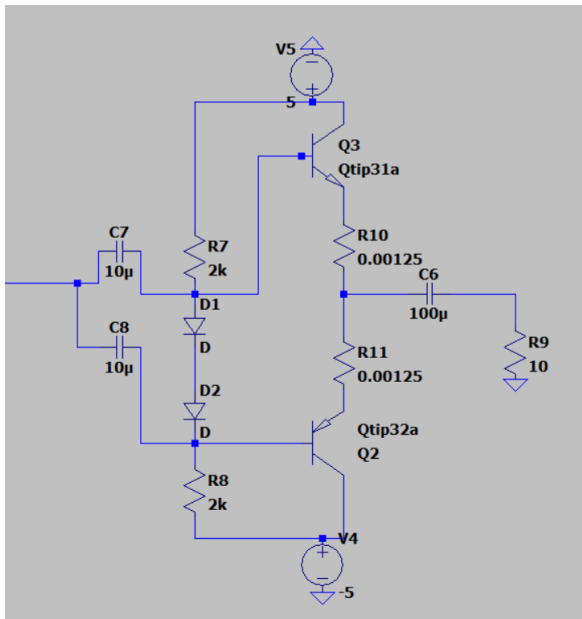


### B. Derivation

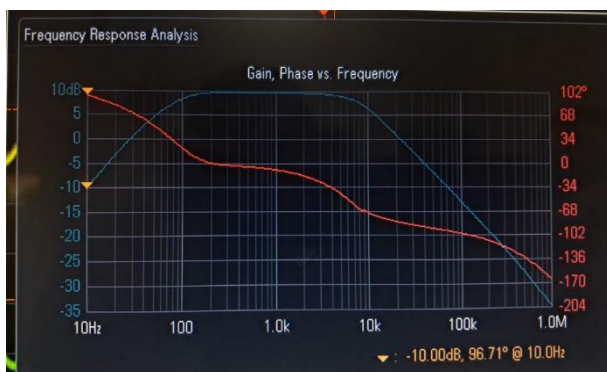




### C. LTSpice



### D. Hardware Output



BODE PLOT AFTER POWER AMP

### E. Observations

The function of the resistors is to bias the transistors in such a way that the amount of signal passing through is slightly more than half cycle (preventing crossover distortion). By setting Bias resistors to be equal, we prevent Voltage gain.

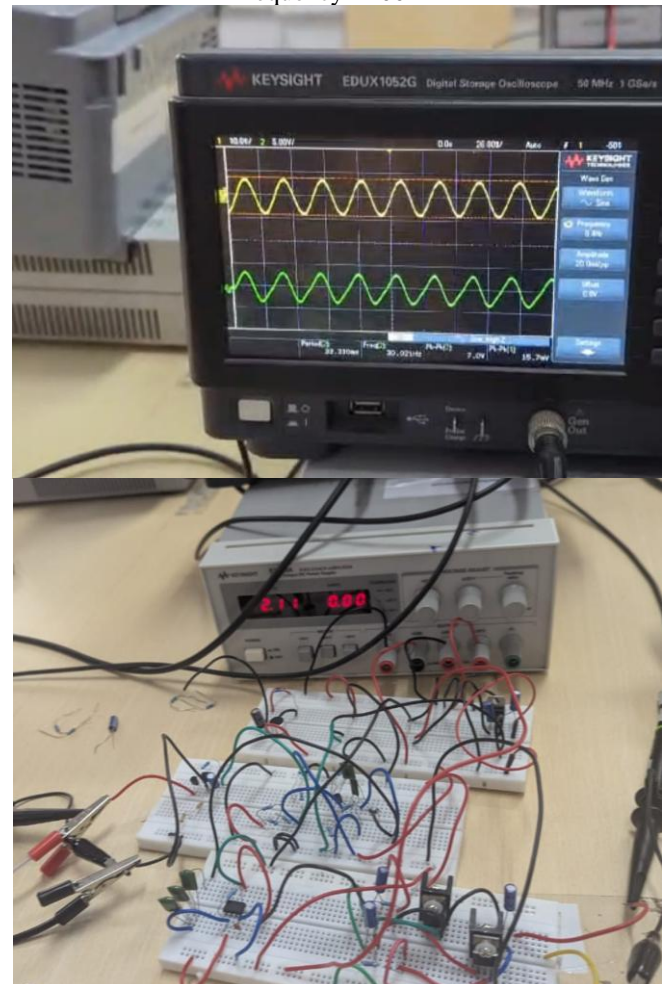
The capacitors are used to minimize the base current for both the transistors which will increase current gain therefore increasing power gain.

### VI. HARDWARE PICTURES COMBINED

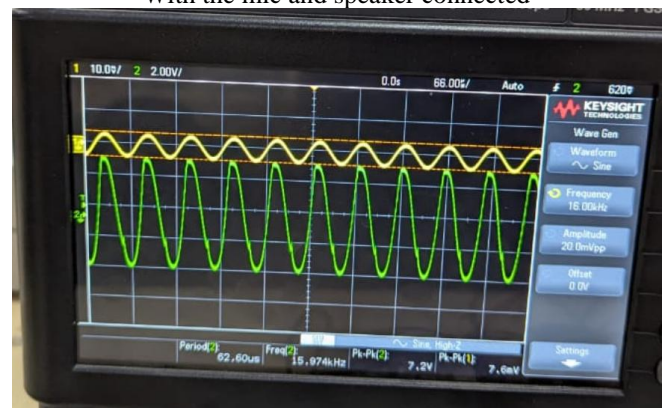
Frequency- 10k Hz

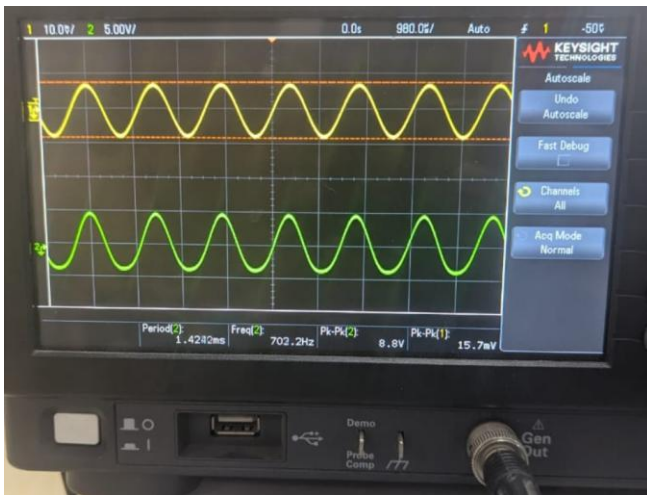


Frequency- 100 Hz

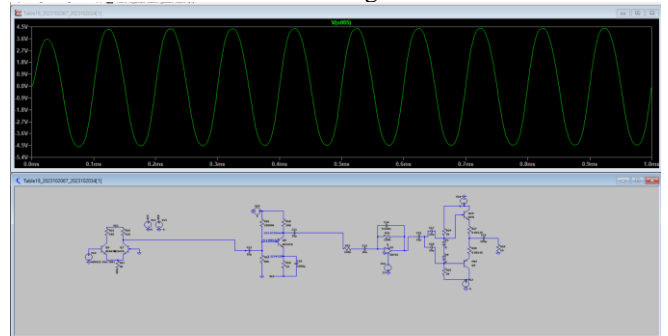


With the mic and speaker connected-

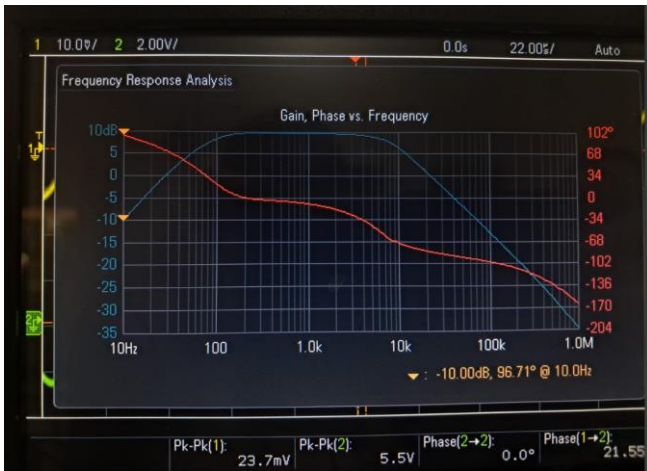
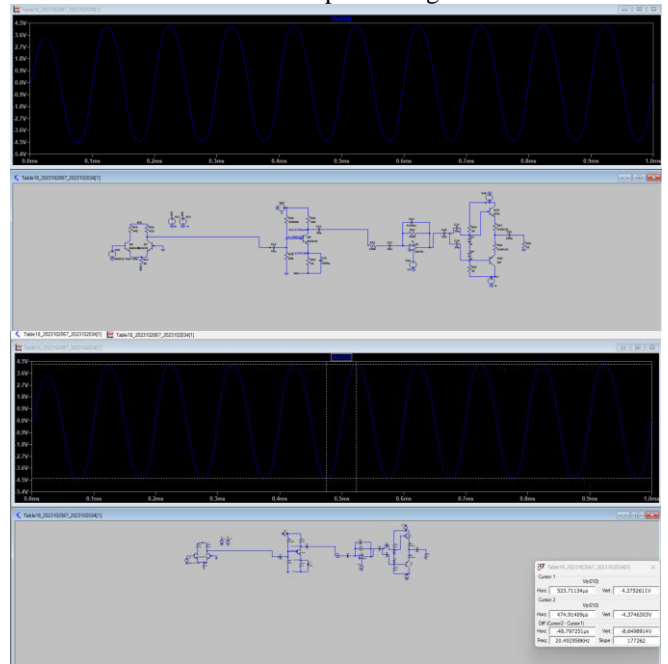




Filter stage-

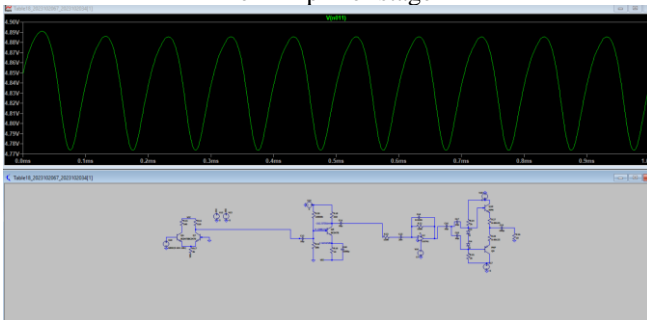


Power Amplifier stage-

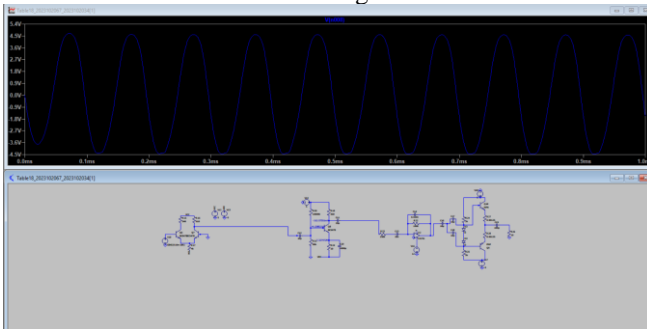


## VII. LTSPICE

Pre- Amplifier stage-

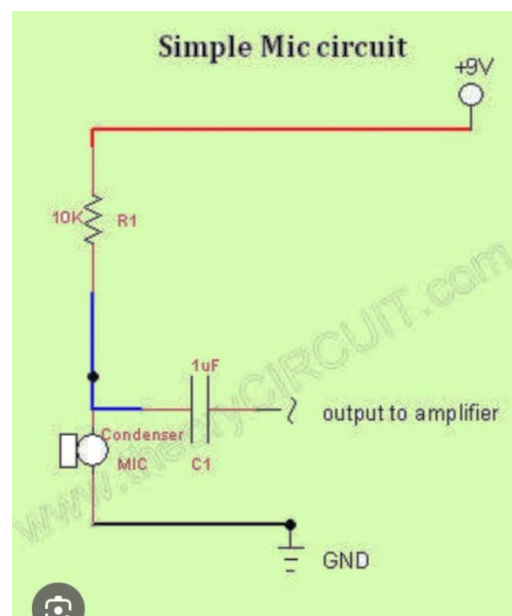


Gain stage-



## VIII. MIC AND SPEAKER

To test the circuit out with actual sounds, we attach a mic to the base of the preamp and we remove the output resistor of power amp and connect the speaker.



## IX. PHASE SHIFT AND BUFFER

We observe the following phase shifts-  $0^\circ$  for preamp,  $180^\circ$  for gain,  $180^\circ$  for the inverted active bandpass filter and  $0^\circ$  for the power amplifier.

The buffer has the property of high input impedance and low output impedance that is generally used for impedance matching.

## X. SLEW RATE

Slew rate (S.R) is the maximum rate at which the output voltage of an amplifier can change with time.

$$S.R. = \max(dV_{out} / dt)$$

- A higher slew rate means the amplifier can handle rapid voltage changes efficiently, which is important for high-frequency signals.
- If the slew rate is too low, the output cannot keep up with fast input transitions, leading to slew-induced distortion—where the output waveform appears stretched and lags the input.
- Ways to increase slew rate include increasing the maximum operating voltage, reduce capacitive impedance in subcircuits and allowing operation at higher frequencies.

$$S = 2\pi f V_m$$

## XI. DISTORTION ANALYSIS

Distortion in an amplifier occurs when unwanted harmonic content is added to the signal. This is quantified using Total Harmonic Distortion (THD).

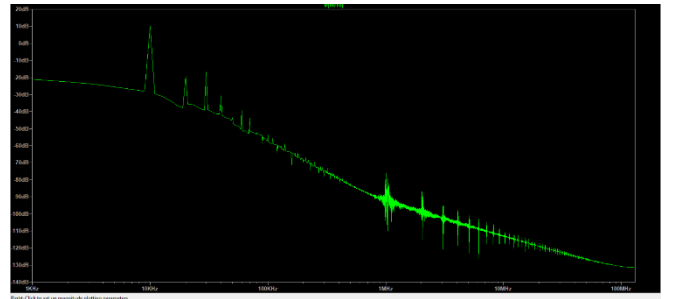
$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_RMS}^2}}{V_{f\_RMS}}$$

- $THD$  is the total harmonic distortion present in the signal
- $V_{n\_RMS}$  is the RMS voltage of the nth harmonic
- $V_{f\_RMS}$  is the RMS voltage of the fundamental frequency

High THD causes distortion, leading to a poor-quality output signal. Low THD ensures faithful reproduction of the input signal. The FFT (Fast Fourier Transform) of a sine wave in the system can help identify and quantify harmonics. We can improve THD by minimizing circuit interference. We can use low-pass filters to remove unwanted harmonics. For an audio amplifier, controlling distortion is crucial because distortion alters the sound quality. Ensuring a low THD and a high slew rate will help maintain clear and accurate audio output.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+4	4.545e+0	1.000e+0	89.53°	0.00°
2	2.000e+4	1.692e-1	3.723e-2	76.66°	-12.87°
3	3.000e+4	2.165e-1	4.764e-2	93.29°	3.76°
4	4.000e+4	4.117e-2	9.057e-3	46.62°	-42.91°
5	5.000e+4	9.428e-3	2.074e-3	-139.99°	-229.52°
6	6.000e+4	1.176e-2	2.588e-3	-45.25°	-134.79°
7	7.000e+4	6.930e-3	1.525e-3	8.84°	-80.69°
8	8.000e+4	4.899e-3	1.078e-3	103.05°	13.52°
9	9.000e+4	3.234e-3	7.114e-4	-173.91°	-263.44°

Partial Harmonic Distortion: 6.125392%  
Total Harmonic Distortion: 6.125710%



## ACKNOWLEDGMENT

We thank the professors and the Tas for constant support and guidance throughout the course of the project.