Lab 1 : testbench development basics for nibble CPU DUT

Objective

To understand DUT specification, design and RTL

To develop a simple testbench to verify basic operations for nibble CPU DUT

To understand how to instantiate DUT in testbench

To generate stimulus to DUT to perform add and multiplication operation

Tasks

1. Read DUT specification thoroughly and understand its operation

2. Create testbench.v file

3. Generate appropriate clock and reset

4. Create memory_model.v and write 4096x32 SRAM model

5. Instantiate DUT and memory model in testbench and make appropriate connections

6. Generate stimulus to DUT : program CPU to perform add and multiply operation

7. Verify result by reading correct memory location, print opcode, operand and result in decimal format

8. Verify important interface signals in waveform, add markers/text as needed In snapshot

Setting up , Compiling and Running simulations with Questa

csh
source /home/mentor/test.cshrc
vlog -64 +acc testbench.v memory_model.v serial_interface.sv output_serializer.sv done_generator.sv cpu_top.sv cmd_controller.sv
vsim -64 testbench -do “log -r *; run -all”

Output files : waveform and logfile: vsim.wlf, transcript

Refer questa documents to understand tool in detail

Deliverable

1. testbench.v

2. logfile

3. Report with waveform snapshot, explain complete sequence of operation