Lab Report

LAB — 02 CSE — 206

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CSE — 206

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LAB-02

Name of the experiment: Implementation of basic logic gates using universal gates.(NAND and NOR).

NAND Gate:

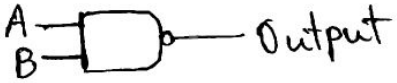
Equipments:

(i) Proteus Software.
(ii) NAND Gate (7400).
(iii) LOGICPROBE (BIG).
(iv) LOGICSTATE.

Description:

The NAND gate represents the complement of the AND operation. It's name is an abbreviation of NOT AND. It has the following truth table.

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



To create other basic gates from NAND:

AND Gate = (A NAND B) NAND (A NAND B)

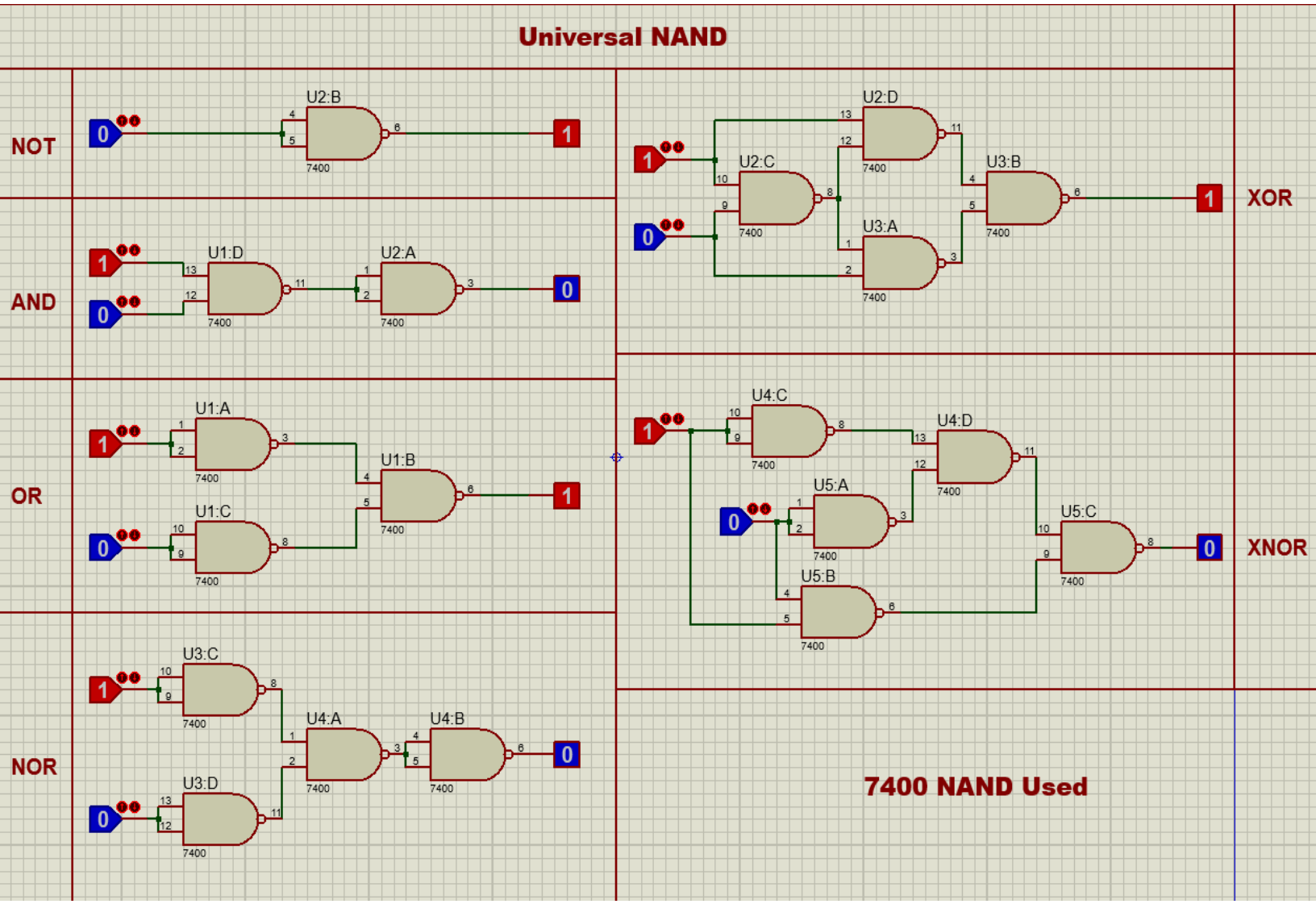
OR Gate = (A NAND A) NAND (B NAND B)

NOT Gate = A NAND A

X-OR Gate = [A NAND (A NAND B)] NAND
[B NAND (A NAND B)]

NOR Gate = [(A NAND A) NAND (B NAND B)] NAND
[(A NAND A) NAND (B NAND B)]

X-NOR Gate = {[A NAND (A NAND B)] NAND
[B NAND (A NAND B)]} NAND
{[A NAND (A NAND B)] NAND
[B NAND (A NAND B)]}


Universal NAND
NOT
AND
OR
NOR
XOR
XNOR
U2:B
U1:D
U2:A
U1:A
U1:B
U1:C
U3:C
U4:A
U4:B
U3:D
U2:D
U2:C
U3:B
U3:A
U4:C
U4:D
U5:A
U5:C
U5:B
7400
7400 NAND Used

NOR Gate:

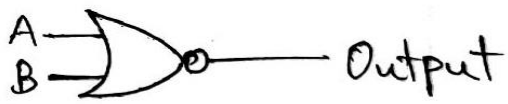
Equipments:

(i) Proteus Software.
(ii) NOR Gate (NOR)
(iii) LOGICPROBE
(iv) LOGICSTATE

Description:

The NOR gate represents the complement of the OR operation. Its ~~name~~ name is an abbreviation of NOT OR. It has the following truth table:

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



A NOR gate is a universal gate. So, other basic gates can be represented as a combination of NOR gates:

AND = (A NOR A) NOR (B NOR B)

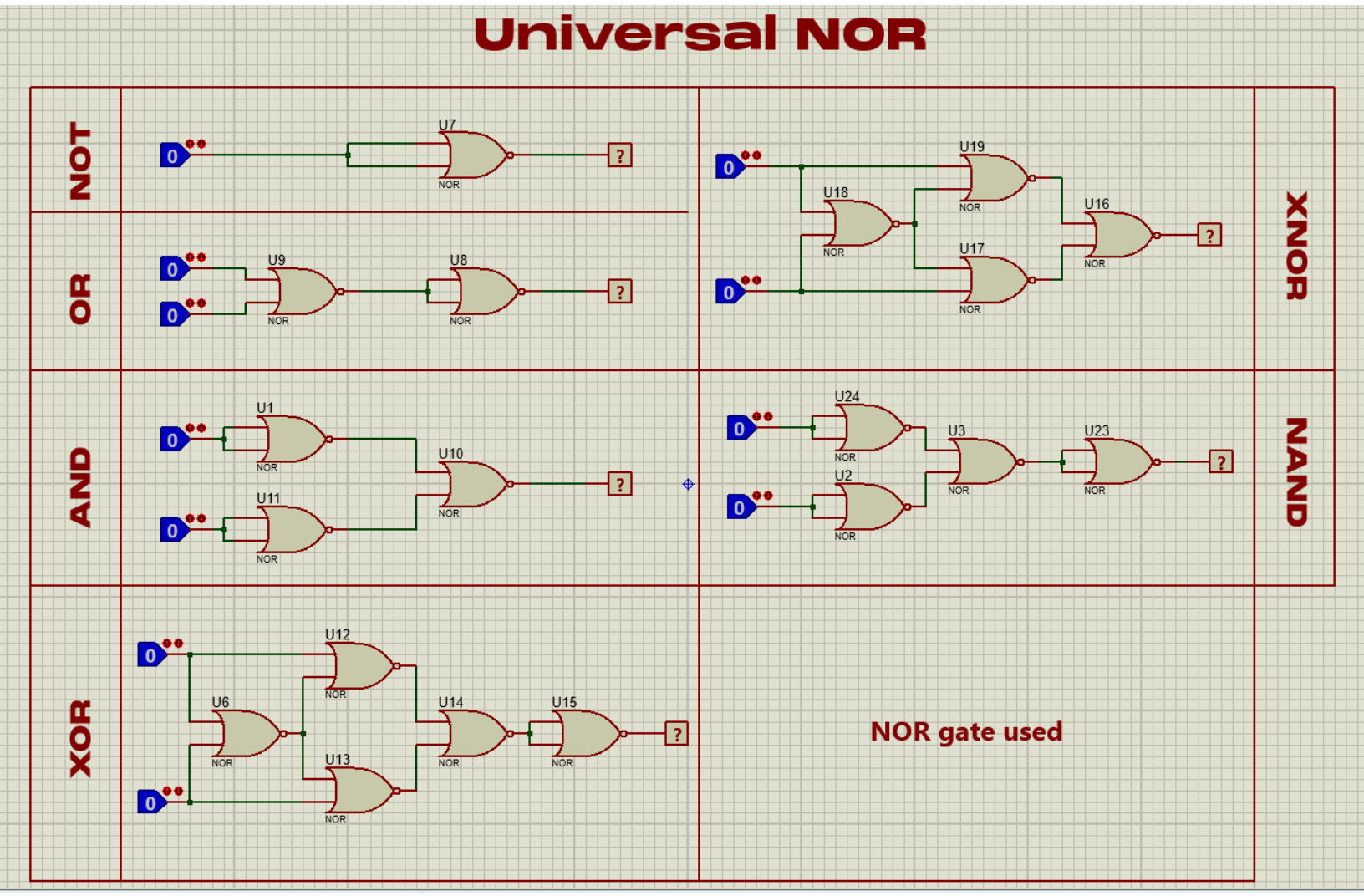
OR = (A NOR B) NOR (A NOR B)

NOT = A NOR A

XOR = (A NOR A) NOR (B NOR B) NOR (A NOR B)

NAND = [(A NOR A) NOR (B NOR B)] NOR [(A NOR A) NOR (B NOR B)]

XNOR = [A NOR (A NOR B)] NOR [B NOR (A NOR B)]



Conclusion:

(i) We have learnt how to implement basic gates from universal gates.

(ii) We have learnt what is NAND and what is NOR.

(iii) We understood the NAND and NOR gates to build up basic gates

(iv) We got two types of variant of each gates from NAND and NOR.

(v) We have also learnt how to implement circuits in Proteus Software.

THE END