Lab Report

LAB — 01 CSE — 206

Presented By:

- **Name:** Tunazzinur Rahman Kabbo
- **Intake:** 44
- **Sec:** 07
- **ID:** 19202103268

Presented To:

❖ **Iffat Tamanna**
Lecturer, BUBT
Department of Computer Science & Engineering
Email: iffat@bubt.edu.bd

LAB-01

Name of the experiment: To verify the behaviorr of logic gates using truth table and implementation of all basic logic gates using Proteus.

Equipments:

(i) Proteus Software.
(ii) And Gate (7408)
(iii) OR Gate (7432)
(iv) NOT Gate (7404)
(V) NAND Gate (7400)
(vi) NOR Geate (7402)
(vii) XOR Gate (XOR)
(viii) XNOR Gate (4077)
(ix) Logic Probe.
(X) Logic State

Description:

Logic gates are like devices that acts as a building block for digital circuits. They perform basic logical functions that are fundamental to digital circuits. Most electronic devices we use today will have some from of logic gates in them. For example, logic gates can be used in technologies such as smartphones etc. Logic gates are based on Boolean Algebra (0 and 1).

Truth Table:

AND Geate

⇒ A • B

Output

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

Input

OR Gate

=> $A+B$

		Output
A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

Input

NOT Gate

=> $\bar{A}$

Input	Output
A	$\bar{A}$
0	1
1	0

NAND Gate

=> $\overline{A.B}$

			Output
A	B	$A.B$	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Input

NOR Gate

=> $\overline{A+B}$

Output

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Input

XOR Gate

=> $A \oplus B$

$= (A+B).(\bar{A}+\bar{B})$

Output

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Input

XNOR Gate

=> $A \odot B$

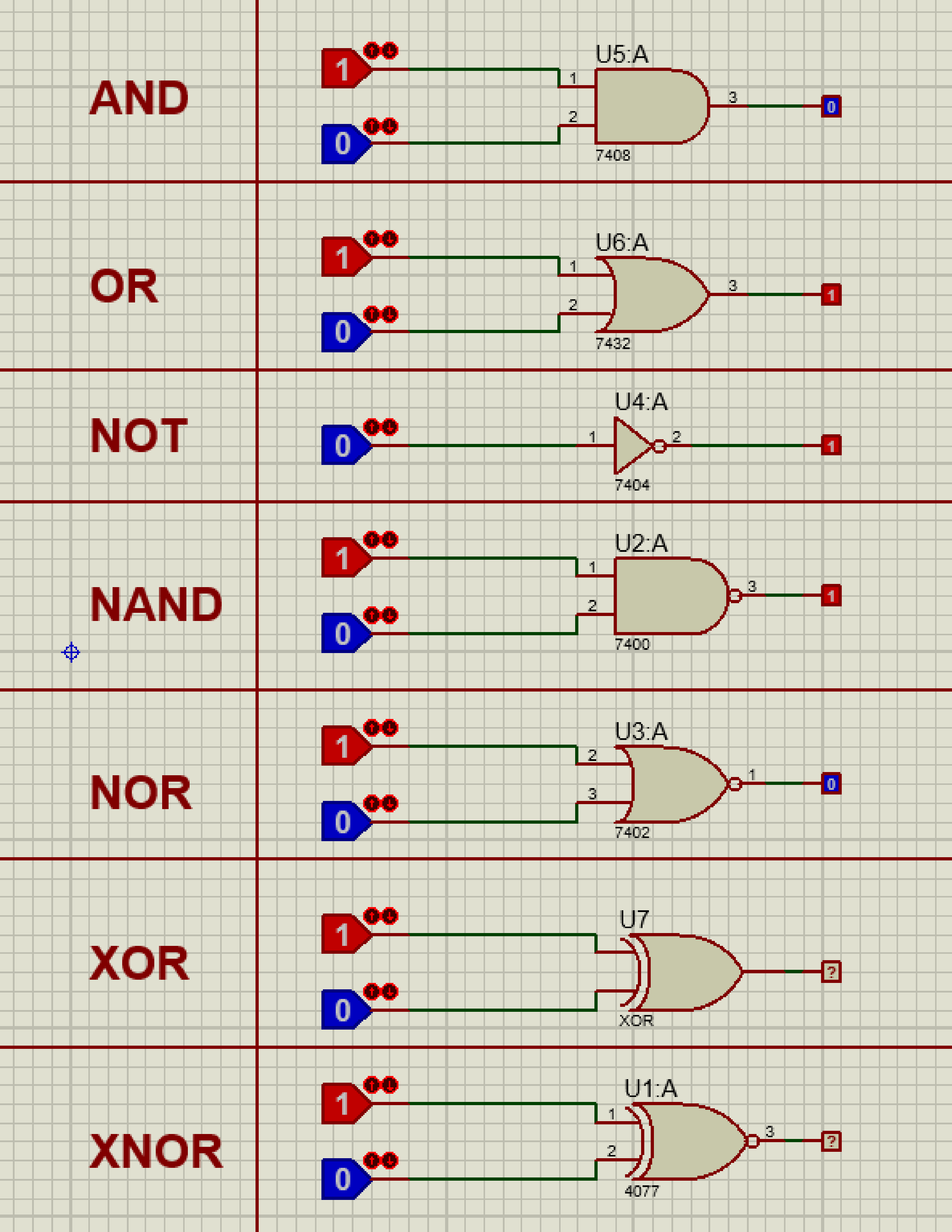
$= \overline{A \oplus B}$

$= (\bar{A}+B).(A+\bar{B})$

Output

A	B	$A \oplus B$	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Input


AND
1
0
U5:A
1
2
3
7408
0
OR
1
0
U6:A
1
2
3
7432
1
NOT
0
U4:A
1
2
7404
1
NAND
1
0
U2:A
1
2
3
7400
1
NOR
1
0
U3:A
2
3
1
7402
0
XOR
1
0
U7
XOR
?
XNOR
1
0
U1:A
1
2
3
4077
?

Conclusion:

(i) We have learnt how to implement circuits in Proteus Software.

(ii) We have understood the digit simulation of any circuit in the software.

(iii) we have verified the truth table for each input/output combination.

(iv) We repeated the process for all other logic gates.

THE END