

**CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY (CHARUSAT),
CHANGA – 388 421**

Chandubhai S. Patel Institute of Technology

V .T. Patel Department of Electronics and Communications Engineering

Report for Expert Talk

Date: 01-09-2023

Date: September 1, 2023

No.of Participants:45

Organized by: Mrs. Arpita P. Patel

ResourcePerson: Mr.Jaydeep Padariya,Parth Ardesana,Prerak Dalia and Nilay soni

Type: Expert talk

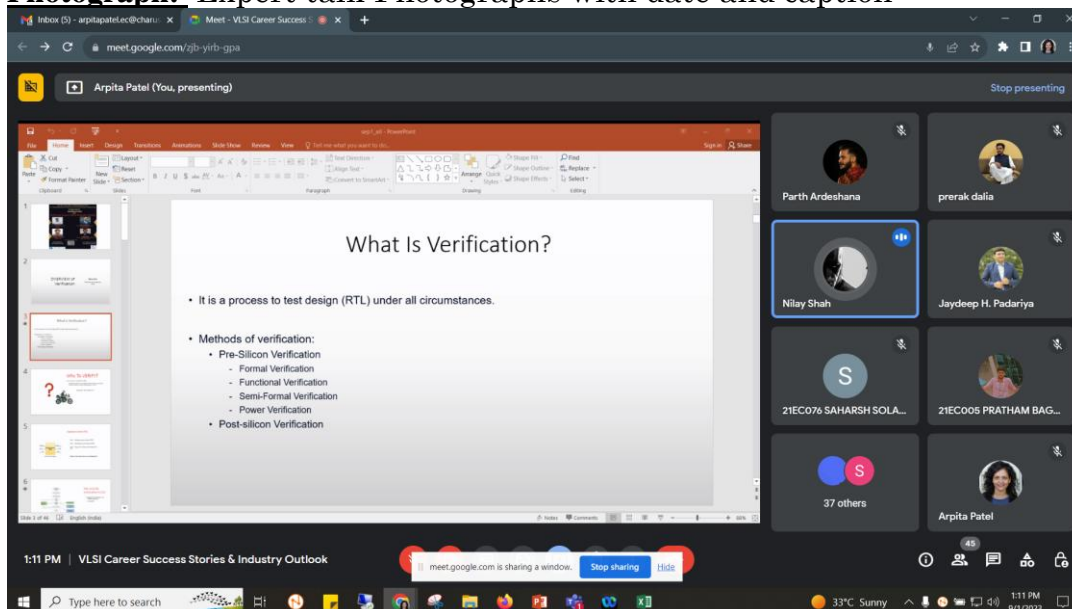
Title: VLSI Career Success Stories & Industry Outlook

Date and Time: 01-09-2023, 01:00 AM to 3:30 pm. (2.50Hours),

Summary/Topics covered in Expert Talk:

- Introduction to ASIC flow, Journey of a chip
- Job opportunities for PD, DFT and verification engineer
- Overview of verification, Pre silicon verification flow

Photograph: Expert talk Photographs with date and caption



Inbox (5) - arpitapatel@chanu... Meet - VLSI Career Success meet.google.com/gjb-yirb-gpa

Arpita Patel (You, presenting) Stop presenting

2:03 PM | VLSI Career Success Stories & Industry Outlook

33°C Sunny 2:03 PM 9/1/2023

Career Opportunity

Design Engineer
A design engineer is responsible for creating the logic and functionality of the chip using hardware description languages (HDLs) such as Verilog or VHDL. A design engineer also performs synthesis, simulation, and verification of the design to ensure its correctness and quality.

Design Verification Engineer
A verification engineer is responsible for checking the functionality and performance of the chip using various verification techniques and tools, such as System Verilog, UVM, formal methods, etc. A verification engineer also analyzes the test coverage and debugs the design errors.

Physical Design Engineer
A physical design engineer is responsible for converting the logical design into a physical layout that can be fabricated on a silicon wafer. A physical design engineer also performs tasks such as floorplanning, placement, routing, timing analysis, power analysis, etc., using various physical design tools.

DFT (Design For Test) Engineer
A DFT engineer is responsible for testing the functionality and quality of the chip after fabrication using various test techniques and tools, such as scan, ATPG, test compressors, boundary scan, etc. A DFT engineer also performs fault simulation, diagnosis, and repair of the chip.

Application Engineer
An application engineer is responsible for assisting the customers in using the chip or system for their specific applications. An application engineer also provides technical support, training, documentation, etc., to the customers.

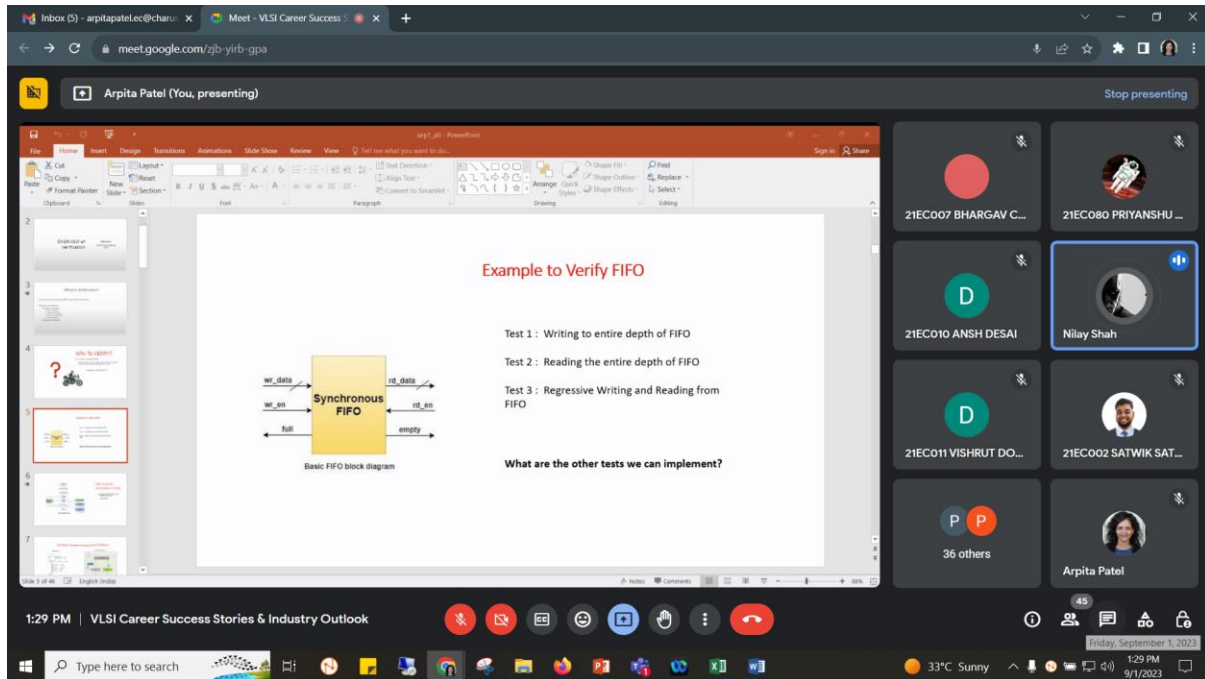
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Journey of a chip



Total Number of students: 45

Amount sanctioned by CSPIT/CHARUSAT:

Accounts details:

Sr. No.	Details	Rupees
Income		
1.		NIL
Expenses		
1.		NIL
Total		

Overall impact of workshop: Very Good

Coordinator Sign:

Head of Department Sign:

Attendance:

SrNo	Participants Type	StudentID
1	CHARUSAT STUDENT	21ec004
2	CHARUSAT STUDENT	21ec005
3	CHARUSAT STUDENT	21ec006
4	CHARUSAT STUDENT	21ec007
5	CHARUSAT STUDENT	21ec008
6	CHARUSAT STUDENT	21ec009
7	CHARUSAT STUDENT	21ec017
8	CHARUSAT STUDENT	21ec018
9	CHARUSAT STUDENT	21ec019
10	CHARUSAT STUDENT	21ec020
11	CHARUSAT STUDENT	21ec021
12	CHARUSAT STUDENT	21ec022
13	CHARUSAT STUDENT	21ec023
14	CHARUSAT STUDENT	21ec024
15	CHARUSAT STUDENT	21ec025
16	CHARUSAT STUDENT	21ec026
17	CHARUSAT STUDENT	21ec027
18	CHARUSAT STUDENT	21ec028
19	CHARUSAT STUDENT	21ec050
20	CHARUSAT STUDENT	21ec051
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29	CHARUSAT STUDENT	21ec060
30	CHARUSAT STUDENT	21ec061
31	CHARUSAT STUDENT	21ec062
32	CHARUSAT STUDENT	21ec063
33	CHARUSAT STUDENT	21ec064
34	CHARUSAT STUDENT	21ec065
35	CHARUSAT STUDENT	21ec066
36	CHARUSAT STUDENT	21ec067
37	CHARUSAT STUDENT	21ec068
38	CHARUSAT STUDENT	21ec069
39	CHARUSAT STUDENT	21ec070
40	CHARUSAT STUDENT	21ec071

VLSI CLUB-ChipXplorers

V T Patel Department of Electronics & Communication Engineering
www.reallygreatsite.com

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VLSI Career Success Stories & Industry Outlook



Nilay Shah
SoC Verification Engineer
Intel



Parth Ardesana
ASIC Physical Design Engineer
Samsung



Jaydeep H. Padariya
Sr. Staff DFT Engineer
SiMa.ai



Prerak Dalia
Senior Physical Design Engineer
eInfochips

Scan here for registration



Coordinator:
Dr.Arпита Patel

Date: September 1,2023
Time: 1:00 p.m onwards
Mode:Online via Google meet