

1. Description

1.1. Project

Project Name	snake_nokia5510
Board Name	NUCLEO-G071RB
Generated with:	STM32CubeMX 6.2.0
Date	10/14/2023

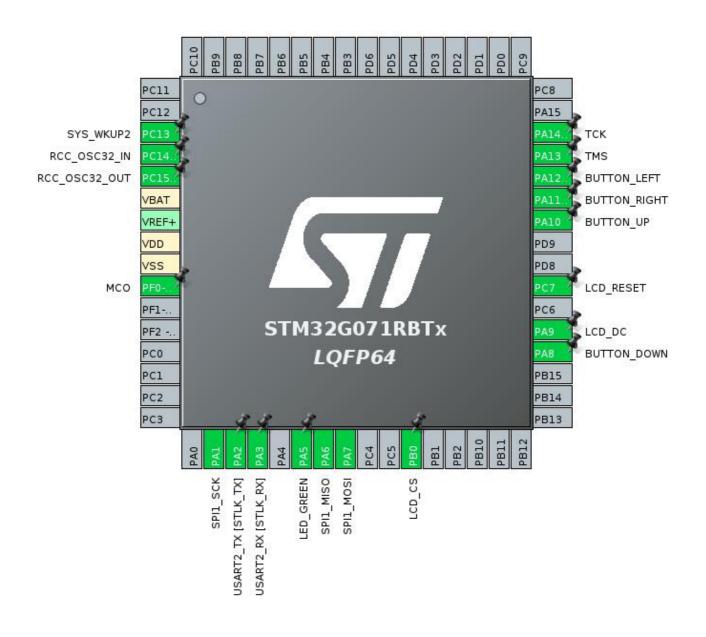
1.2. MCU

MCU Series	STM32G0
MCU Line	STM32G0x1
MCU name	STM32G071RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M0+

2. Pinout Configuration

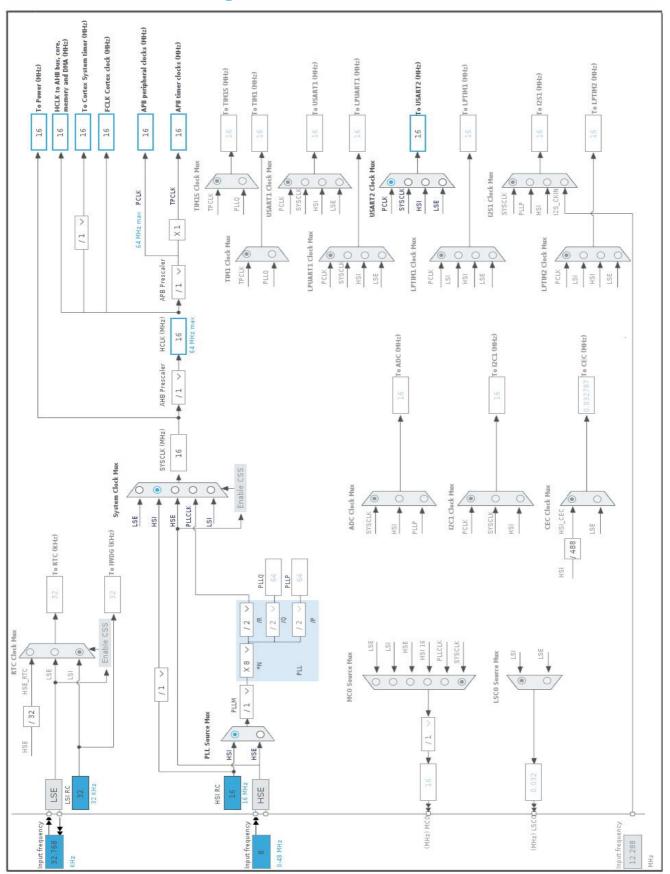


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PC13	I/O	SYS_WKUP2	
4	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
5	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
6	VBAT	Power		
8	VDD	Power		
9	VSS	Power		
10	PF0-OSC_IN (PF0)	I/O	RCC_OSC_IN	MCO
18	PA1	I/O	SPI1_SCK	
19	PA2	I/O	USART2_TX	USART2_TX [STLK_TX]
20	PA3	I/O	USART2_RX	USART2_RX [STLK_RX]
22	PA5 *	I/O	GPIO_Output	LED_GREEN
23	PA6	I/O	SPI1_MISO	
24	PA7	I/O	SPI1_MOSI	
27	PB0 *	I/O	GPIO_Output	LCD_CS
36	PA8	I/O	GPIO_EXTI8	BUTTON_DOWN
37	PA9 *	I/O	GPIO_Output	LCD_DC
39	PC7 *	I/O	GPIO_Output	LCD_RESET
42	PA10	I/O	GPIO_EXTI10	BUTTON_UP
43	PA11 [PA9]	I/O	GPIO_EXTI11	BUTTON_RIGHT
44	PA12 [PA10]	I/O	GPIO_EXTI12	BUTTON_LEFT
45	PA13	I/O	SYS_SWDIO	TMS
46	PA14-BOOT0	I/O	SYS_SWCLK	TCK

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	snake_nokia5510	
Project Folder	/home/kacper/projects/snake_nokia5510	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_G0 V1.4.1	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART2_UART_Init	USART2
4	MX_SPI1_Init	SPI1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G0
Line	STM32G0x1
MCU	STM32G071RBTx
Datasheet	DS12232_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

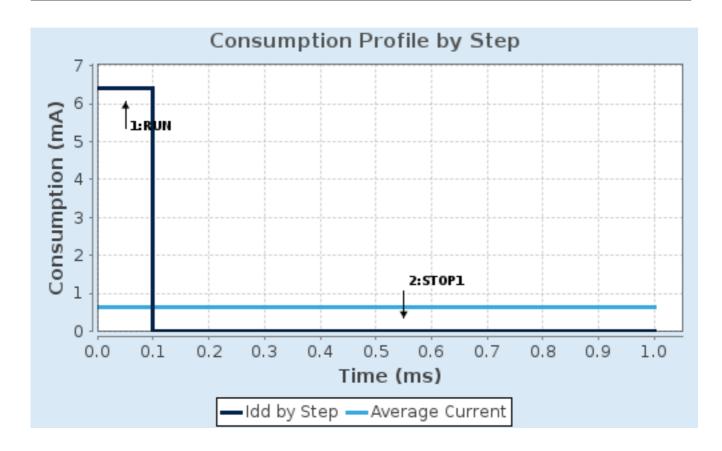
6.4. Sequence

	T	
Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	Flash-PowerDown
CPU Frequency	64 MHz	16 MHz
Clock Configuration	HSI PLL	HSI
Clock Source Frequency	16 MHz	16 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	6.4 mA	3.4 µA
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	128.75	130
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	643.06 µA
Battery Life	1 month, 14 days,	Average DMIPS	80.0 DMIPS
	21 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value (64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration TRUE

7.2. SPI1

Mode: Full-Duplex Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 4 *

Baud Rate 4.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSSP Mode Enabled

NSS Signal Type Software

7.3. SYS

mode: Debug

mode: System Wake-Up 2 Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.4. USART2

Mode: Asynchronous 7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 9600 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode GPIO pull/up pull Max down Speed		User Label	
RCC	RCC PC14- RCC_OSC32_IN OSC32_IN (PC14)		n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
	PF0-OSC_IN (PF0)	RCC_OSC_IN	n/a	n/a	n/a	МСО
SPI1	PA1	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PC13	SYS_WKUP2	n/a	n/a	n/a	
	PA13	SYS_SWDIO	n/a	n/a	n/a	TMS
	PA14- SYS_SWCLK BOOT0		n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up *	Low	USART2_TX [STLK_TX]
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up *	Low	USART2_RX [STLK_RX]
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LED_GREEN
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_CS
					1	
	PA8	GPIO_EXTI8	External Interrupt	Pull-up *	n/a	BUTTON_DOWN
	PA8	•	External Interrupt Mode with Falling	Pull-up *	n/a	BUTTON_DOWN
	PA8	•	•	Pull-up *	n/a	BUTTON_DOWN
	PA8	•	Mode with Falling	Pull-up * No pull-up and no pull-down	n/a Low	BUTTON_DOWN LCD_DC
		GPIO_EXTI8	Mode with Falling edge trigger detection	·		
	PA9	GPIO_EXTI8 GPIO_Output	Mode with Falling edge trigger detection Output Push Pull	No pull-up and no pull-down	Low	LCD_DC
	PA9 PC7	GPIO_EXTI8 GPIO_Output GPIO_Output	Mode with Falling edge trigger detection Output Push Pull Output Push Pull	No pull-up and no pull-down No pull-up and no pull-down	Low Low	LCD_DC LCD_RESET
	PA9 PC7	GPIO_EXTI8 GPIO_Output GPIO_Output	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt	No pull-up and no pull-down No pull-up and no pull-down	Low Low	LCD_DC LCD_RESET
	PA9 PC7	GPIO_EXTI8 GPIO_Output GPIO_Output	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt Mode with Falling	No pull-up and no pull-down No pull-up and no pull-down	Low Low	LCD_DC LCD_RESET
	PA9 PC7 PA10	GPIO_EXTI8 GPIO_Output GPIO_Output GPIO_EXTI10	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down No pull-up and no pull-down Pull-up *	Low Low n/a	LCD_DC LCD_RESET BUTTON_UP
	PA9 PC7 PA10	GPIO_EXTI8 GPIO_Output GPIO_Output GPIO_EXTI10	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt Mode with Falling edge trigger detection External Interrupt	No pull-up and no pull-down No pull-up and no pull-down Pull-up *	Low Low n/a	LCD_DC LCD_RESET BUTTON_UP
	PA9 PC7 PA10	GPIO_EXTI8 GPIO_Output GPIO_Output GPIO_EXTI10	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt Mode with Falling edge trigger detection External Interrupt Mode with Falling	No pull-up and no pull-down No pull-up and no pull-down Pull-up *	Low Low n/a	LCD_DC LCD_RESET BUTTON_UP
	PA9 PC7 PA10 PA11 [PA9]	GPIO_EXTI8 GPIO_Output GPIO_EXTI10 GPIO_EXTI11	Mode with Falling edge trigger detection Output Push Pull Output Push Pull External Interrupt Mode with Falling edge trigger detection External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down No pull-up and no pull-down Pull-up * Pull-up *	Low Low n/a	LCD_DC LCD_RESET BUTTON_UP BUTTON_RIGHT

8.	2.	DMA	config	uration
•			909	a. a. o.

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
System service call via SWI instruction	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
EXTI line 4 to 15 interrupts	true	0	0	
PVD interrupt through EXTI line 16		unused		
Flash global interrupt	unused			
RCC global interrupt	unused			
SPI1 global interrupt	unused			
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26		unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line 4 to 15 interrupts	true	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Computing	Utilities
DMA			SPI1 ⊘			
GPIO ⊘			USART2 ♥			
NVIC 🕏						
RCC ⊘						
sys 🔮						

10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00412180.pdf

Reference http://www.st.com/resource/en/reference_manual/DM00371828.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00104451.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/DM00463881.pdf

Application note http://www.st.com/resource/en/application_note/CD00160362.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application_note/DM00081379.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00151811.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00355687.pdf

Application note http://www.st.com/resource/en/application_note/DM00311483.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00535045.pdf

Application note http://www.st.com/resource/en/application_note/DM00443870.pdf

Application note http://www.st.com/resource/en/application_note/DM00449912.pdf

Application note	http://www.st.com/resource/en/application_note/DM00483659.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf