UNIVERSITY of WASHINGTON | TACOMA

Digital Integrated Circuit Design (TCES 421)

Name _____

Homework 3 (Q1, 2, 3: 20pts each, Q4: 40pts Total: 3X20pts+40pts=100pts): ***Based on "Combinational Logic Gates Design in CMOS" (Chap 6); Submit report containing circuit schematics, plots and all descriptions; (grading emphasis will be given for showing all the steps clearly); Due on 7/18/2023***

Please Note: IBM 0.18um CMOS 7RF (cmrf7sf) device normal supply voltage Vdd=1.8V

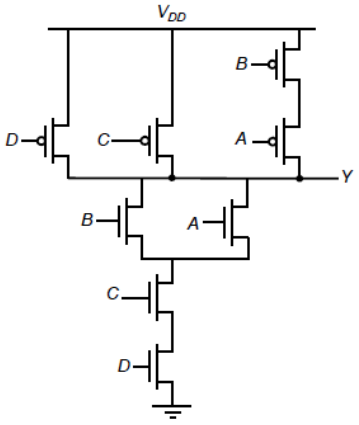
Q1: Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

$$\bar{Y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

Q2: Implement the following logic function using complementary CMOS.

a) $Y = \left((\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D} + \bar{E}) + \bar{F}\right) \cdot \bar{G}$
b) Size the devices such that the output resistance is the same as that of an inverter with NMOS $W_n/L=2$ and PMOS $W_p/L=6$
c) Which input patterns would give the "worst" and the "best" equivalent pull-up or pull-down resistance?

Q3: What is the logic function implemented by the CMOS transistor network shown below?



Q4: (Cadence)

a) For a CMOS inverter determine propagation delays: t_{pHL}, t_{pLH}, and t_p. Use W_n=2um W_p=6um and a pulsed voltage input with 4GHz frequency.

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b) Implement 2-input NAND function using CMOS transistors of IBM 0.18um CMOS 7RF (cmrf7sf) technology in cadence. Create a NAND symbol. Run simulation in cadence to verify VTC of the NAND gate using different input combinations as shown in Fig. 1.
c) Run transient simulation in cadence to verify the delay dependency on the input patterns as shown in Fig. 2.
d) Verify the NAND logic functionality by connecting the 2-inputs to "pulsed voltage sources" with different frequency such as 300MHz and 500MHz and verify the output voltage for different logic state such as 00, 01, 10, 11 etc. as in the truth-table shown below.
e) Build an AND function by combining NAND+INV. Create AND symbol containing NAND+INV and simulate as in (d) above.

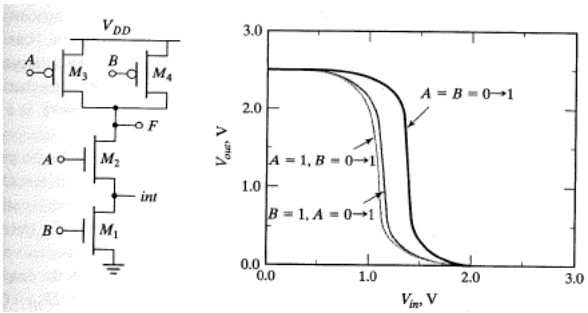
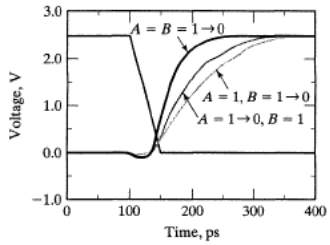


Fig.1



Input Data Pattern	Delay (ps)
$A = B = 0 \rightarrow 1$	69
$A = 1, B = 0 \rightarrow 1$	62
$A = 0 \rightarrow 1, B = 1$	50
$A = B = 1 \rightarrow 0$	35
$A = 1, B = 1 \rightarrow 0$	76
$A = 1 \rightarrow 0, B = 1$	57

Fig.2

Truth Table for two-input NAND

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0