# TCES 330 Digital Systems Design

# Spring 2022

Note: this homework doesn't require to build Quartus Prime project, unless you want to check your design using Quartus tools, e.g., Netlist Viewers. ModelSim would be functional enough for code developing, debugging, and testing of your design, as we discussed during class time.

Please follow the instructions given below in terms of creating folders, adding files and Canvas submission.

1: On your personal drive, create a folder named HW1, and two subfolders named Q1 and Q2, as shown in Figure 1:
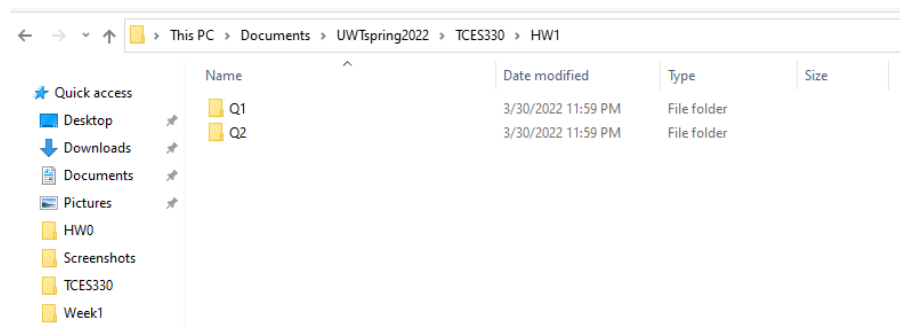


Figure 1

2: Inside your Q1 folder,

a.  Using Quartus (or ModeSim directly) to develop a SystemVerilog module **Q1.sv** to describe the circuit in Figure 2, in its structural representation, i.e., gate instantiations. Notice that the numbers (#4, #5, #6) don't mean anything here.
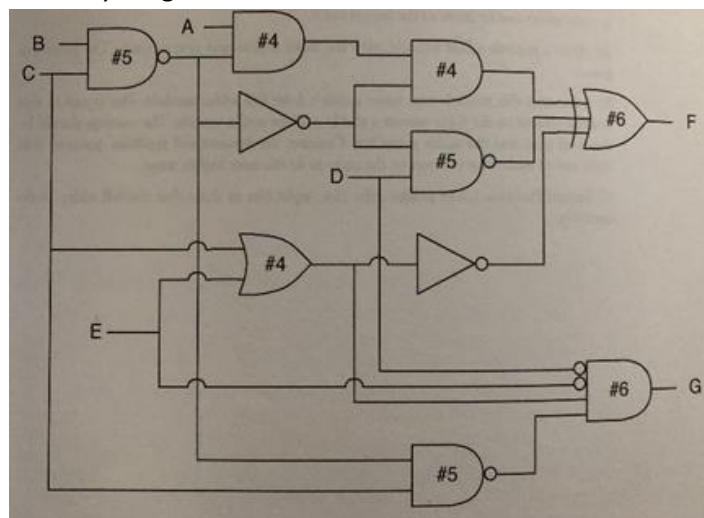


Figure 2

b. In your **Q1.sv** file, add a test bench **Q1_testbench** for testing purpose. Note that in this first assignment, the testbench should consider all the possible cases when the 5 inputs go through 32 ($2^5$) input combinations. Instead of 32 lines of assigning input values, use **for** loop to improve the readability.

c. Copy the runlab.do, light_wave.do files into your Q1 folder. Modify them as we discussed in class.

d. Run the simulation for your circuit. Correct any errors you may find. Repeat until you get a successful simulation run.

3: Inside your Q2 folder,

a. Using Quartus (or ModeSim directly) to develop a SystemVerilog module **Q2.sv** which describes the circuit in Figure 3a by continuous assignment. Notice that the numbers (#1, #3, #4, #5) don't mean anything here.

b. In your **Q2.sv** file, add a test bench **Q2_testbench** for testing purpose. Note that the inputs **A/a** and **B/b** should change as described in Figure 3b.

c. Copy the runlab.do, light_wave.do files into your Q2 folder. Modify them as we discussed in class.

d. Run the simulation for your circuit. Correct any errors you may find. Repeat until you get a successful simulation run.



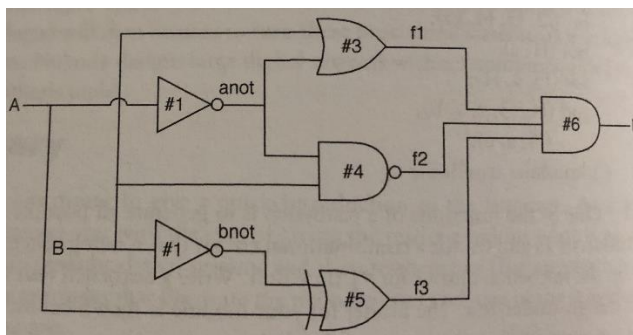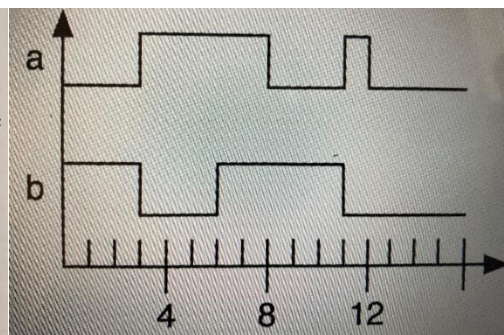Figure 3a                                        Figure 3b

4: Check and zip both Q1 and Q2 folders, you will get a zip file named HW1.zip, as shown below. Submit HW1.zip to Canvas by 11:59pm, Saturday 04/09.