Kadir Emre Oto
150140032

BLG 322E - Computer Architecture
Assignment 4

Due Date: 25.04.2018, Wednesday, 22:00

a) Construct the truth table for the bus arbiter. BR_i represents the BR output of the $DMAC_i$, and BG_i represents the BG input of the $DMAC_i$.

$\overline{BR_1}$	$\overline{BR_2}$	$\overline{BR_3}$	$\overline{BR}$	$\overline{BG}$	$\overline{BG_1}$	$\overline{BG_2}$	$\overline{BG_3}$
0	X	X	0	0	0	1	1
0	X	X	0	1	1	1	1
1	0	X	0	0	1	0	1
1	0	X	0	1	1	1	1
1	1	0	0	0	1	1	0
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

b) Write the minimized logic expressions for the outputs of the bus arbiter.

$$BR = BR_1 + BR_2 + BR_3$$

$$BG_1 = BR_1 \cdot BG$$

$$BG_2 = \overline{BR_1} \cdot BR_2 \cdot BG$$

$$BG_3 = \overline{BR_1} \cdot \overline{BR_2} \cdot BR_3 \cdot BG$$

c) $DMAC_1$ and $DMAC_3$ are in the cycle-stealing mode, and $DMAC_2$ is in the burst mode. All $DMACs$ are programmed to transfer 10 words. Assume that $DMAC_1$, $DMAC_2$ and $DMAC_3$ issue bus requests at the same time as the processor is in the instruction fetch cycle. Write step by step operations performed by the $DMACs$ and the CPU from the beginning of the instruction fetch until the end of the completion of the first instruction.

Firstly, all bus request input signals (BR_1, BR_2, BR_3) are active (zero), and BR signal turns active. Then CPU activates the signal BG. Bus arbiter activates BG_1 and $DMAC_1$ observes AS and BGACK signals and waits until the previous bus cycle is complete and the previous bus master releases the bus. After that, $DMAC_1$ takes control of the bus, inactivates the BR_1 output to allow other DMACs sending their requests, and puts a word to bus. Because BR_1 is not active now, BG_2 will be active, and $DMAC_2$ starts observing the bus flags.

After $DMAC_1$ put a word, it changes the bus signals (AS and BGACK), and $DMAC_2$ takes the bus control immediately (in different designs, cpu may take the control of bus first). $DMAC_2$ puts all 10 words.

Then, these steps repeat and $DMAC_1$ takes control of the bus, and one more word will be put into the bus. $DMAC_1$ and $DMAC_3$ transfers their data consecutively.