Istanbul Technical University
Department of Computer Engineering

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BLG 322E – Computer Architecture
Assignment 2 - Solution

a) [50 points]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
LD 0(R5), R1	FR	EX	MW													
LD 0(R6), R2		FR	EX	MW												
LD 0(R7), R3			FR	EX	MW											
NOOP				FR	EX	MW										
ADD R3, R2, R3					FR	EX	MW									
NOOP						FR	EX	MW								
SUB R3, R1, R3							FR	EX	MW							
BNZ EX								FR	EX	MW						
NOOP									FR	EX	MW					
ADD R0, 0, R3										FR	EX	MW				
:::::: (a piece of code)																
EX: NEG R3											FR	EX	MW			
NOOP												FR	EX	MW		
ADD R3, R2, R2													FR	EX	MW	

Total amount of penalty is 4 clock cycles.

b) [50 points]

	1	2	3	4	5	6	7	8	9	10	11	12	13	
LD 0(R6), R2	FR	EX	MW											
LD 0(R7), R3		FR	EX	MW										
LD 0(R5), R1			FR	EX	MW									
ADD R3, R2, R3				FR	EX	MW								
NOOP					FR	EX	MW							
SUB R3, R1, R3						FR	EX	MW						
BNZ EX							FR	EX	MW					
NOOP								FR	EX	MW				
ADD R0, 0, R3									FR	EX	MW			
:::::: (a piece of code)														
EX: NEG										FR	EX	MW		
NOOP											FR	EX	MW	
ADD R3, R2, R2												FR	EX	MW

Total amount of penalty is 3 clock cycles.

Bir diğer çözüm: NEG R3 'ten sonra R3 sıfırlandığından devamındaki kod NEG R3'ten etkilenmez. Ancak bu kadar detayı belirleyebilecek bir compiler tasarlamak zordur.

	1	2	3	4	5	6	7	8	9	10	11	12	13
LD 0(R6), R2	FR	EX	MW										
LD 0(R7), R3		FR	EX	MW									
LD 0(R5), R1			FR	EX	MW								
ADD R3, R2, R3				FR	EX	MW							
NOOP					FR	EX	MW						
SUB R3, R1, R3						FR	EX	MW					
BNZ EX							FR	EX	MW				
NEG R3								FR	EX	MW			
ADD R0, 0, R3									FR	EX	MW		
:::::: (a piece of code)													
EX: NOOP										FR	EX	MW	
ADD R3, R2, R2											FR	EX	MW

Total amount of penalty is 2 clock cycles.