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DIGITAL CIRCUITS FINAL EXAM (Question 1)

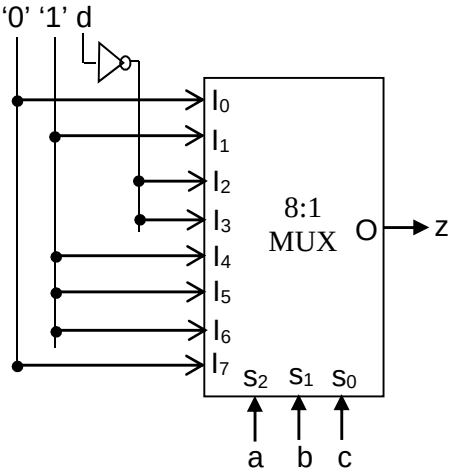
Regulations:

1. Duration is 110 minutes.
2. Asking questions to proctors is not allowed.
3. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
4. Cell phones are prohibited on the desk, they must be switched off.

QUESTION 1 (30 Points):

The given combinational circuit has four inputs (a,b,c,d) and one output (z).

a. Construct the truth table of this circuit and write the expression of the logical function z=f(a,b,c,d) in 1st canonical form.
b. Minimize the expression using axioms and theorems of the Boolean algebra.
c. Design and draw the same circuit using a 4:16 decoder and other necessary logic gates.



Solution:

a.

Truth table:

a b c d	z
0 0 0 0	0
0 0 0 1	0
0 0 1 0	1
0 0 1 1	1
0 1 0 0	1
0 1 0 1	0
0 1 1 0	1
0 1 1 1	0
1 0 0 0	1
1 0 0 1	1
1 0 1 0	1
1 0 1 1	1
1 1 0 0	1
1 1 0 1	1
1 1 1 0	0
1 1 1 1	0

From the truth table we can obtain minterms and write the expression of the function in the 1st canonical form.
Remember, in minterms all variables (literals) appear once.
1st canonical form:

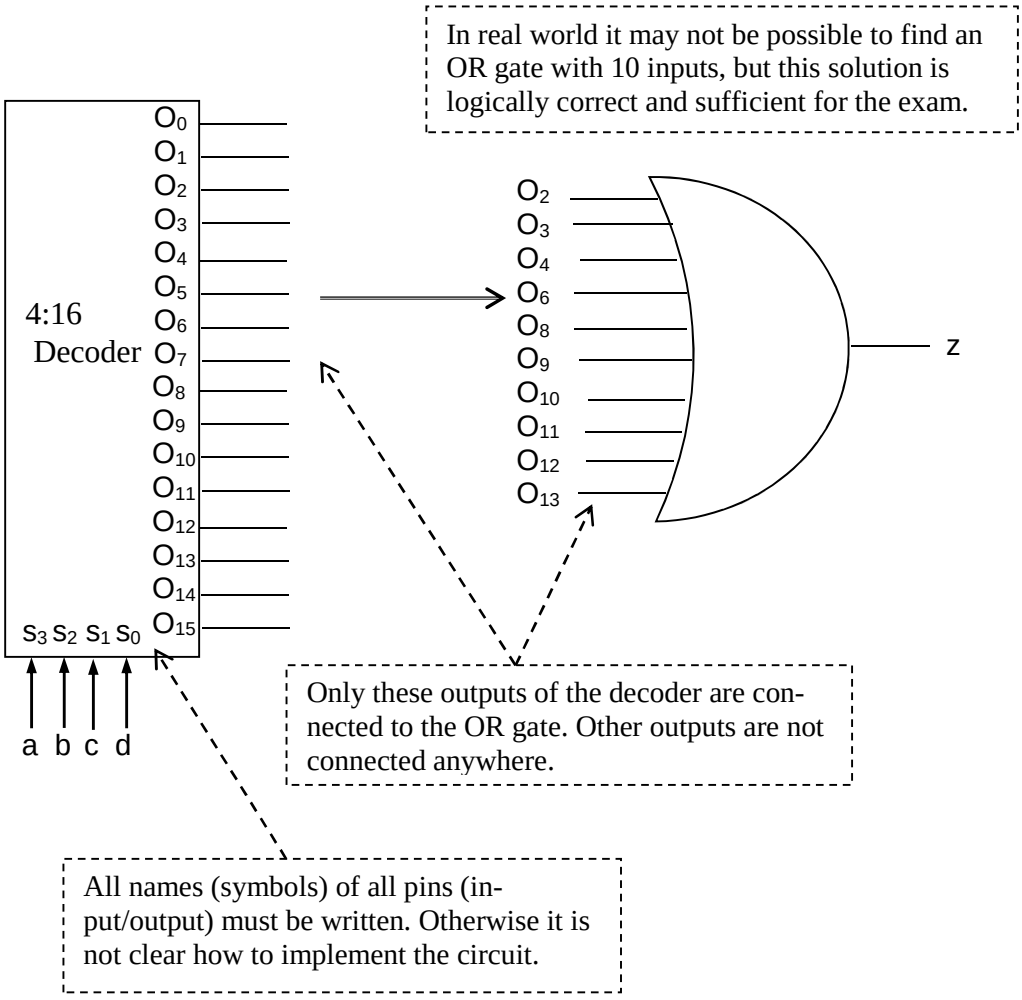
z= a'b'cd'+ a'b'cd + a'bc'd'+ a'bcd'+ ab'c'd'+ ab'c'd + ab'cd' + ab'cd
+ abc'd'+ abc'd

b.

There are different ways to minimize the expression in the 1st canonical form.
Minimized expression:

z= a'bd' + ac' + b'c

c.

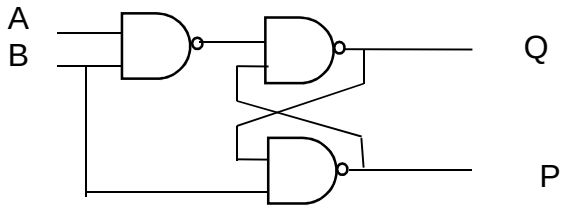

In real world it may not be possible to find an OR gate with 10 inputs, but this solution is logically correct and sufficient for the exam.
4:16
Decoder
O0
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
O11
O12
O13
O14
O15
S3 S2 S1 S0
a b c d
O2
O3
O4
O6
O8
O9
O10
O11
O12
O13
z
Only these outputs of the decoder are connected to the OR gate. Other outputs are not connected anywhere.
All names (symbols) of all pins (input/output) must be written. Otherwise it is not clear how to implement the circuit.

DIGITAL CIRCUITS FINAL EXAM (Question 2)

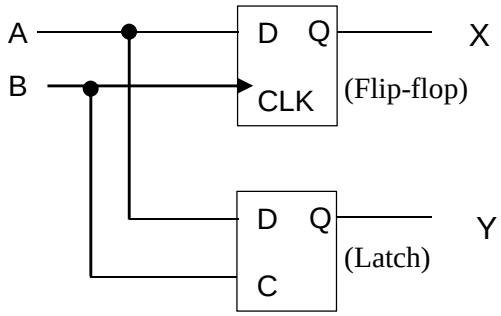
QUESTION 2 (30 Points):

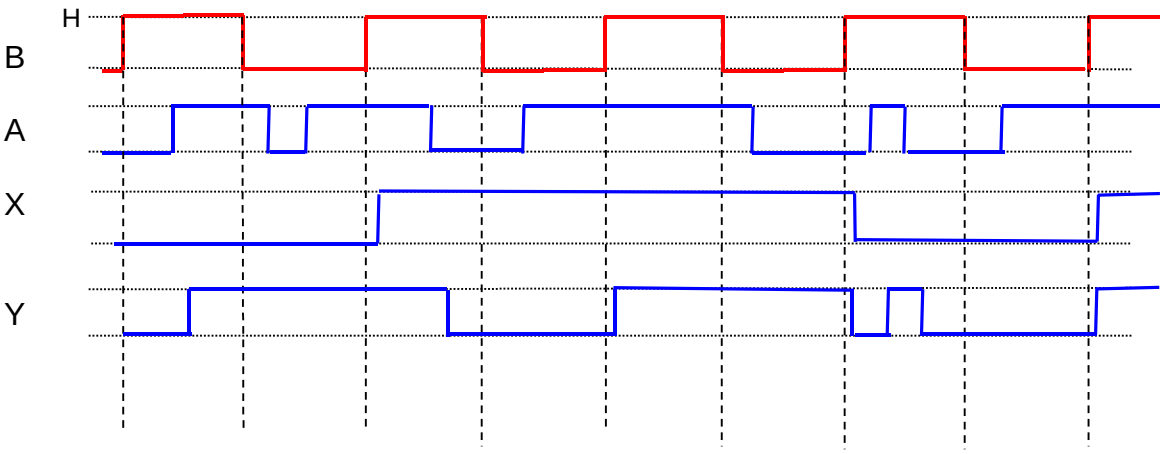
a. Analyze the given circuit by applying different input values and show that this circuit can be used as a memory unit.

Derive the next state equation for Q as Q(t+1)=f(A,B,Q(t)).

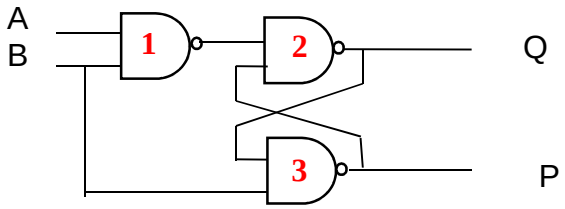


b. In the circuit given below, there is one **flip flop** (positive edge-triggered) and one **latch** with an enable (C) input. Complete the timing diagram and show how outputs X and Y respond according to the input changes.





a.



A	B	Q	P	
0	0	0	1	If B=0 then P = 1. The output of NAND1 is 1 and Q is 0 (stable)
0	1	0	1	After (A=0, B=0), Q=0 from previous state and P = 1. The output of NAND1 is 1and Q = 0 (stable)
1	0	0	1	If B=0 then P = 1. The output of NAND1 is 1 and Q is 0 (stable)
1	1	1	0	The output of NAND1 is 0. Therefore the output of NAND2, Q= 1 and P=0 (stable)
0	1	1	0	After (A=1, B=1), The output of NAND1 is 1. P = 0 from previous state and Q = 1, P=0 (stable)

A	B	
0	0	Reset
1	0	
0	1	Don’t change
1	1	Set

The circuit is stable and can be switched to another state and has set, reset and don’t change conditions. Therefore it can be used as a memory unit.

A	**B**	**Q(t)**	**Q(t+1)**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

AB\Q(t)	**0**	**1**
00	0	0
01	0	1
11	1	1
10	0	0

Q(t+1) = BQ(t) + AB

DIGITAL CIRCUITS FINAL EXAM (Question 3)

QUESTION 3 (40 Points):

A clocked synchronous circuit with one input (X) and one output (Z) will be designed using the **Moore model**. Whenever the total number of "1"s received at input X during the positive edges of the clock signal is odd and greater than 2 (3, 5, 7, …) the output Z will be "1", otherwise "0". The "1"s at the input X don't need to be successive.

Example for input and output sequences:

X = 1 1 1 0 0 1 0 1 0 1 0

Z = 0 0 1 1 1 0 0 1 1 0 0

a. Draw the state diagram and construct the State/Output table of the circuit.

b. Implement and draw the circuit using positive edge triggered **JK** flip-flops and other necessary logic gates.

a)

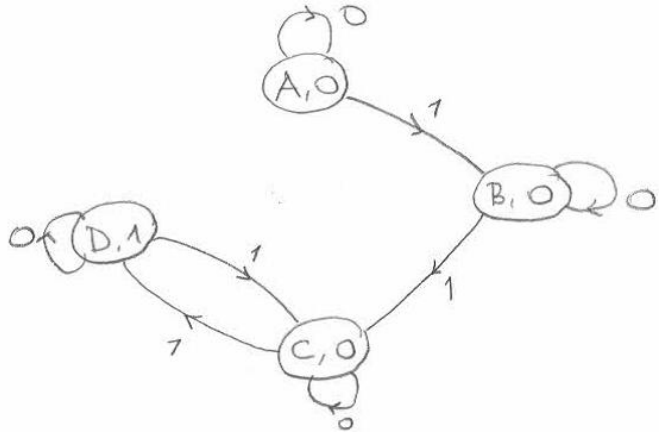
States

A: zero ones

B: one one

C: two or even ones

D: (three or more) and odd ones



State/output table

$Q_1^+Q_0^+, Z$

Q_1Q_0	X = 0	X = 1	Z
A	A	B	0
B	B	C	0
C	C	D	0
D	D	C	1

Codes

A: 00

B: 01

C: 10

D: 11

$Q_1^+Q_0^+$

Q_1Q_0 \ X	0	1
00	00	01
01	01	10
10	10	11
11	11	10

b)

Symbol	Transition	J	K
0	0→0	0	ϕ
α	0→1	1	ϕ
β	1→0	ϕ	1
1	1→1	ϕ	0

Q_1^+

Q_1Q_0 \ X	0	1
00	0	0
01	0	α
10	1	1
11	1	1

Q_0^+

Q_1Q_0 \ X	0	1
00	0	α
01	1	β
10	0	α
11	1	β

J_1

Q_1Q_0 \ X	0	1
00	0	0
01	0	1
11	ϕ	ϕ
10	ϕ	ϕ

K_1

Q_1Q_0 \ X	0	1
00	ϕ	ϕ
01	ϕ	ϕ
11	0	0
10	0	0

J_0

Q_1Q_0 \ X	0	1
00	0	1
01	ϕ	ϕ
11	0	1
10	ϕ	ϕ

K_0

Q_1Q_0 \ X	0	1
00	ϕ	ϕ
01	0	1
11	ϕ	ϕ
10	0	1

$J_1 = Q_0X$ $\quad$ $J_0 = X$

$K_1 = 0$ $\quad$ $K_0 = X$

$Z = Q_1Q_0$