Clocked Synchronous Sequential Circuits

In sequential circuits output values depend both on input values and on the state of the circuit.

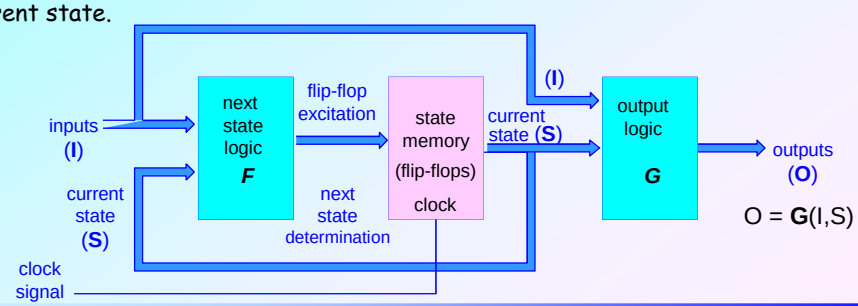
The clocked synchronous sequential circuits are designed based on *finite state machine* model where the current state is stored in memory elements (flip-flops).

All flip-flops are triggered with the same **clock signal** (synchronized). Therefore the machine can change its state only during the active transition of the clock signal.

Sequential circuits can be designed according to following two models.

a) Mealy Model (*George H. Mealy, computer scientist, USA*)

In this model, outputs are determined by a function of current input values and current state.



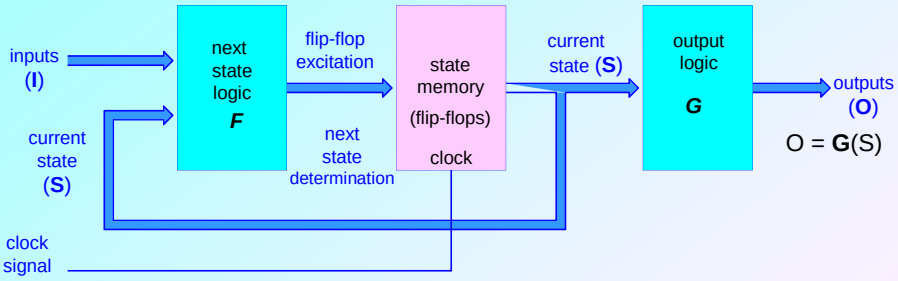
b) Moore Model

Edward Forrest Moore (1925-2003) Mathematician, computer scientist, USA

In this model, the output depends only on current state.

Input values determine only the next state.

And the state determines the output.



Most of sequential circuits can be designed in both Mealy and Moore models.

Analysis of clocked synchronous sequential circuits

Before we start to design sequential circuits we will see how to analyze a given sequential circuit.

Reminder: Implementation of a sequential circuit means implementation of the functions F (next state) and G (output). (See 7.1 and 7.2)

I: Input, S: Current *State*, S^+: Next state, O : Output

$S^+ = \mathbf{F}(I,S)$, Mealy: $O = \mathbf{G}(I,S)$ Moore: $O = \mathbf{G}(S)$

Analysis of a synchronous circuits means, to find out the behavior of a circuit, which is given by the functions F and G. (What does the circuit do?)

Analysis of a synchronous circuits has 3 steps:

1. Determine the expressions of the functions F (next state) and G (output).
2. Use F and G functions to construct the state/output table that specifies the next state and output of the circuit for every possible combination of input and current state.
3. To see the behavior of the circuit better the state diagram can be optionally drawn, which shows all state transitions and outputs of the machine graphically.

Determination of next states:
Characteristic Equations of flip-flops

F function of a clocked sequential circuit determines input values of flip-flops (flip-flop excitation).

These input values with the current state of the flip-flop determine its next state (output of the flip-flop after the transition of the clock signal).

The functional behavior of a latch or flip-flop can be described by a **characteristic equation** that specifies the flip-flop's next state as a function of its inputs and current.

Characteristic equations of flip-flops:

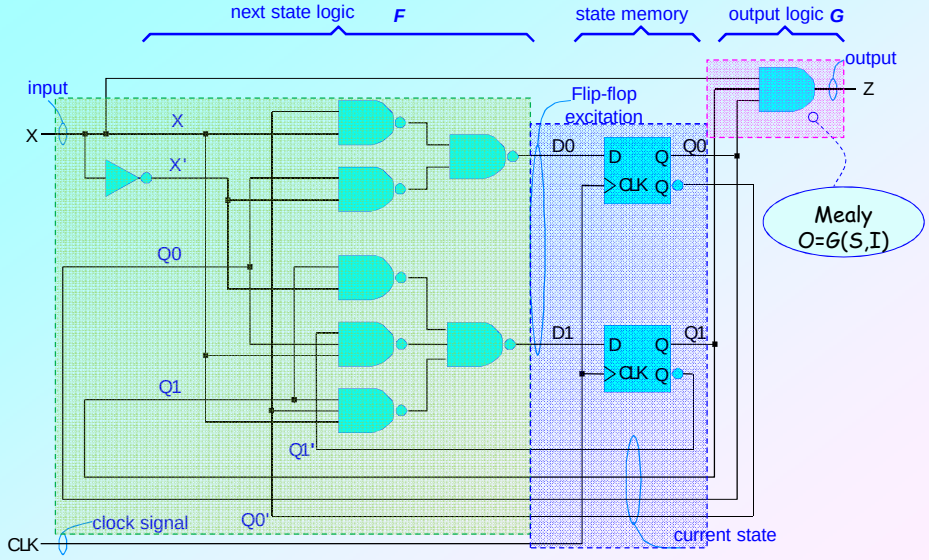
SR FF: $Q(t+1) = S + R' \bullet Q(t), \quad SR=0$

JK FF: $Q(t+1) = J \bullet Q(t)' + K' \bullet Q(t)$

D FF : $Q(t+1) = D$

T FF : $Q(t+1) = T \oplus Q(t)$

Example: Analyze the given clocked synchronous circuit.



S={Q0(t),Q1(t)} S^+={Q0(t^+), Q1(t^+)} = ff(D0,D1) I={X} O={Z}

1. Determining the expression of F function that drives the flip-flops:

$D_0 = Q_0 \bullet X' + Q_0' \bullet X$

$D_1 = Q_1 \bullet X' + Q_1' \bullet Q_0 \bullet X + Q_1 \bullet Q_0' \bullet X$

2. Determining expressions of next states S^+={Q0(t^+), Q1(t^+)}

$Q0^+ = D0$ (D type FF characteristic function)

$Q1^+ = D1$ (D tipi FF characteristic function)

$Q0^+ = Q0 \bullet X' + Q0' \bullet X$

$Q1^+ = Q1 \bullet X' + Q1' \bullet Q0 \bullet X + Q1 \bullet Q0' \bullet X$

3. Constructing the state transition table

$Q1^+ Q0^+$ \ X	0	1
Q1Q0		
00	00	01
01	01	10
10	10	11
11	11	00

Inputs

Current States

Next States

To make the table more understandable we assign state names to state codes.

00: A
01: B
10: C
11: D

State Table

S^+ \ X	0	1
S		
A	A	B
B	B	C
C	C	D
D	D	A

S: Current state S^+: Next state Q1 and Q0: State variables

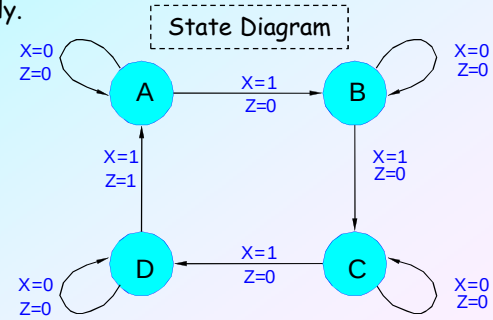
4. Determining the expression of the output function G.

Z = Q1•Q0•X (Mealy model, because output depends both on input and state)

5. Constructing the State/Output table

S^+,Z \ X / S	0	1
A	A,0	B,0
B	B,0	C,0
C	C,0	D,0
D	D,0	A,1

This table presents the behavior of the finite state machine.
This behavior can be also presented by a state diagram graphically.



Reading the table:
When the machine is in state A, if it gets 1 from the input, the output becomes 0; after the transition of the clock signal machine goes to state B.

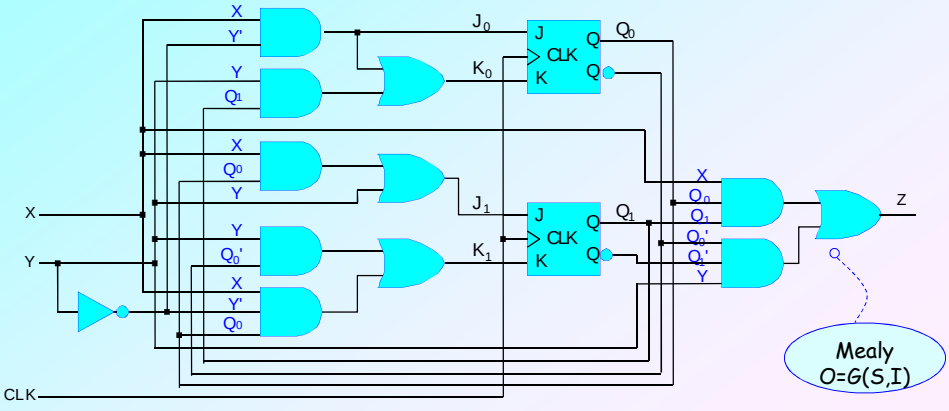
Verbal expression of the behavior of the circuit: We assume that A is the initial state. Only if the number of 1s received from the input is a multiple of 4 then the output is 1. Otherwise the output is 0.

Example: Analysis of a clocked synchronous circuit with JK Flip-flops

Differently from the previous example, during determining the expressions of next states (Q_i^+), here we will use the characteristic function of the JK flip-flop.

Reminder: $Q^+ = J•Q' + K'•Q$ (characteristic function of the JK flip-flop)

Circuit:



1. Determining the F function that drives the inputs of the flip-flops:

J0 = X•Y'
K0 = X•Y' + Y•Q1

J1 = X•Q0 + Y
K1 = Y•Q0' + X•Y'•Q0

2. Next state $S^+=\{Q0(t^+), Q1(t^+)\}$ expressions.

$Q0^+$ = J0•Q0' + K0'•Q0 (JK FF characteristic function)
$Q0^+$ = X•Y'•Q0' + (X•Y' + Y•Q1)'•Q0
$Q0^+$ = X•Y'•Q0' + X'•Y'•Q0 + X'•Q1'•Q0 + Y•Q1'•Q0
$Q0^+$ = X•Y'•Q0' + X'•Y'•Q0 + Y•Q1'•Q0 (minimization)

$Q1^+$ = J1•Q1' + K1'•Q1 (JK FF characteristic function)
$Q1^+$ = (X•Q0 + Y)•Q1' + (Y•Q0' + X•Y'•Q0)'•Q1
$Q1^+$ = X•Q1'•Q0 + Y•Q1' + X'•Y'•Q1 + Y'•Q1•Q0' + X'•Q1•Q0 + Y•Q1•Q0
$Q1^+$ = X•Q1'•Q0 + Y•Q1' + Y•Q0 + X'•Q1•Q0 + Y'•Q1•Q0' (minimization)

3. Determining the expression of the output function G.

Z = X•Q1•Q0 + Y•Q1'•Q0'

State/Output Table:

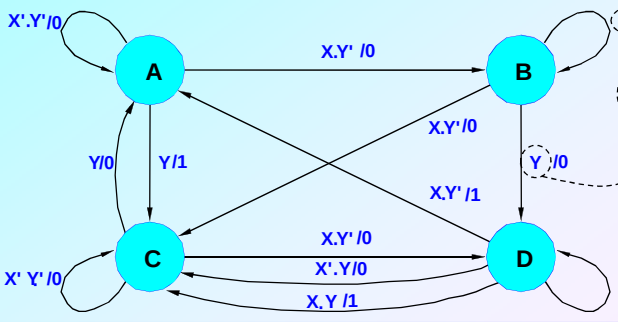
$Q1^+$ $Q0^+$,Z

Q1Q0 \ XY	00	01	10	11
00	00,0	10,1	01,0	10,1
01	01,0	11,0	10,0	11,0
10	10,0	00,0	11,0	00,0
11	11,0	10,0	00,1	10,1

S^+ ,Z

S \ XY	00	01	10	11
A	A,0	C,1	B,0	C,1
B	B,0	D,0	C,0	D,0
C	C,0	A,0	D,0	A,0
D	D,0	C,0	A,1	C,1

State Transition Diagram:

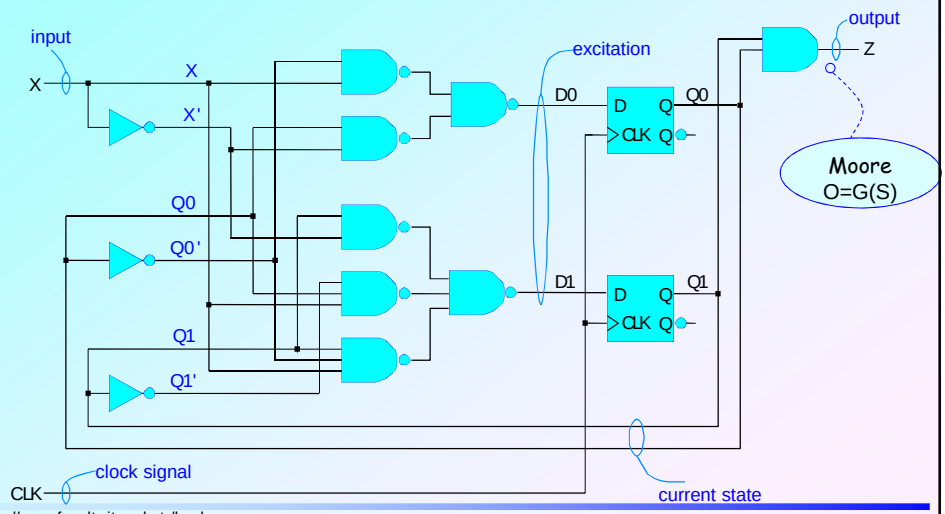


Meaning of some input symbols:
X'·Y' means X=0, Y=0
Y means X=Φ, Y=1
Actually it represents two input combinations:
X=0, Y=1 and X=1, Y=1

Analysis of a clocked synchronous sequential circuit designed according to Moore model:

Remember, in Moore model output depends only to current state.

In the circuit below, output Z depends only on state variables (Q1,Q0).



Analysis of circuits designed with Moore model is very similar to Mealy model.
Only construction and interpretation of the state/output table are different.

1. Determining the expression of F function that drives the flip-flops:

$D0 = Q0 \bullet X' + Q0' \bullet X$

$D1 = Q1 \bullet X' + Q1' \bullet Q0 \bullet X + Q1 \bullet Q0' \bullet X$

2. Next state $S^+=\{Q0(t^+), Q1(t^+)\}$ expressions.

$Q0^+ = D0$

$Q1^+ = D1$

$Q0^+ = Q0 \bullet X' + Q0' \bullet X$

$Q1^+ = Q1 \bullet X' + Q1' \bullet Q0 \bullet X + Q1 \bullet Q0' \bullet X$

3. Transition table and state table are constructed.

$Q1^+ Q0^+$ / Q1Q0	X = 0	X = 1
00	00	01
01	01	10
10	10	11
11	11	00

For simplicity alphanumeric names are assigned to state codes.

S^+ / S	X = 0	X = 1
A	A	B
B	B	C
C	C	D
D	D	A

S: Current state S^+: Next state Q1 and Q0: State variables

4. Determining the expression of the output function G

Z = Q1•Q0 (**Moore** model; output depends only on state variables.)

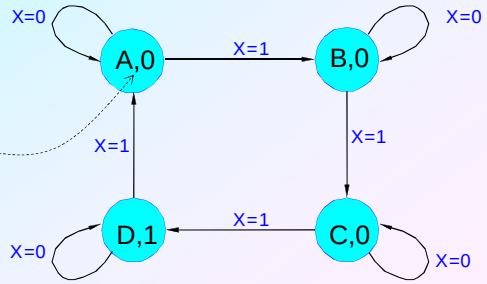
5. Constructing the State/Output table

S^+ / X / S	0	1	Z
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1

Since in Moore model output depends only on state, only one output value is written in each row, independently from inputs.

Each row corresponds to a state.

In the state diagram of a circuit in Moore model, output values are written inside the state circles, since they are functions of state only.



(Compare to diagram in 7.7)

Interpretation of Outputs in Mealy and Moore Models

If you check the output of a digital circuit at a certain moment you will always read a logical value 0 or 1 (except high impedance outputs).

But this value may not be valid due to some reasons for example due to internal delays. (The circuit has not finished its job yet.)

Therefore it is important when to read (sample) an output.

In clocked synchronous sequential circuits outputs are sampled (read) in different times dependent on the model (Mealy or Moore).

Mealy Model:

Since the output depends also on input, if the input changes the output also changes at the same time (actually after the propagation delay).

Working steps of a circuit in Mealy model:

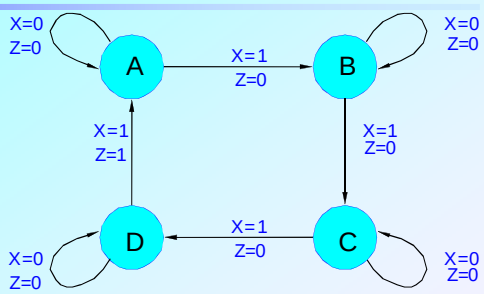
1. Input values (I) are given.
2. **Output values are obtained** as a function of input and current state. O=G(S,I)
3. Clock signal gets active. For example positive edge (0 to 1 transition).
4. The machine goes to the next state.
   Next state is a function of input and current state. S^+=F(S,I)

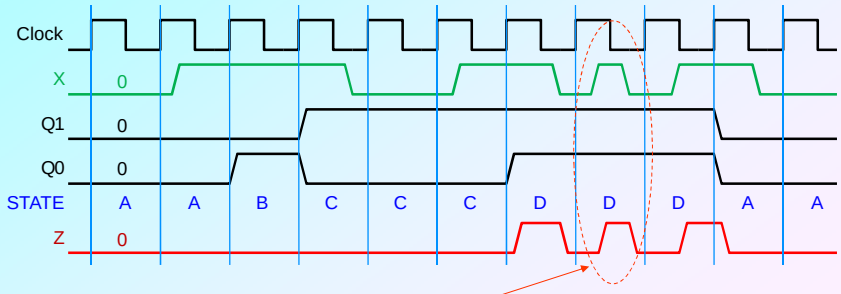
Example: The timing diagram of the sequential circuit designed according to Mealy model with the given state diagram is shown below.

State Coding:

Q_1Q_0

0 0 : A
0 1 : B
1 0 : C
1 1 : D





Output changes at the same time with the input.

Moore Model:

Since the output is the function of the state only, in Moore model change in the input cannot affect the output immediately.

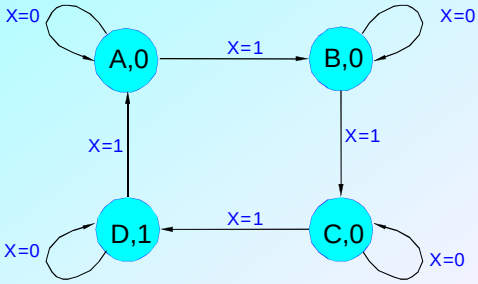
The effect of changes in input can be seen on the output just after the change in the state.

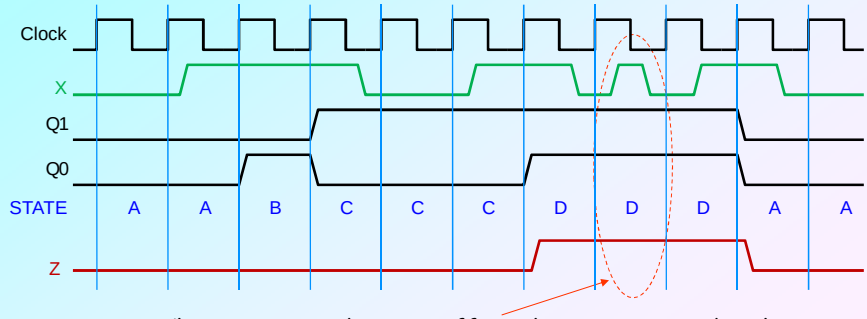
Working steps of a circuit in Moore model:

1. Input values (I) are given.
2. Clock signal gets active. For example positive edge (0 to 1 transition).
3. The machine goes to the next state. Next state is a function of input and current state. $S^+=F(S,I)$
4. **Output value is determined** as a function of the **new state**. O=G(S)

In Moore model, effect of changes in inputs are seen after one clock pulse.

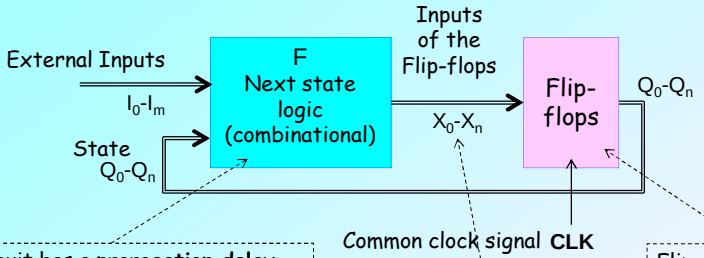
Example: The timing diagram of the sequential circuit designed according to Moore model with the given state diagram is shown below.





Change in input does not effect the output immediately.

The Role of the Clock Signal



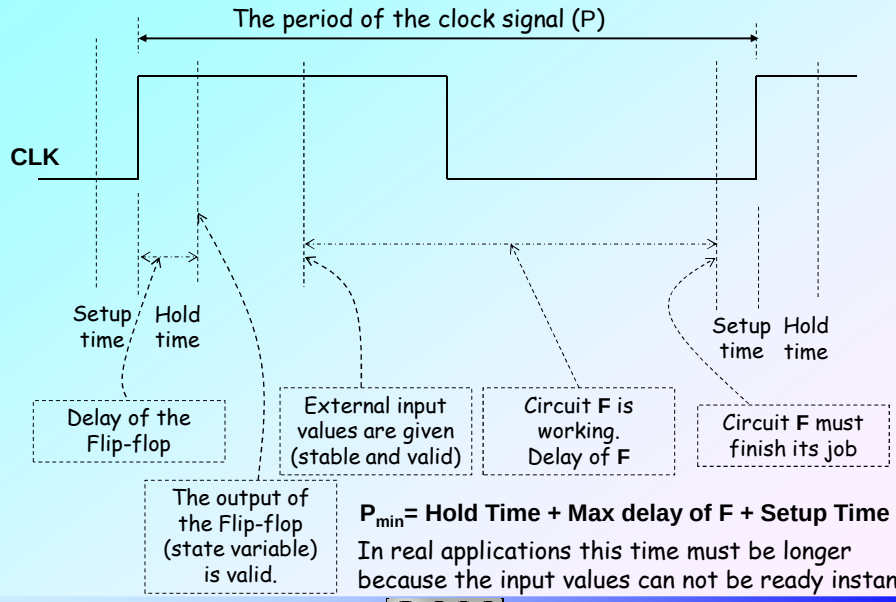
This circuit has a **prorogation delay**. The output values are not always valid. There may be also hazard problem.

These values must be stable and valid when the clock signal is active (for example rising edge).

Flip-flops also have propagation delays. Setup time, hold time.

- The speed (period) of the clock signal is determined according the maximum delay (longest path) of the **F** circuit.
- Before the clock signal is active (for example a rising edge comes) the circuit **F** must finish its job and the inputs of the flip-flops must be stable and valid.
- Possible hazards in **F** must also be terminated before the clock signal gets active.

Determining the speed (period) of the clock signal



P_{min}= Hold Time + Max delay of F + Setup Time

In real applications this time must be longer because the input values can not be ready instantly.