BLG222E – Computer Organization

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For administrative issues please send email to the teaching assistants.

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Web Site:

• Official website of the course is in the Ninova e-learning system. (http://ninova.itu.edu.tr)

• Students that are registered to the course can enter the system using their İTÜ user ids and passwords.

• All lecture notes, announcements, grades and assignments are published in the Ninova system.

• Continuously check your İTÜ mailbox. Mails about assignments and announcements are sent to the İTÜ accounts. If you use another mail account forward your İTÜ mails to your valid account.

How to forward your İTÜ email:
http://bidb.itu.edu.tr/yardim/sikca-sorulan-sorular

Academic dishonesty:

Disciplinary regulations of The Council of Higher Education and of the university are applied.

Syllabus

Textbook: Computer System Architecture, Morris Mano, 3rd edition

Grading:

3 Projects	30 %
2 Midterms	30 %
Final	40 %

Ninova: http://ninova.itu.edu.tr/Ders/3557/Sinif/25485

In order to take the final exam:

- All 3 projects should be submitted. A project is assumed to be submitted if 3 points (out of 10) is given.
- Total midterm grade (midterm 1+midterm 2) should be equal or higher than 10 (out of 30).
- Total grades (midterm 1+midterm 2+project) should be equal or higher than 25 (out of 60).

Course Objectives

The course objective is to provide knowledge to **design and build a digital computing machine** with the background of digital circuits and logic.

The students will get the understanding of computer operation, design principles, and how physical definition and software are interrelated in computer system.

Tentative course outline

1) Introduction, combinational circuits, decoders, multiplexers **(1.1-2.3)**
2) Registers, ripple counters, memory units **(2.4, 2.5, 2.6, 2.7)**
3) Register transfer language (RTL), Bus, memory transfers **(4.1, 4.2, 4.3)**
4) Arithmetic operations, logical operations, shift operations, ALU **(4.4, 4.5, 4.6, 4.7)**
5) Instruction codes, timing and control, instruction cycles **(5.1-5.5)**
6) Memory-reference instructions, IO instructions **(5.6, 5.7)**
7) Midterm 1
----------BREAK----------
8) Design of a complete computer **(5.8, 5.9, 5.10)**
9) Micro-programmed control, address sequencing **(7.1, 7.2)**
10) Design of control unit **(7.3,7.4)**
11) Stack organization, reverse polish notation **(8.3)**
12) Midterm 2
13) Algoritmic state machines
14) RISC/CISC processors

Tentative course outline

1) Introduction, combinational circuits, decoders, multiplexers **(1.1-2.3)**
2) Registers, ripple counters, memory units **(2.4, 2.5, 2.6, 2.7)** ***Assignment1***
3) Register transfer language (RTL), Bus, memory transfers **(4.1, 4.2, 4.3)**
4) Arithmetic operations, logical operations, shift operations, ALU **(4.4, 4.5, 4.6, 4.7)**
5) Instruction codes, timing and control, instruction cycles **(5.1-5.5)**
Deadline1
6) Memory-reference instructions, IO instructions **(5.6, 5.7)** ***Assignment2***
7) Midterm 1
----------BREAK----------
8) Design of a complete computer **(5.8, 5.9, 5.10)**
9) Micro-programmed control, address sequencing **(7.1, 7.2)** ***Deadline2***
10) Design of control unit **(7.3,7.4)** ***Assignment3***
11) Stack organization, reverse polish notation **(8.3) Demo**
12) Midterm 2
13) Algoritmic state machines
14) RISC/CISC processors ***Deadline3***