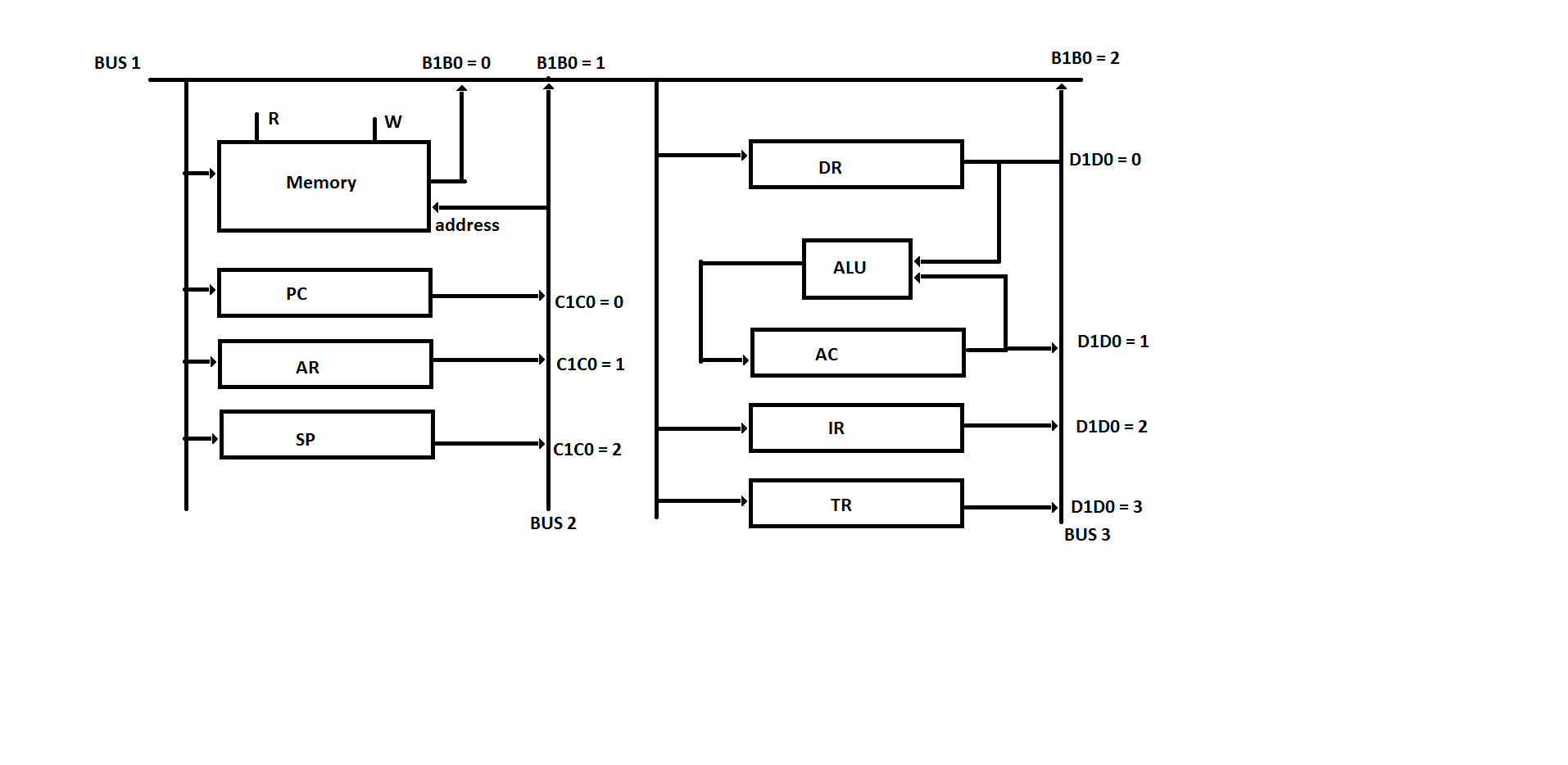
**A, B, C and D should be solved according to the following architecture and information.**



There are 3 16-bit common busses (BUS1, BUS2 and BUS3). BUS2 and BUS3 are connected to BUS1. All register except AC, can be loaded from BUS1.

**PSH:** Instruction decrements the value of the stack register (SP) by ones, and then write the content into the memory cell.

**PULL:** Instruction loads a value into DR from the memory cell whose address be pointed by SP, and then increments the value of the stack register (SP) by one.

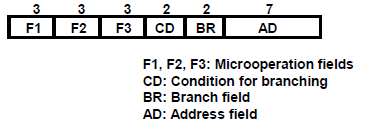
**C:\Users\akeli\AppData\Local\Microsoft\Windows\INetCache\Content.Word\Captutgfre.jpg**

**For Part C use the following information:**

The hardware based control unit, the opcode bits from IR is connected an opcode decoder and output signals from K0 to K13**.**

**For Part D use the following information:**

The microinstruction format of the software based control unit is as follows:



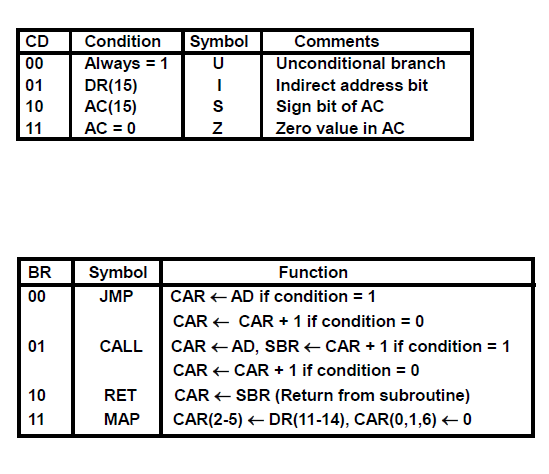
Microoperations for F1, F2 and F3 are gives as following:

|  |  |  |
| --- | --- | --- |
| F1 | Microoperation | Symbol |
| 000 | None | NOP |
| 001 | AC AC + DR | ADD |
| 010 | AC 0 | CLRAC |
| 011 | AC AC + 1 | INCAC |
| 100 | AC DR | DRTAC |
| 101 | AC DR(0-10) | DRTAR |
| 110 | AC PC | PCTAR |
| 111 | M[AR] DR | WRITE |

|  |  |  |
| --- | --- | --- |
| F2 | Microoperation | Symbol |
| 000 | None | NOP |
| 001 | AC AC - DR | SUB |
| 010 | SP SP + 1 | INCSP |
| 011 | SP SP - 1 | DECSP |
| 100 | DR M[AR] | READ |
| 101 | DR AC | ACTDR |
| 110 | DR DR + 1 | INCDR |
| 111 | DR(0-10) PC | PCTDR |

|  |  |  |
| --- | --- | --- |
| F3 | Microoperation | Symbol |
| 000 | None | NOP |
| 001 | AC AC DR | ADD |
| 010 | AC | CLRAC |
| 011 | PC SP | SPTPC |
| 100 | SP AR | ARTSP |
| 101 | PC PC + 1 | INCPC |
| 110 | PC AR | ARTPC |
| 111 | AR SP | SPTAR |

Consider for conditional branches (BR) and condition field (status bit) CD as follows:





**Part C** For a hardware based control unit, each register have control signal for load (LD), increment (INC) and clear (CLR). However, they do not have any control signal for decrementing.

**Hint:** Value of the register can be decremented to transfer its value to AC, clearing and increasing the value of the DR such that DR 1, complementing the value of the DR and adding DR to AC. However, the content of the DR should be preserved and then should be transferred to the stack memory.

1. (5 pts) Write the stack operation of PSH (Opcode=101) and PULL (Opcode = 110) using RTL.
2. (5 pts) Write the value of control signals () for each cycle.

