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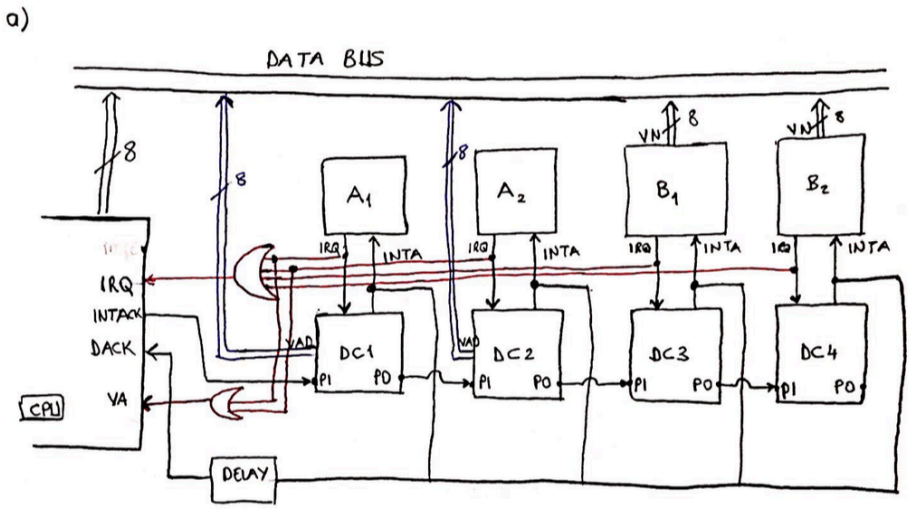
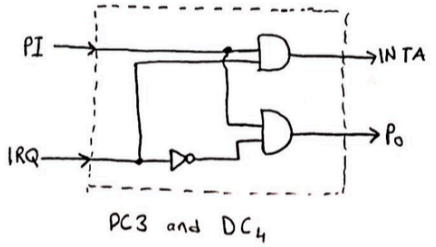
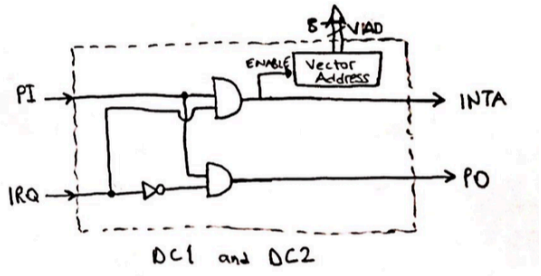
BLG 322E - Computer Architecture
Assignment 3

Due Date: 18.04.2018, Wednesday, 22:00

a) Design and draw the system with the CPU, 4 devices (A1, A2, B1, B2) and the priority interrupt controller. First, show the priority interrupt controller only as a box. Then design and draw the internal structure of the priority interrupt controller using logical gates.







b) Assume that the devices A1 and B1 assert their interrupt requests at the same time. Show step by step all the signals that are sent in the system until the requests of both devices has been fulfilled.

- IRQ(A1) = 1, IRQ(B1) = 1, IRQ(CPU) = 1
- INTACK(CPU) = 1, PI(DC1) = 1, INTA(A1) = 1, VAD(DC1)=1(Active), DACK(CPU) = 1
- IRQ(B1) = 1, IRQ(CPU) = 1
- INTACK(CPU) = 1, PI(DC1) = 1, PI(DC2) = 1, PI(DC3) = 1, INTA(B1) = 1, VN(B1)=1 (Active), DACK(CPU) = 1

PS: All other signals are zero.

c) How does the CPU determine the start address of the interrupt service routine to be run if the interrupt source is a device of type A or of type B ?

Type A: This type of devices does not have a vector number output (VN or VAD), so these devices works in auto-vectored mode. Daisy-Chain devices that are linked to type-a sources have vector address table, and send the address to data bus, then make the DACK signal active, then CPU reads the address from data bus, and determines the start address of the ISR.

Type B: This type of devices have a vector number output (VN or VAD).When the interrupt request is accepted, the device sends the vector address to data bus directly, and makes the DACK signal active, then CPU reads the address from data bus, and determines the start address of the ISR.