

# Homework-2 Solutions - EHB322E

## a) • Complex Gate Circuit

$$f = x_1 x_2 \bar{x}_4 + x_1 \bar{x}_2 x_3 + x_2 x_3 \bar{x}_4 \rightarrow \bar{f} = \bar{f} \rightarrow f = \overline{x_1 x_2 \bar{x}_4 + x_1 \bar{x}_2 x_3 + x_2 x_3 \bar{x}_4}$$

$$f = \overline{x_1 x_2 \bar{x}_4 \cdot x_1 \bar{x}_2 x_3 \cdot x_2 x_3 \bar{x}_4} = \overline{(\bar{x}_1 + \bar{x}_2 + x_4) \cdot (\bar{x}_1 + x_2 + \bar{x}_3) \cdot (\bar{x}_2 + \bar{x}_3 + x_4)}$$

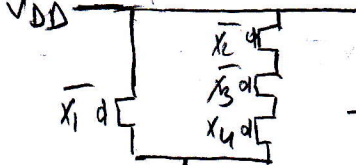
$$f = \overline{(\bar{x}_1 + \bar{x}_2 \bar{x}_3 + x_2 x_4 + \bar{x}_3 x_4) \cdot (\bar{x}_2 + \bar{x}_3 + x_4)}$$

$$f = \overline{\bar{x}_1 \bar{x}_2 + \bar{x}_1 \bar{x}_3 + \bar{x}_1 x_4 + \bar{x}_2 \bar{x}_3 + x_2 x_4 + \bar{x}_3 x_4} \rightarrow \text{for Pull-Down network}$$

$$= \bar{x}_1 (\bar{x}_2 + \bar{x}_3 + x_4) + \bar{x}_3 (\bar{x}_2 + x_4) + x_2 x_4$$

⇒ Dual of this expression;

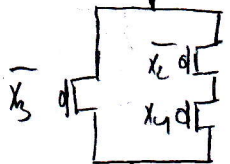
$$V_{DD} \left[ \bar{x}_1 + (\bar{x}_2 \cdot \bar{x}_3 \cdot x_4) \right] \cdot \left[ \bar{x}_3 + \bar{x}_2 \cdot x_4 \right] \cdot \left[ x_2 + x_4 \right]$$



→ Pull-up  
worst case  
6 transistors

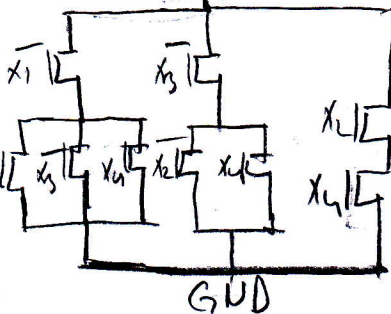
$$b) t_{PLH}(wc) = 0.69 \cdot 6 \cdot 2 \cdot 6 \cdot 10^3 \cdot 10 \cdot 10^{-12}$$

$$= 107,64 \text{ ns}$$



$$t_{PHL}(wc) = 0.69 \cdot 2 \cdot 4 \cdot 7 \cdot 10^3 \cdot 10 \cdot 10^{-12}$$

$$= 64,86 \text{ ns}$$



→ Pull-down  
worst case  
2 transistors

$$\text{NMOS PTL} \rightarrow f = x_1 x_2 \bar{x}_4 + x_1 \bar{x}_2 x_3 + x_2 x_3 \bar{x}_4$$

Shannon expansion  $x_4 \rightarrow x_3 \rightarrow x_2 \rightarrow x_1$

$$\Rightarrow x_1 x_2 \bar{x}_4 (x_3 + \bar{x}_3) + x_1 \bar{x}_2 x_3 (x_4 + \bar{x}_4) + x_2 x_3 \bar{x}_4 (x_1 + \bar{x}_1)$$

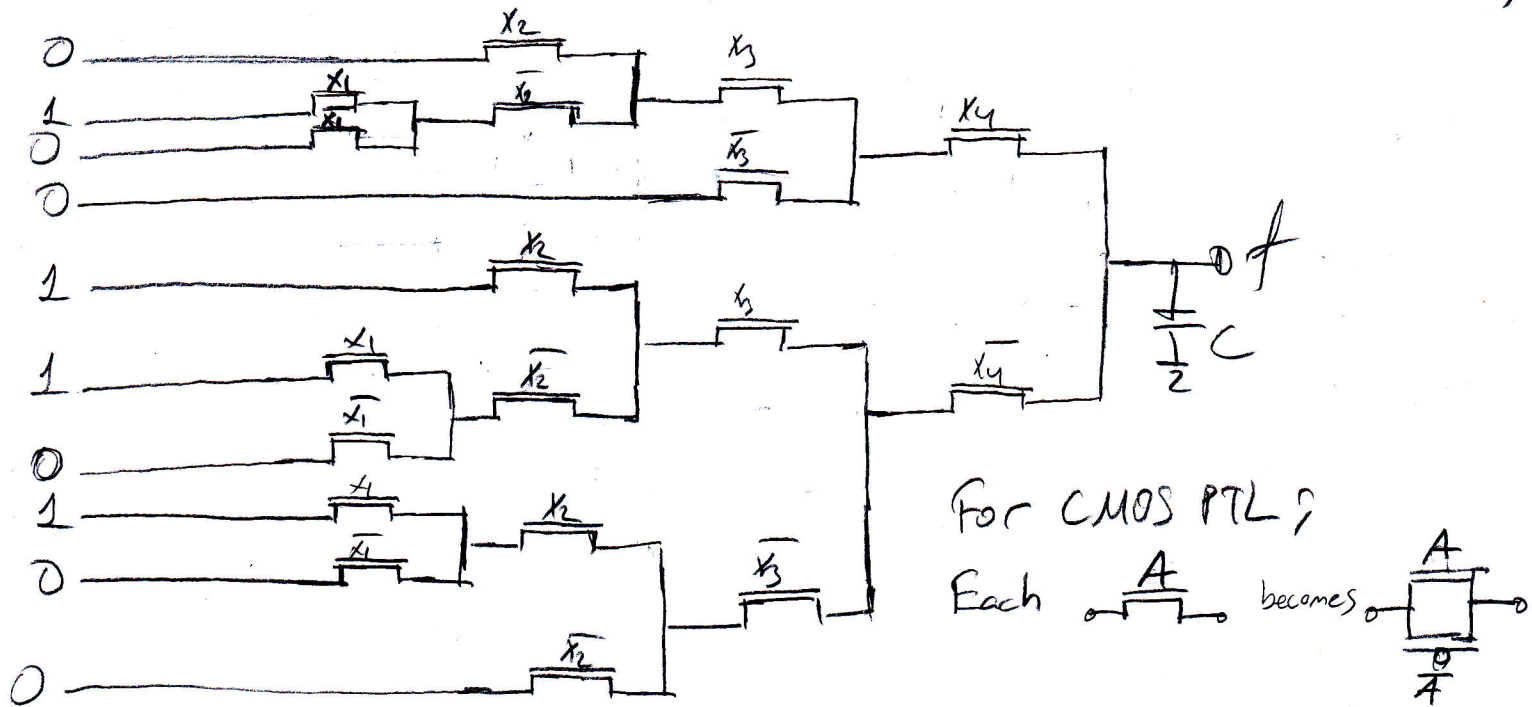
$$\Rightarrow x_1 x_2 x_3 \bar{x}_4 + x_1 x_2 \bar{x}_3 \bar{x}_4 + x_1 \bar{x}_2 x_3 x_4 + x_1 \bar{x}_2 x_3 \bar{x}_4 + \cancel{x_1 x_2 x_3 x_4} + \bar{x}_1 x_2 x_3 \bar{x}_4$$

$$\Rightarrow x_4 (x_1 \bar{x}_2 x_3) + \bar{x}_4 (x_1 x_2 x_3 + x_1 x_2 \bar{x}_3 + x_1 \bar{x}_2 x_3 + \bar{x}_1 x_2 x_3)$$

$$x_4 (x_3 (x_1 \bar{x}_2) + \bar{x}_3 (0)) + \bar{x}_4 (x_3 (x_1 x_2 + x_1 \bar{x}_2 + \bar{x}_1 x_2) + \bar{x}_3 (x_1 x_2))$$

$$x_4 (x_3 (x_2(0) + \bar{x}_2(x_1)) + \bar{x}_3(0)) + \bar{x}_4 (x_3 (x_2(x_1 + \bar{x}_1) + \bar{x}_2(x_1)) + \bar{x}_3 (x_2(x_1) + \bar{x}_2(0)))$$

$$x_4 (x_3 (x_2(0) + \bar{x}_2(x_1(1) + \bar{x}_1(0))) + \bar{x}_3(0)) + \bar{x}_4 (x_3 (x_2(1) + \bar{x}_2(x_1(1) + \bar{x}_1(0))) + \bar{x}_3 (x_2(x_1(1) + \bar{x}_1(0)) + \bar{x}_2(0)))$$



b) NMOS PTL  $\rightarrow t_{PLHCWC} = 0.69 \cdot t \cdot R_n \cdot C_{out} = 0.69 \cdot t \cdot t_1 \cdot 7 \cdot 10^3 \cdot 10 \cdot 10^{-12}$   
 $= 129,72 \text{ ns}$

$\hookrightarrow$  4 transistors  
on  $H \rightarrow L$  and  $L \rightarrow H$   
paths

$$t_{PHLCWC} = 0.69 \cdot t \cdot R_n \cdot C_{out} = 129,72 \text{ ns}$$

b) CMOS PTL  $\rightarrow t_{PLHCWC} = 0.69 \cdot t \cdot (R_n \parallel R_p) \cdot C_{out} = 0.69 \cdot t \cdot (4,7 \cdot 10^3 \parallel 26 \cdot 10^3)$   
 $= 0.69 \cdot t \cdot 1677 \cdot 10 \cdot 10^{-12} = 116,28 \text{ ns}$

$\hookrightarrow$  4 transmission  
gates on  $H \rightarrow L$   
and  $L \rightarrow H$  paths

$$t_{PHLCWC} = 0.69 \cdot t \cdot (R_n \parallel R_p) \cdot C_{out} = 116,28 \text{ ns}$$