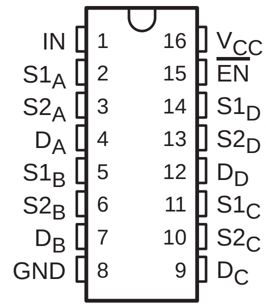
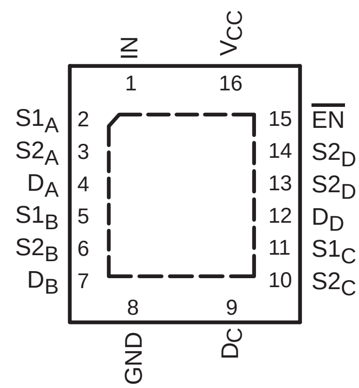
- **Low Differential Gain and Phase (D_G = 0.64%, D_P = 0.1 Degrees Typ)**
- **Wide Bandwidth (BW = 300 MHz Min)**
- **Low Crosstalk (X_{TALK} = −63 dB Typ)**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on} = 3 Ω Typ)**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both RGB and Composite-Video Switching**

D, DBQ, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The TI TS5V330 video switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the D port is connected to the S port. When $\overline{EN}$ is high, the switch is disabled and the high-impedance state exists between the D and S ports. The select (IN) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	TS5V330RGYR	TE330
	SOIC − D	Tube	TS5V330D	TS5V330
		Tape and reel	TS5V330DR	
	SSOP (QSOP) − DBQ	Tape and reel	TS5V330DBQR	TE330
	TSSOP − PW	Tube	TS5V330PW	TE330
		Tape and reel	TS5V330PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Low differential gain and phase make this switch ideal for composite and RGB video applications. This device has wide bandwidth and low crosstalk, making it suitable for high-frequency applications as well.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. This switch maintains isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{EN}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS		INPUT/OUTPUT D	FUNCTION
$\overline{EN}$	IN		
L	L	S1	D port = S1 port
L	H	S2	D port = S2 port
H	X	Z	Disconnect

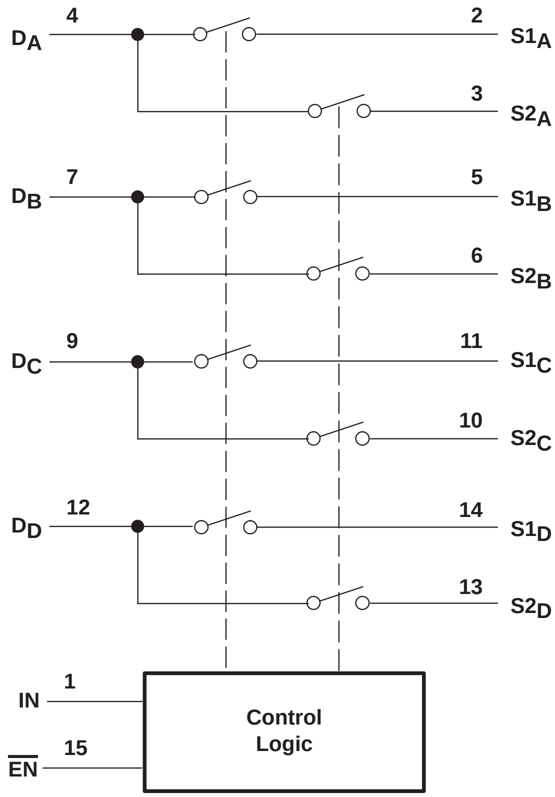
PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
S1, S2	Analog video I/Os
D	Analog video I/Os
IN	Select input
$\overline{EN}$	Switch-enable input

PARAMETER DEFINITIONS

PARAMETER	DESCRIPTION
r_{on}	Resistance between the D and S ports, with the switch in the ON state
I_{OZ}	Output leakage current measured at the D and S ports, with the switch in the OFF state
I_{OS}	Short-circuit current measured at the I/O pins
V_{IN}	Voltage at the IN pin
V_{EN}	Voltage at the $\overline{EN}$ pin
C_{IN}	Capacitance at the control ($\overline{EN}$, IN) inputs
C_{OFF}	Capacitance at the analog I/O port when the switch is OFF
C_{ON}	Capacitance at the analog I/O port when the switch is ON
V_{IH}	Minimum input voltage for logic high for the control ($\overline{EN}$, IN) inputs
V_{IL}	Minimum input voltage for logic low for the control ($\overline{EN}$, IN) inputs
V_{hys}	Hysteresis voltage at the control ($\overline{EN}$, IN) inputs
V_{IK}	I/O and control ($\overline{EN}$, IN) inputs diode clamp voltage
V_I	Voltage applied to the D or S pins when D or S is the switch input
V_O	Voltage applied to the D or S pins when D or S is the switch output
I_{IH}	Input high leakage current of the control ($\overline{EN}$, IN) inputs
I_{IL}	Input low leakage current of the control ($\overline{EN}$, IN) inputs
I_I	Current into the D or S pins when D or S is the switch input
I_O	Current into the D or S pins when D or S is the switch output
I_{off}	Output leakage current measured at the D or S ports, with V_{CC} = 0
t_{ON}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON
t_{OFF}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF
BW	Frequency response of the switch in the ON state measured at −3 dB
X_{TALK}	Unwanted signal coupled from channel to channel. Measured in −dB. X_{TALK} = 20 log V_O/V_I. This is a nonadjacent crosstalk.
O_{IRR}	Off isolation is the resistance (measured in −dB) between the input and output with the switch OFF.
D_G	Magnitude variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V.
D_P	Phase variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V.
I_{CC}	Static power-supply current
I_{CCD}	Variation of I_{CC} for a change in frequency in the control ($\overline{EN}$, IN) inputs
ΔI_{CC}	This is the increase in supply current for each control input that is at the specified voltage level, rather than V_{CC} or GND.

functional diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	73°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage ($\overline{EN}$, IN)	2	5.5	V
V_{IL}	Low-level control input voltage ($\overline{EN}$, IN)	0	0.8	V
V_{ANALOG}	Analog I/O voltage	0	2	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{EN}$, IN	V_{CC} = 4.5 V,	I_{IN} = −18 mA					−1.8	V
V_{hys}	$\overline{EN}$, IN						150		mV
I_{IH}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	V_{IN} and V_{EN} = V_{CC}					±1	μA
I_{IL}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	V_{IN} and V_{EN} = GND					±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF				±1	μA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V_{CC}, V_I = 0,	Switch ON		50			mA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				1	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0,	Switch ON or OFF				3	μA
ΔI_{CC}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND				2.5	mA
I_{CCD}		V_{CC} = 5.5 V, V_{EN} = GND,	D and S ports open,	V_{IN} input switching 50% duty cycle				0.25	mA/MHz
C_{IN}	$\overline{EN}$, IN	V_{IN} or V_{EN} = 0,	f = 1 MHz				3.5		pF
C_{OFF}	D port	V_I = 0,	f = 1 MHz, Outputs open	Switch OFF			6		pF
	S port						4		
C_{ON}		V_I = 0,	f = 1 MHz, Outputs open	Switch ON			14		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 1 V,	I_O = 13 mA,	R_L = 75 Ω		3	7	Ω
			V_I = 2 V,	I_O = 26 mA,	R_L = 75 Ω		7	10	

V_I, V_O, I_I, and I_O refer to I/O pins.
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ For I/O ports, I_{OZ} includes the input leakage current.
§ The I_{OS} test is applicable to only one ON channel at a time. The duration of this test is less than one second.
¶ Measured by the voltage drop between the D and S terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or S) terminals.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10%, R_L = 75 Ω, C_L = 20 pF (unless otherwise noted) (see Figure 5)

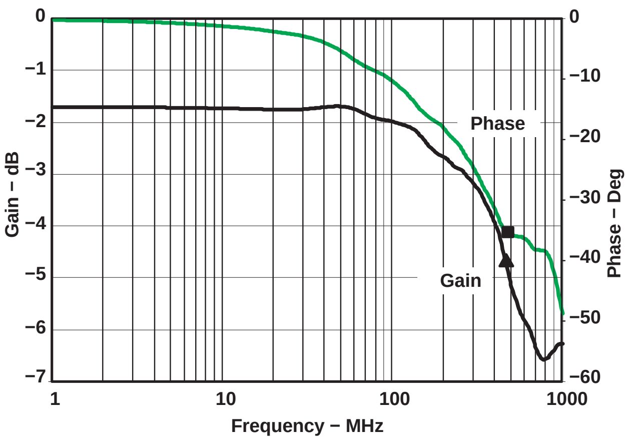
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{ON}	S	D		2.5	6	ns
t_{OFF}	S	D		1.1	6	ns

dynamic characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
D_G#	R_L = 150 Ω,	f = 3.58 MHz, see Figure 6			0.64		%
D_P#	R_L = 150 Ω,	f = 3.58 MHz, see Figure 6			0.1		Deg
BW	R_L = 150 Ω, see Figure 7			300			MHz
X_{TALK}	R_L = 150 Ω,	f = 10 MHz,	R_{IN} = 10 Ω, see Figure 8		−63		dB
O_{IRR}	R_L = 150 Ω,	f = 10 MHz, see Figure 9			−60		dB

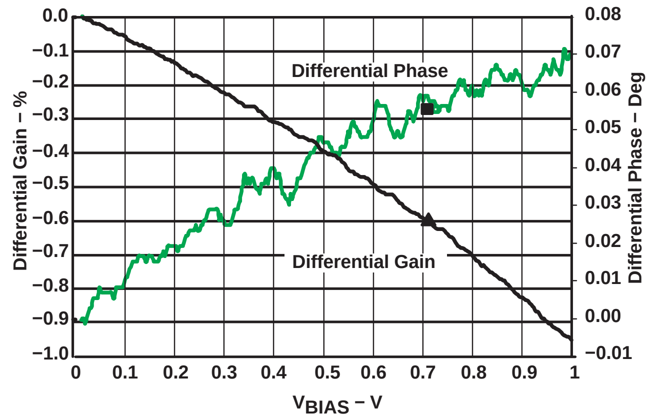
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
# D_G and D_P are expressed in absolute magnitude.

OPERATING CHARACTERISTICS



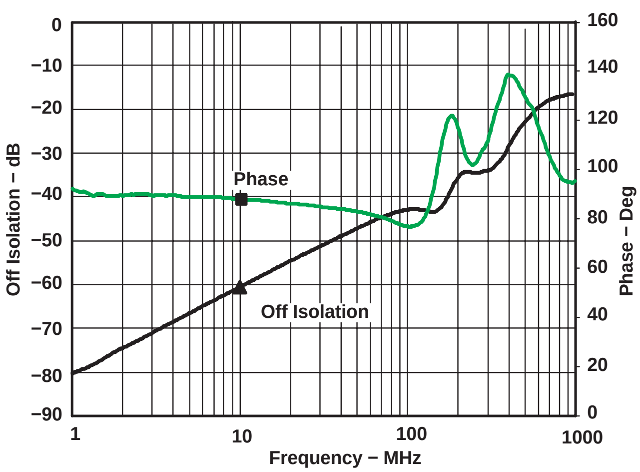
■ Phase at −3-dB Frequency, 35 Degrees
▲ Gain −3 dB at 460 MHz

Figure 1. Gain/Phase vs Frequency



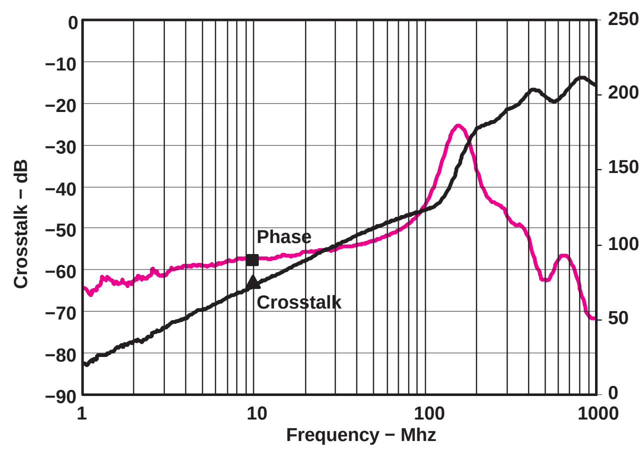
■ Differential Phase at 0.714, 0.056 Degree
▲ Differential Gain at 0.714, −0.63%

Figure 2. Differential Gain/Phase vs V_{BIAS}



■ Phase at 10 MHz, 88.5 Degrees
▲ Off Isolation at 10 MHz, −60 dB

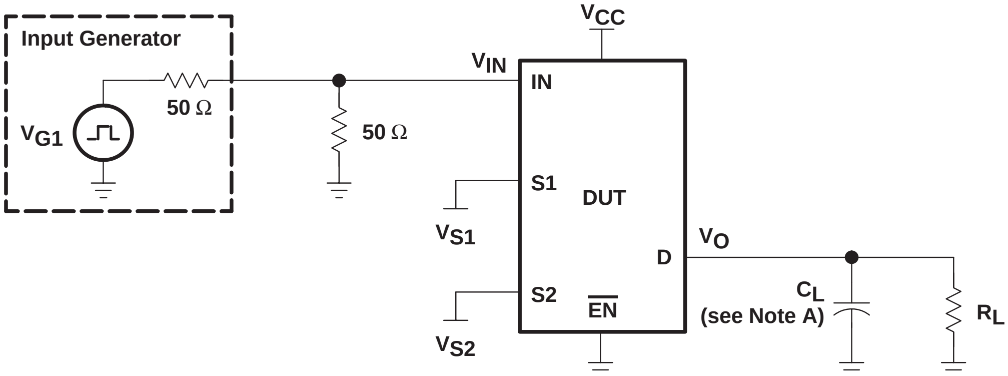
Figure 3. Off Isolation vs Frequency



■ Phase at 10 MHz, −90.4 Degrees
▲ Crosstalk at 10 MHz, −63.9 dB

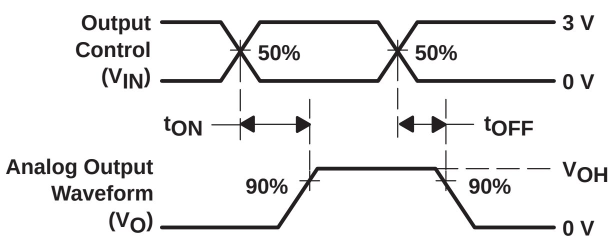
Figure 4. Crosstalk vs Frequency

PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	R_L	C_L	V_{S1}	V_{S2}
t_{ON}	5 V ± 0.5 V 5 V ± 0.5 V	75 75	20 20	GND 3 V	3 V GND
t_{OFF}	5 V ± 0.5 V 5 V ± 0.5 V	75 75	20 20	GND 3 V	3 V GND

TEST CIRCUIT

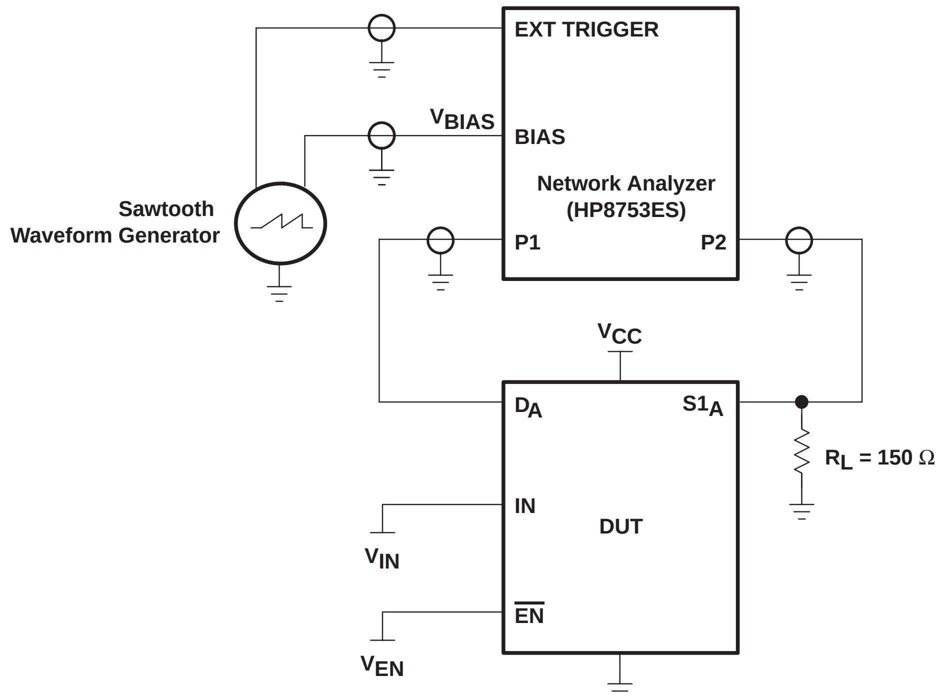


VOLTAGE WAVEFORMS
t_{ON} AND t_{OFF} TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For additional information on measurement method, refer to the TI application report, *Measuring Differential Gain and Phase*, literature number SLOA040.

Figure 6. Test Circuit for Differential Gain/Phase Measurement

Differential gain and phase are measured at the output of the ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at $S1_A$.

HP8753ES setup

Average = 20
RBW = 300 Hz
ST = 1.381 s
P1 = −7 dBM
CW frequency = 3.58 MHz

sawtooth waveform generator setup

V_{BIAS} = 0 to 1 V
Frequency = 0.905 Hz

PARAMETER MEASUREMENT INFORMATION

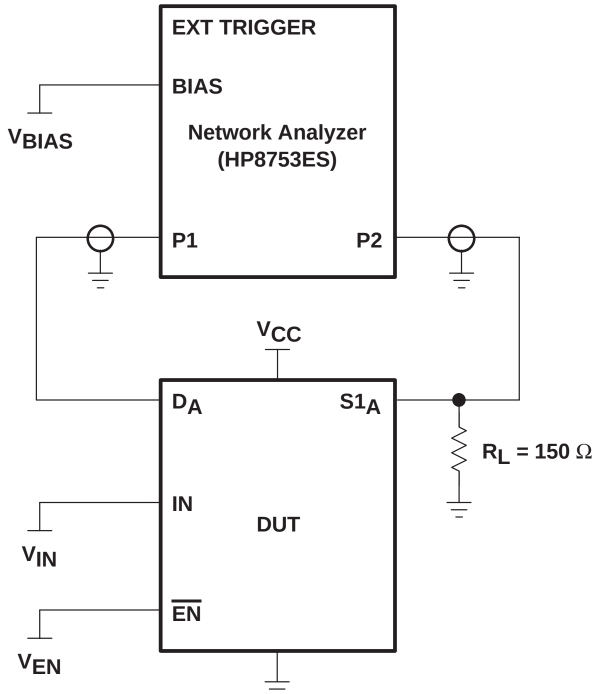


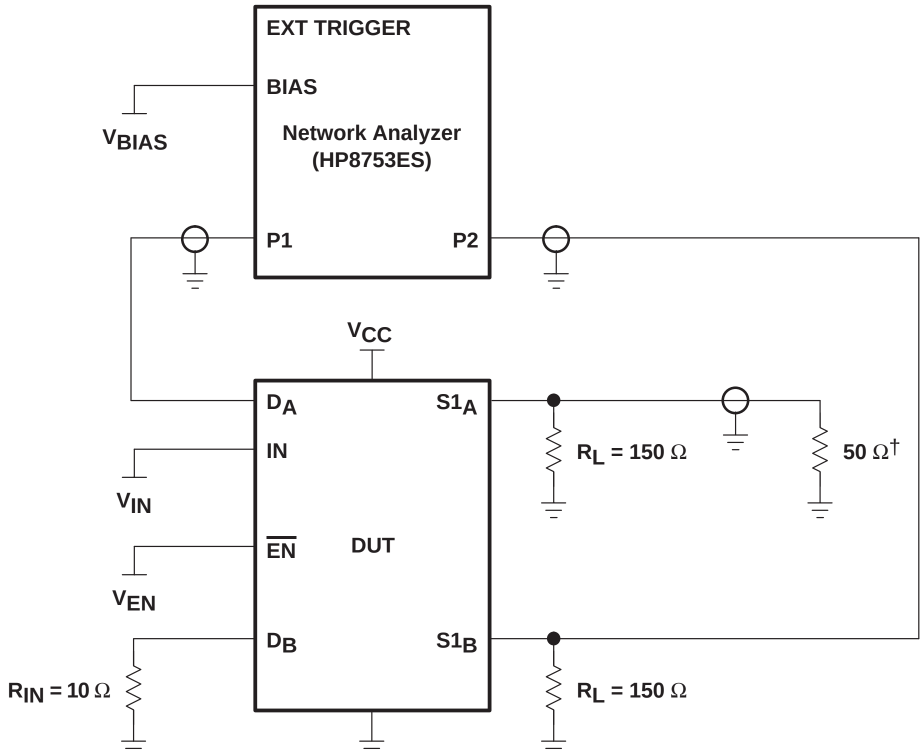
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at $S1_A$. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



† A 50-Ω termination resistor is needed for the network analyzer.

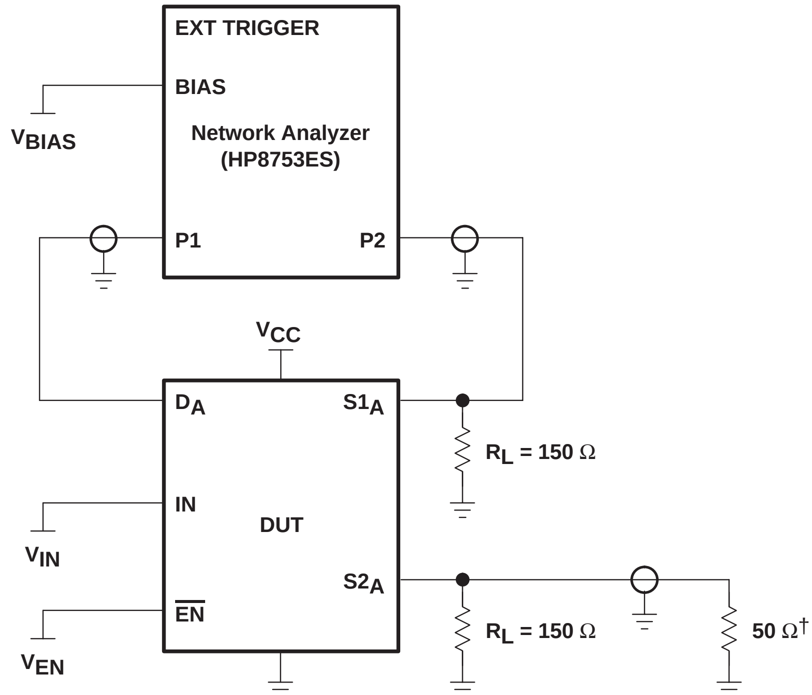
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at $S1_B$. All unused analog input (D) ports and output (S) ports are connected to GND through 10-Ω and 50-Ω pulldown resistors, respectively.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



† A 50-Ω termination resistor is needed for the network analyzer.

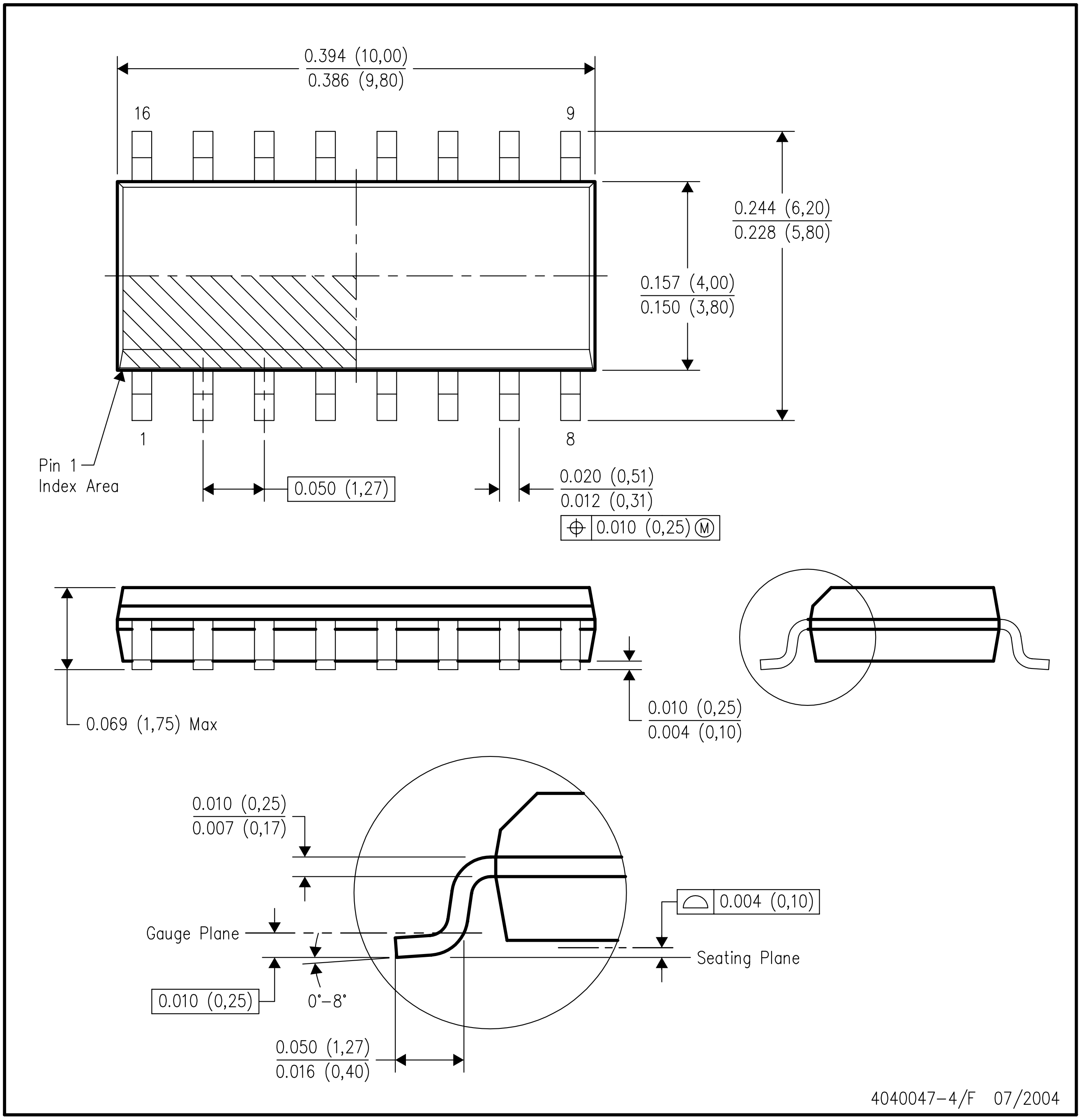
Figure 9. Test Circuit for Off Isolation (O_{IRR})

Off-isolation is measured at the output of the OFF channel. For example, when $V_{IN} = V_{CC}$, $V_{EN} = 0$, and D_A is the input, the output is measured at $S1_A$. All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

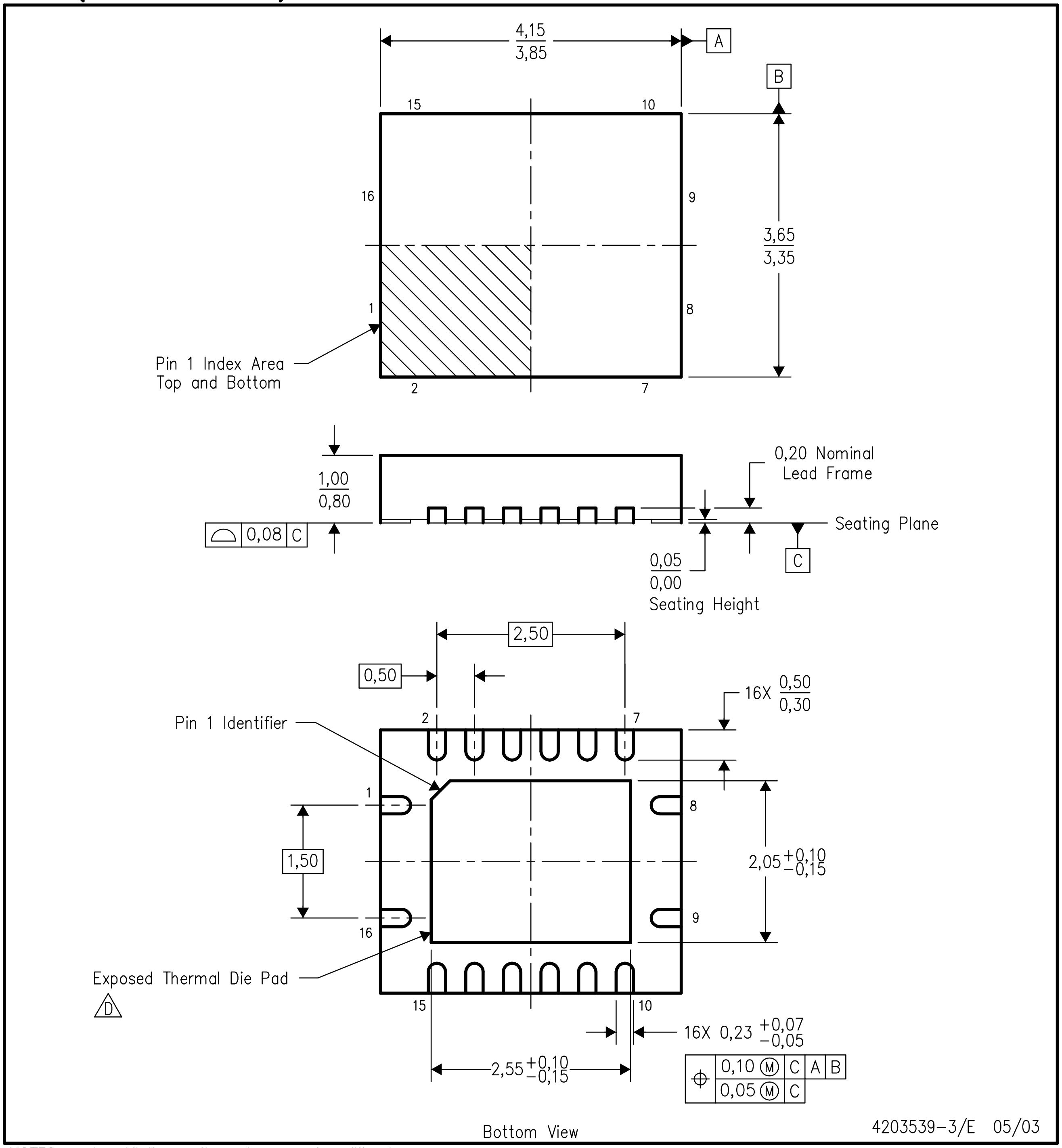
Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



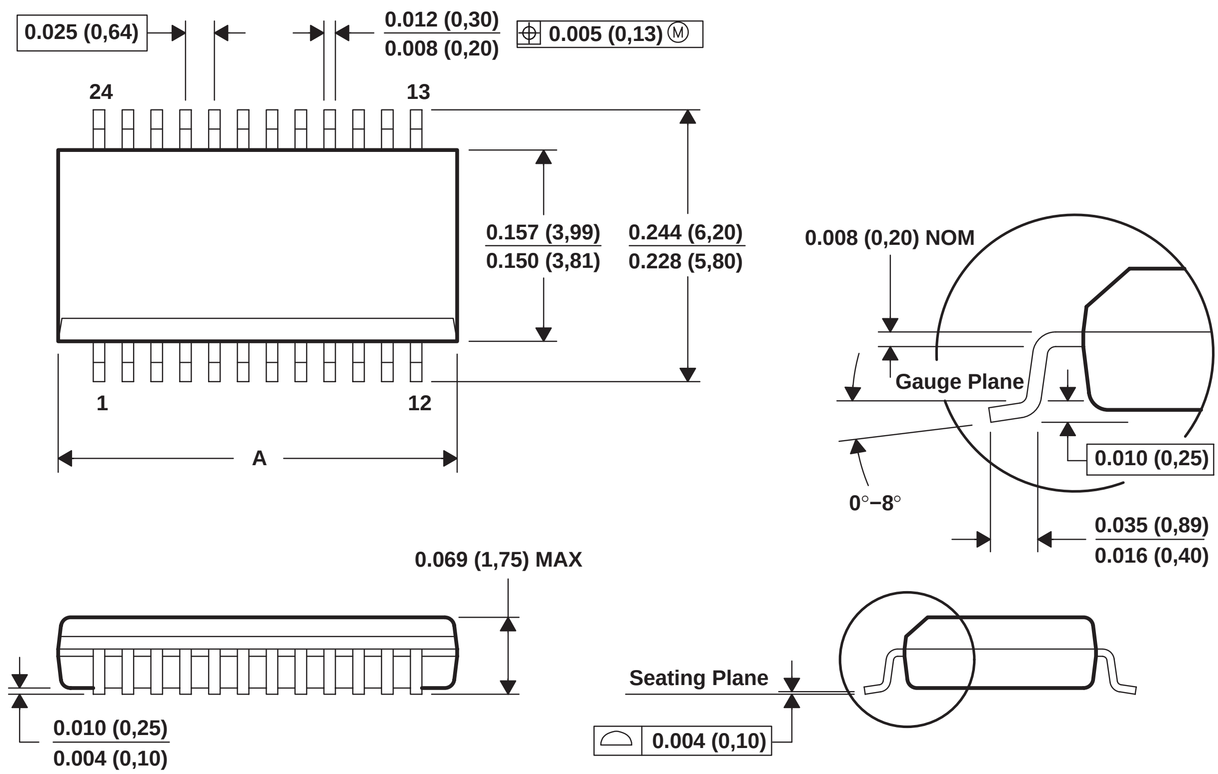
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Package complies to JEDEC MO-241 variation BB.

DBQ (R−PDSO−G)** **PLASTIC SMALL−OUTLINE PACKAGE**



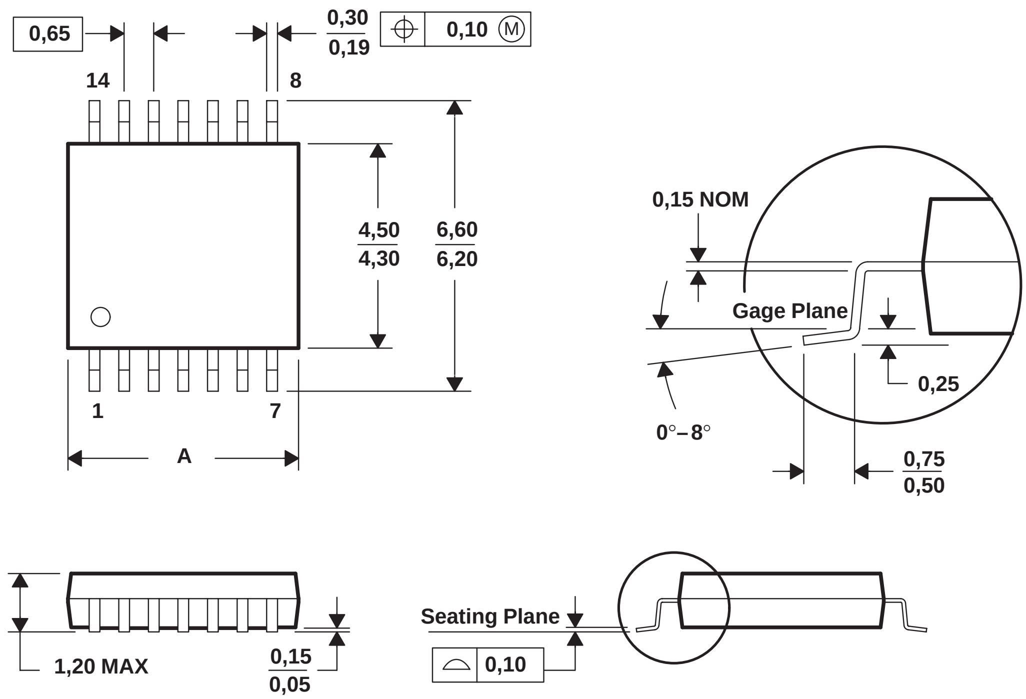
PINS ** / DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0−137 VARIATION	AB	AD	AE	AF

4073301/F 02/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−137.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153