Xi'an Jiaotong-Liverpool University

西交利物浦大學

PAPER CODE	EXAMINER	DEPARTMENT	TEL
CPT210	Jianjun Chen	Computing	81889137

2nd SEMESTER 2022/23 FINAL EXAMINATION

Undergraduate – Year 3

Microprocessor Systems

TIME ALLOWED: 2 Hours

INSTRUCTIONS TO CANDIDATES

1、 **This is a closed-book examination.**

2、 **Total marks available are 100. This will count for 70% in the final assessment.**

3、 **Answer all questions.**

4、 **Only English solutions are accepted.**

Condition codes

Code	Suffix	Flags	Meaning
0000	EQ	Z set	equal
0001	NE	Z clear	not equal
0010	CS	C set	unsigned higher or same
0011	CC	C clear	unsigned lower
0100	MI	N set	negative
0101	PL	N clear	positive or zero
0110	VS	V set	overflow
0111	VC	V clear	no overflow
1000	HI	C set and Z clear	unsigned higher
1001	LS	C clear or Z set	unsigned lower or same
1010	GE	N equals V	greater or equal
1011	LT	N not equal to V	less than
1100	GT	Z clear AND (N equals V)	greater than
1101	LE	Z set OR (N not equal to V)	less than or equal
1110	AL	(ignored)	always

Question A (20 Marks)

1. Convert 7.4375 into IEEE 754 single-precision format and explain how this number is stored on a big-endian platform. Please write down all intermediate steps clearly for the conversion and write down each byte (in hexadecimal) along with its corresponding memory address. The most significant byte of this number should be stored at 0x8000004D.

   (10 marks)

2. Explain what is "sign and magnitude" encoding and compare it against "two's complement" encoding, what are its advantages (or disadvantages)?

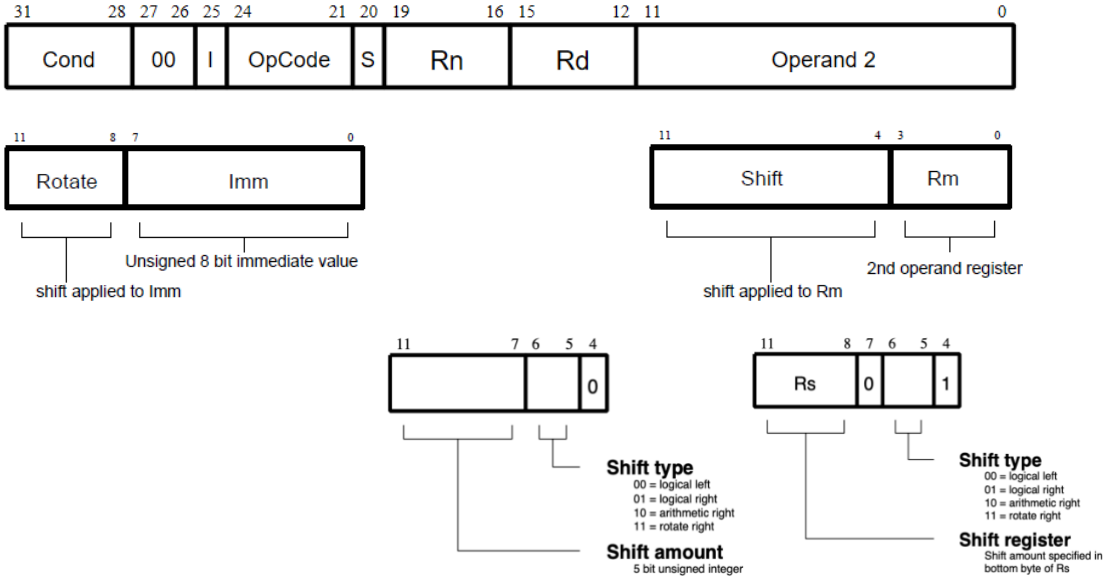
   (5 marks)

3. Convert -115 into sign and magnitude encoding and **one's** complement encoding. Assume that one byte is used to store this number. Please write down the conversion steps.

   (5 marks)

Question B (20 Marks)

Below is the encoding format of the ADD instruction in ARM.



1. If the bits for "Operand 2" are 0x7F1 and if the second operand is an immediate number, then what is the value of this immediate number? Please write down the detailed calculation steps.

   (8 marks)

2. If the bits for "Operand 2" are 0x170 and if the second operand is a register, can you extract all details about the second operand, such as the register involved and any shift operations applied? Please write down the details of how you find this out.

   (7 marks)

3. Explain what are banked registers? When are they available? What is the benefit of using such design?

   (8 marks)

Question C (30 Marks)

1. Write a program to calculate the sum of 16-bit unsigned integers stored in my_numbers and store the result in register R8. Assume that my_numbers is always 8 bytes long and the 2 words are stored in little endian ordering. When storing the result to R8, make sure that the most significant 16 bits of R8 are always zeros and the least significant 16 bits store the result. That is, overflows should not affect the upper 16 bits of R8. Your program should also set the C flag to 1 if unsigned overflow happens. Other flags are ignored when marking this question.

   (30 marks)

   Example 1:

   ```
   my_numbers      DCD         0x012A0022, 0x00112233
   ```

   Calculate: 0x012A + 0x0022 + 0x0011 + 0x2233 = 0x2390
   R8 = 0x00002390
   C flag = 0

   Example 2:

   ```
   my_numbers      DCD         0x00010002, 0x0003FFFA
   ```

   Calculate: 0x0001 + 0x0002 + 0x0003 + 0xFFFA = 0x10000
   R8 = 0x00000000
   C flag = 1

Question D (30 marks)

Given the following piece of ARM code and also assume a three-stage pipeline:

```
values    DCD     1,2,0
          adr     r0, values
          mov     r2, #0
loop      ldr     r1, [r0], #4
          add     r2, r2, r1, lsl r1
          cmp     r1, #0
          bne     loop
```

Note the following instruction cycle times:

Processing Type	Cycles
Any unexecuted (condition code fails)	S
Normal Data Processing	S
Data Processing with register specified shift	I + S
Data Processing with PC written	N + 2S
Data Processing with register specified shift and PC written	I + N + 2S
LDR	N + I + S
LDR into PC	N + I + N + 2S
STR	N + N

Draw the pipeline diagrams of this ARM program. Please clearly indicate the status of each clock cycle and the number of cycles needed for the whole process. (30 marks)

END OF FINAL EXAM