EE332 Lab2: Simulation of Full Adder on Nexys 4 DDR

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I. Abstract

***Abstract*—This report focuses on the phenomenons encountered in the simulation of a simple full adder, to reveal some critical features of FPGA programming comparing to ordinary programmable devices. Among these phenomenons, jitters and the race-hazard conditions are of the most concerns.**

II. Introduction

Half adder and full adder are basic elements in digital circuits used to perform addition operations on binary numbers.

A half adder

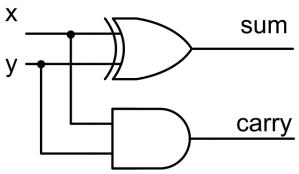

Fig. 1: Gate Level Description of Half Adder

is a combinational logic circuit that takes two binary inputs and produces two binary outputs: sum and carry.

$$\mathrm{HA} : (x_1, x_2) \mapsto (Q, C) := \begin{cases} Q & = \mathrm{xor}(x_1, x_2) \\ C & = \mathrm{and}(x_1, x_2) \end{cases} \tag{1}$$

The main limitation of the half adder is that it cannot handle carry inputs and therefore can only be used for 1-bit addition.

A full adder

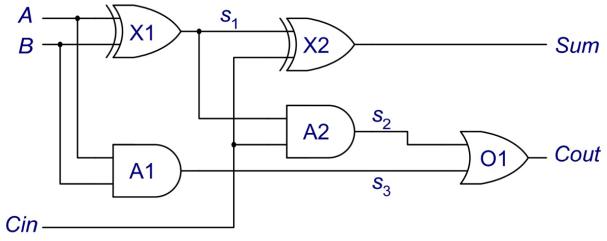

Fig. 2: Gate Level Description of Full Adder

is an extension of the half adder that accepts three binary inputs: two additions and a rounding input, and produces two binary outputs: sum and carry. Full adders can be connected in series to achieve binary addition of any number of bits.

Implementation of full adder can be derived directly from 3-digit addition, where the final carry output is toggled if any of $X_1 + X_2$ or $C_i + Q_1$ produces a carry:

$$(q_1, c_1) = \mathrm{HA}(x_1, x_2) \tag{2}$$
$$(q_2, c_2) = \mathrm{HA}(q_1, c_i) \tag{3}$$
$$c_o = \mathrm{or}(c_1, c_2) \tag{4}$$

Therefore the gate-level circuit of the full adder can be easily captured, as shown of Figure. (II)