Experiment #3

Open-Loop DC-DC Converter

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The objectives of this experiment are:

- To design and construct the converter magnetics
- To construct, test, and demonstrate your open-loop dc-dc converter
- To develop a systematic approach to debugging
- To learn good practices of circuit layout and grounding

1. Inductor Construction

Your laboratory kit contains several EFD 15/8/5 ferrite cores with bobbins and clips. Datasheets describing the important parameters of this core shape and core material are linked to the course website. Copper magnet wire of three sizes is included in the parts kit.

Design inductors L_1 and L_2 for your SEPIC. Select the wire gauge, wind the required number of turns on the bobbin, insert the proper air gaps, and assemble the core.

You can use standard notebook paper for the air gap: this paper is normally 0.003 inches thick. Cut the paper into pieces having the same shape as the face of the core leg, and insert as many pieces of paper as is needed to obtain the correct total air gap length. It is necessary to insert the same gap length in each of the three core legs.

Check the inductance value L of your inductor using the Digilent AD2 with its *Impedance Analyzer* function. A guide for measuring impedance plots is available online at: `https://reference.digilentinc.com/reference/instrumentation/guides/waveforms-impedance-analyzer`

If necessary, adjust your design to obtain a measured inductance that is adequate for your converter design.

Do the above for both inductors of your SEPIC. In your Exp. 3 lab report, document your design for each inductor (turns, wire gauge used, how you gapped the core). Report the measured inductances you obtained.

2. Power Stage Construction

Figure 1 contains a high-level schematic of the open-loop SEPIC and related circuit for Experiment 3. You should construct your SEPIC design on your perfboard. For each component, refer to its data sheet to find its pin assignments. Before constructing your circuit, it is highly recommended

that you watch the lecture on layout and grounding, and then attempt to construct your prototype circuit accordingly.

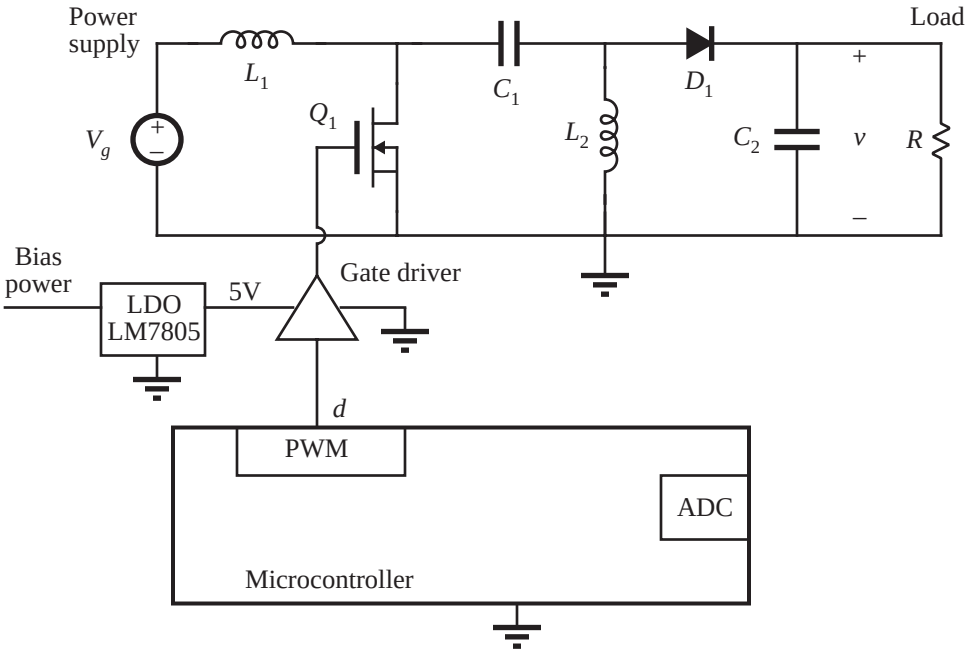

Figure 1 SEPIC circuit schematic.

Include an LM7805 series-pass voltage regulator on your perfboard, to supply 5V to power your gate driver IC and other future circuitry. The input to this IC (labeled "Bias power" in Fig. 1 may be connected either to the converter input or to its output; you may find it helpful to install a switch to switch between these sources for the controller power. Note that the LM7805 requires a minimum input voltage before it can produce an output of 5 V. As noted on the LM7805 data sheet, this IC requires ceramic capacitors connected between the power input and ground pins, and between the power output and ground pins, close to the IC. Use ceramic capacitors of at least 0.1μF from your parts kit.

Glue an 8 pin IC socket to your perfboard for the gate driver IC, and connect it to the microcontroller PWM output, the 5 V power/ground, and the MOSFET gate/source. Bypass its power supply with a ceramic capacitor of at least 0.1μF, connected to the power and ground pins in close proximity to the IC. It is suggested that you then turn on your microcontroller, LDO, and gate driver IC; with the microcontroller producing a PWM output that is applied to the gate driver IC, check whether the gate driver produces an output. Further, use your AD2 oscilloscope to examine each of the 8 pins of the gate driver IC relative to the circuit ground, and check whether the waveforms look correct. When you are satisfied that the gate driver, LDO, and PWM are operating correctly, turn off the power supply and microcontroller, and construct the remainder of the power stage.

Construct your SEPIC converter circuit on your perfboard, between the power input terminals and the power output terminals. Your power stage design should operate all components within their datasheet ratings. Of particular importance are the rated voltage and average current of the

MOSFET and Schottky diode, and the maximum voltages and rms currents of the capacitors. Typical design margins are 70% on semiconductor voltages (i.e., the actual worst-case peak voltage is no greater than 70% of the datasheet rating), and 50% on semiconductor average currents. The capacitor maximum voltages should not exceed the rated working voltages, and the capacitor rms currents should not exceed the datasheet rated rms current.

Connect a 30Ω power resistor to the converter output terminals. *Caution*: the output voltage of the ideal SEPIC tends to infinity if the load is disconnected. This happens because the converter then operates in deep discontinuous conduction mode with $K \rightarrow 0$. If your load resistor is not securely connected to the converter output, the output voltage will tend to a large value that may cause components to fail.

Connect multimeters to measure the converter input and output voltages. Turn on your microcontroller and verify again that it produces a PWM output with the proper switching frequency and a duty cycle somewhat less than 50%.

Adjust the current limit setting on your dc power supply to a value that is large enough to supply the expected converter input current. Connect the power supply to the SEPIC input, and increase the power supply voltage to 7-10 volts. You should observe dc input and output voltages having ratio similar to that expected for the SEPIC and your chosen duty cycle. Your power supply should not current limit. Use your AD2 oscilloscope to view the voltages with respect to ground at each node in your converter power stage, and verify that the waveforms appear correct. When the waveforms appear to be correct, proceed to the tests below.

3. Power Stage Testing

The objective of this part is to demonstrate that your SEPIC can operate with the following full power conditions:

- Input voltage = 17 V
- Output voltage = 12.25 V
- Load resistance = 15Ω

This operating point approximates use of the PV panel at its maximum power point of 17 V and 10 W, with the battery in a somewhat discharged state of 12.25 V. The testing of this part should be done with your dc power supply and power resistor loads.

Adjust your duty cycle so that the converter produces the correct output voltage with the above conditions. With the AD2 oscilloscope monitoring the MOSFET drain voltage, slowly increase your power supply voltage until it reaches 17 V. It may be necessary to adjust the power supply current limit setting. Capture the following waveforms, and record for your report: MOSFET drain-to-source voltage, diode anode voltage, and output capacitor voltage.

With the converter operating at the above operating point, use your multimeters to measure the dc input voltage, dc input current, dc output voltage, and dc output current. *Note*: the multimeters are more accurate than the power supply readings, and multitmeters should be used for all four measurements. Compute the efficiency of your converter.

With the duty cycle and input voltage unchanged, increase your load resistance to 60Ω, i.e., put the load resistors in series instead of parallel. Measure the output voltage using a multimeter. Did it change? Why? Adjust the duty cycle as necessary to return the output voltage to 12.25 V, and record the value of this duty cycle.

4. Current Waveform Measurement

The object in this part is to build a current sensing circuit to observe the MOSFET drain current $i_D(t)$. A suitable circuit is illustrated in Fig. 2. Your parts kit includes a ferrite toroid, signal diodes, and zener diodes that can be used for this purpose. When this circuit operates correctly, the output voltage is proportional to the drain current according to $v(t) = i_D(t)\,R/n$.

The textbook problem 6.8 outlines how to choose the secondary turns n, zener voltage V_z, and resistance R so that the transformer magnetizing current resets to zero before the end of the switching period, with specified maximum i_D and duty cycle. Choose n and R, using the 18 V zener diode in your kit. Construct the current sense circuit on your breadboard, to monitor the MOSFET drain current.

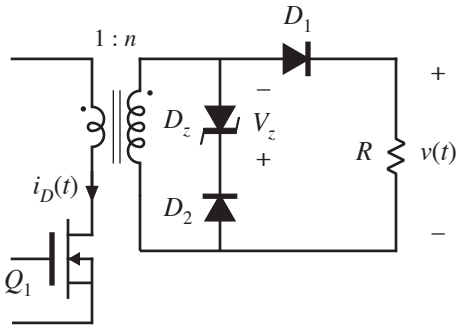

Figure 2 Transistor current sense circuit.

In the SEPIC, when the MOSFET conducts then its drain current is equal to the sum of the two inductor currents: $i_D = i_{L1} + i_{L2}$. Operate your converter at the full power point defined above. Use the first channel of your AD2 oscilloscope to record $v(t)$, and document the scale factor for converting the measured $v(t)$ into a calibrated drain current value. During the interval when the MOSFET conducts, what is the average drain current? Compare this to the sum of the dc input and output currents. Also record the peak drain current, and compare with the sum of inductor current ripples you expect based on your inductor values.

During the diode conduction interval, the sum of inductor currents flows through the diode. With the converter operating at the above full power operating point, use the second channel of your AD2 oscilloscope to measure the switching ripple on the output capacitor. You will need to set your oscilloscope to ac coupling, and adjust the volts/division setting so that the ripple can be clearly seen.

A practical capacitor model includes an *equivalent series resistance* (ESR) in series with an ideal capacitor. In many capacitors, including the aluminum electrolytic capacitors in your parts kit,

the ESR induces the major portion of the ac voltage ripple. Based on your measured capacitor voltage and MOSFET current waveforms, estimate the value of the ESR: $ESR \approx \Delta v/\Delta i$ during the switching transition. Also estimate the power loss induced in the ESR, $P_C = I_{rms}^2 ESR$. This power loss limits the maximum ac current that can be handled by the capacitor. Include in your report: (*i*) your estimate of the ESR, (*ii*) your estimate of the power loss P_C, and (*iii*) the datasheet rms current rating for this capacitor.

5. Open Loop Behavior in PV System

This part requires operation outside in the sun, with a battery that is not fully charged. Connect the PV panel to your converter input, and the battery to the converter output. Your laptop computer will need to continue to power its USB connection to the Launchpad, and you will need to be able to adjust the programmed duty cycle. Connect multimeters to measure the PV voltage, PV current, and battery current.

Adjust the duty cycle in steps of 0.1, from 0 to 1. At each step, record all meter readings and the duty cycle. If a duty cycle step overstresses one or more components, you may omit that measurement.

In your report, you should plot your Part 5 measured data of (i) PV voltage vs. D, (ii) battery current vs. D, (iii) PV power vs. D, and (iv) V_{batt}/V_{pv} vs. D. Explain theoretically the salient features of your plots.

Perform a dc simulation of this part, using LTspice or Simulink. Use your model developed in Experiment 1 for the PV panel, and use the Spice averaged switch model CCM-DCM1 (or your own Simulink equivalent) in place of the MOSFET and diode. Use a Thevenin equivalent for the battery. Sweep the duty cycle, and generate simulated versions of plots (i) - (iv) above.

How do your measured and simulated plots compare with the theoretical model of the SEPIC? If you choose the optimum duty cycle, how much power can you obtain? How does this compare with the direct energy transfer approach used to charge the battery in Experiment 1?

Grading Rubric

Inductor L_1

(10 points total)

- Theoretical inductance L_1 value
- Computed current ripple Δi_{L1}, based on theoretical inductance and at $V_{pv} = 17\text{V}, V_{batt} = 12.5\text{V}, P_{pv} = 10\text{W}$
- Computed dc winding resistance at a winding temperature of 100°C
- Predicted copper loss of inductor based on its dc resistance and at the above operating point
- Computed saturation current at a core temperature of 100°C
- Wire gauge (AWG)

- Turns
- Air gap: computed total air gap length, and the number of sheets of paper that you actually used.
- Measured impedance plot for inductor L_1 and its inductance value

Inductor L_2

(10 points total)

- Theoretical inductance L_2 value
- Computed current ripple Δi_{L2}, based on theoretical inductance and at $V_{pv} = 17\text{V}, V_{batt} = 12.5\text{V}, P_{pv} = 10\text{W}$
- Computed dc winding resistance at a winding temperature of 100°C
- Predicted copper loss of inductor based on its dc resistance and at the above operating point
- Computed saturation current at a core temperature of 100°C
- Wire gauge (AWG)
- Turns
- Air gap: computed total air gap length, and the number of sheets of paper that you actually used.
- Measured impedance plot for inductor L_2 and its inductance value

Component stress analysis

(10 points total)

Analyze your design to estimate the worst case component stresses applied to the semiconductor switches and electrolytic capacitors in your converter. In particular, compute the entries in the two tables below, and include in your report. Do these elements operate within their ratings in your converter? How large are the design margins?

Table 1 Summary of Semiconductor Stress Analysis

Component	Rated V_{max}	Actual max V	$\frac{V}{V_{max}}$	Rated I_{av}	Actual avg I	$\frac{I}{I_{av}}$
MOSFET						
Diode						

Table 2 Summary of Capacitor Stress Analysis

Component	Rated V_{max}	Actual max V	$\frac{V}{V_{max}}$	Rated I_{rms}	Actual rms I	$\frac{I}{I_{av}}$
C_1						
C_2						

Power Stage Testing

(15 points total)

- For your power stage testing with the input voltage at 17 V and the output voltage at approximately 12.25 V and load resistance of 15Ω, document the following experimental waveforms: MOSFET drain-to-source voltage, diode anode voltage, and output capacitor voltage. (5 points)
- For your power stage testing with the input voltage at 17 V and the output voltage at approximately 12.25 V and load resistance of 15Ω, document your multimeter measurements of input voltage, input current, output voltage, output current, and converter efficiency. (5 points)
- For your power stage testing with the input voltage at 17 V, load resistance increased to 60Ω, and duty cycle unchanged, document your multimeter measurements of input voltage, input current, output voltage, and output current. Adjust the duty cycle such at the output voltage is 12.25 V, document your multimeter measurements, and compute the converter efficiency at this operating point. Briefly discuss the reason for the change in efficiency. (5 points)

Current Waveform Measurement

(20 points total)

- Document your current sense circuit design calculations (Fig. 2) to select values for the resistance R and secondary turns n. (5 points)
- Document your measurements of the MOSFET drain current using your current sense circuit: include your oscilloscope waveform of the voltage $v(t)$ in Fig. 2 at the full power point defined earlier. Specify the scale factor from measured voltage $v(t)$ to the actual drain current, and use this scale factor to compute the actual peak drain current. Compare this maximum current to the predicted sum of peak inductor currents at this operating point. Also find the average drain current, according to the sensed waveform $v(t)$, and compare to the sum of the converter dc input and output currents. (5 points)
- Document your measured MOSFET drain current and output capacitor voltage waveforms. The capacitor voltage waveform should be shown with ac coupling at a vertical (voltage scale) appropriate to determine the peak-to-peak capacitor voltage ripple. Estimate the capacitor ESR using $ESR \approx \Delta v/\Delta i$ during the switching transition. Also estimate the power loss induced in the ESR, $P_C = I_{rms}^2 ESR$. Give the datasheet rated rms capacitor current, and

estimate the power loss that would be consumed in the ESR by this rated rms current. (10 points)

Open-Loop Behavior in PV System

(35 points total)

- Plot your Part 5 measured data of (i) PV voltage vs. D, (ii) battery current vs. D, (iii) PV power vs. D, and (iv) V_{batt}/V_{pv} vs. D. Explain theoretically the salient features of your plots. (15 points)
- Perform a dc simulation of this part, using LTspice or Simulink. Use your model developed in Experiment 1 for the PV panel, and use the Spice averaged switch model CCM-DCM1 (or your own Simulink equivalent) in place of the MOSFET and diode. Use a Thevenin equivalent for the battery. Sweep the duty cycle, and generate simulated versions of plots (i) - (iv) above. (15 points)
- How do your measured and simulated plots compare with the theoretical model of the SEPIC? If you choose the optimum duty cycle, how much power can you obtain? How does this compare with the direct energy transfer approach used to charge the battery in Experiment 1? (5 points)