University of Colorado
Boulder

Photovoltaic Power Electronics
ECEA 5716 Open-Loop Photovoltaic Power Electronics Laboratory
Open-Loop DC-DC Converter

Kai I. Tam

October 03, 2021

Circuit Analysis

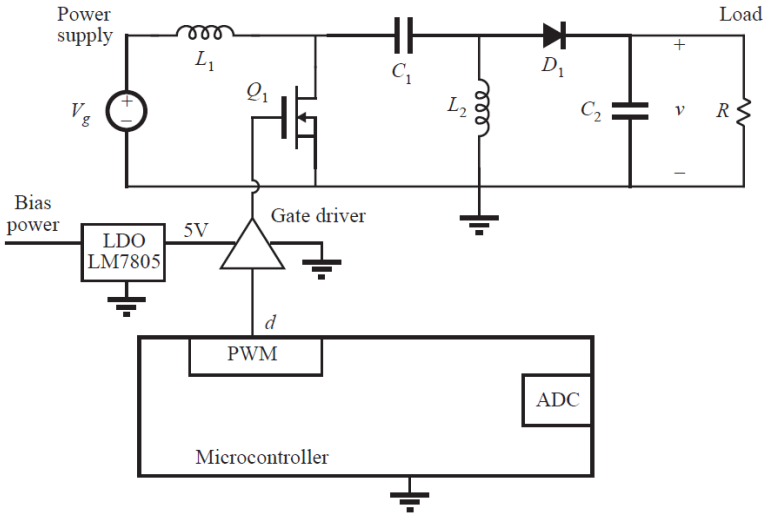


Figure 1 SEPIC circuit schematic.

Using Volt-Second and Charge Balance, deriving the following:

D	D'
$V_{L1}(t) = V_g$	$V_{L1}(t) = V_g - V_{c1} - V$
$V_{L2}(t) = V_{C1}$	$V_{L2}(t) = -V$
$I_{C1}(t) = -I_{L2}$	$I_{C1}(t) = I_{L1}$
$I_{C2}(t) = -\frac{V}{R}$	$I_{C2}(t) = I_{L1} + I_{L2} - \frac{V}{R}$

Volt-Second Balance	Charge Balance
$< V_{L1} >_{Ts} = D(V_g) + D'(V_g - V_{C1} - V) = 0$	$< I_{C1} >_{Ts} = D(-I_{L2}) + D'(I_{L1}) = 0$
$< V_{L2} >_{Ts} = D(V_{C1}) + D'(-V) = 0$	$< I_{C2} >_{Ts} = D\left(-\frac{V}{R}\right) + D'\left(I_{L1} + I_{L2} - \frac{V}{R}\right) = 0$

Four Key Equations
$V_{C1} = V_g$
$V = \frac{D}{1-D} V_g$
$I_{L1} = \frac{D}{D'}\frac{V}{R} = (\frac{D}{1-D})^2 \frac{V_g}{R}$
$I_{L2} = \frac{V}{R} = (\frac{D}{1-D})\frac{V_g}{R}$

Given Parameters:

$$V_{in} = V_g = V_{pv} = 17V$$
$$V_{out} = V = V_{batt} = 12.5V$$
$$P_{in} = P_{pv} = 10W$$

- Assuming 100% efficiency, Output Load **R** can be considered as :

$$P_{in} = P_{out} = \frac{{V_{out}}^2}{R}$$
$$R = \frac{{V_{out}}^2}{P_{out}} = \frac{12.5^2}{10} = 15.625\Omega \approx 15\Omega$$

- Duty cycle **D** can be approximate:

$$D = \frac{V_{out}}{V_{in} + V_{out}} = \frac{12.5}{17 + 12.5} = 0.4237$$

- Inductor **L_1** Current

$$I_{L1} = (\frac{D}{1-D})^2 \frac{V_g}{R} = (\frac{0.423729}{1-0.423729})^2 \frac{17}{15.625} = 0.5882A$$

- Inductor **L_2** Current

$$I_{L2} = (\frac{D}{1-D}) \frac{V_g}{R} = (\frac{0.423729}{1-0.423729}) \frac{17}{15.625} = 0.8000A$$

Desired Parameters:

- Switching Frequency = 500kHz
- Switching Period = 1/500kHz = 2µS
- Maximum allowable Peak to Peak Current Ripple ≈ 6% (by choice)
- Maximum allowable Peak to Peak Voltage Ripple ≈ 50mV (by choice)

Theoretical Inductor Value			
$L_1 \frac{dI_{L1}(t)}{dt} = V_{L1}(t)$	$\Delta I_{L1} = \frac{0.06 \times I_{L1}}{2} = 17.65mA$	$\Delta I_{L1} = \frac{V_g D T_s}{2L_1}$	$L_1 = \frac{V_g D T_s}{2\Delta I_{L1}} = 408.19\mu H$
$L_2 \frac{dI_{L2}(t)}{dt} = V_{L2}(t)$	$\Delta I_{L2} = \frac{0.06 \times I_{L2}}{2} = 24.00mA$	$\Delta I_{L2} = \frac{V_g D T_s}{2L_2}$	$L_2 = \frac{V_g D T_s}{2\Delta I_{L2}} = 300.14\mu H$

Theoretical Capacitor Value			
$C_1 \frac{dV_{C1}(t)}{dt} = I_{C1}(t)$	$\Delta V_{C1} = 0.025V$	$\Delta V_{C1} = \frac{I_{L2} D T_s}{2C_1} = \frac{D^2}{D'} \frac{V_g T_s}{2RC_1}$	$C_1 = \frac{D^2}{D'} \frac{V_g T_s}{2R\Delta V_{C1}} = 13.559\mu F$
$C_2 \frac{dV_{C2}(t)}{dt} = I_{C2}(t)$	$\Delta V_{C2} = 0.025V$	$\Delta V_{C2} = \frac{V D T_s}{2RC_2} = \frac{D^2}{D'} \frac{V_g T_s}{2RC_2}$	$C_2 = \frac{D^2}{D'} \frac{V_g T_s}{2R\Delta V_{C2}} = 13.559\mu F$

For the simplicity of the circuit design, I chose **L1 = L2 = 470µH**, **C1 = C2 = 100µF**, which are also common commercial value.

Inductor L_1, L_2

- Theoretical inductance L_1 value

  $L_1 = L_2 =$ 470µH (by choice)

- Computed current ripple $\Delta i_{L1}/\Delta i_{L2}$, based on theoretical inductance and at
  - V_{pv} = 17V
  - V_{batt} = 12.5V
  - P_{pv} = 10W

$$\Delta I_{L1}/\Delta I_{L2} = \frac{V_g D T_s}{2L} = \frac{17 \times 0.4237 \times 2\mu S}{2 \times 470\mu H} = 15.3253mA$$

- Wire gauge (AWG)

  26 AWG (by choice)

- Turns

For N87 material [1] [2]:

$$K1\ (25℃) = 29.7$$
$$K2\ (25℃) = -0.676$$

$$s = \ell_g = \frac{A_L^{\frac{1}{K2}}}{K1} = \frac{A_L^{\frac{1}{-0.676}}}{29.7}$$

Assuming one sheet of paper is used

$$\ell_g = 0.004" = 0.1016mm$$

$$A_L(nH) = 29.7 \times \left(\ell_g\right)^{-0.676} = 29.7 \times (0.1016)^{-0.676} = 139.347nH$$

We can then utilize A_L and desired Inductance to find out turns ratio n.

$$A_L = \frac{L}{n^2}$$

$$n = \sqrt{\frac{470uH}{139.347nH}} \approx 58.0765 \approx 58$$

- Measured impedance plot for inductor L_1 and its inductance value.

EFD 15/8/5 Datasheet Parameters[1]

Effective magnetic path length	l_e = 34 mm
Effective magnetic cross section	A_e = 15 mm^2
Minimum core cross section	A_{min} = 12.2 mm^2
Effective magnetic volume	V_e = 510 mm^3
Inductance factor;	$A_L = L/N^2$ = 780 +30%/-20%
Relative effective permeability	μ_e = 1400
Winding cross section	A_N = 18.1 mm^2
Average length of turn	l_N = 35.1 mm
Resistance factor;	$A_R = R_{Cu}/N^2$ = 66.7μΩ

Note: With turns n = 58 that calculated previously, I round it up to 60 and used 1 paper thickness on all three legs. I only get around 355uH with the measurement of Digilent AD2. I ended up round to 64-66 turns to achieve ≥ 470uH. Below are the configurations that I have tried:

INDUCTOR L1							
TURNS	PAPER	GAP (mm)	Core	WIRE (AWG)	WIRE RESISTANCE mΩ	INDUCTANCE (uH)	
						METER	PLOT @ 500kHz
60	1	0.1016	Ferrite	26	198.2	368.1	354.597
75	1	0.1016	Ferrite	26	256.6	541.5	525.848
75	1	0.1016	Ferrite	26	258.2	536	550.358
75	2	0.2032	Ferrite	26	254.2	349.1	343.456
70	1	0.1016	Ferrite	26	234.5	431.9	441.496
72	1	0.1016	Ferrite	26	244.3	574.6	578.687
65	1	0.1016	Ferrite	26	230.5	487.2	493.699
64	1	0.1016	Ferrite	26	232.5	472.1	485.423
64	1	0.1016	Ferrite	26	232.7	480.3	497.518
64	1	0.1016	Ferrite	26	228.8	484.7	483.194

INDUCTOR L2							
TURNS	PAPER	GAP (mm)	Core	WIRE (AWG)	WIRE RESISTANCE mΩ	INDUCTANCE (uH)	
						METER	PLOT @ 500kHz
70	1	0.1016	Ferrite	26	254.4	529.8	555.451
68	1	0.1016	Ferrite	26	246.4	504.5	521.392
65	1	0.1016	Ferrite	26	234	461.7	465.687
66	1	0.1016	Ferrite	26	236.4	473.8	475.237
66	1	0.1016	Ferrite	26	234.4	473.5	485.741
66	1	0.1016	Ferrite	26	218.5	481.9	491.47
66	1	0.1016	Ferrite	26	218.2	481.5	489.879

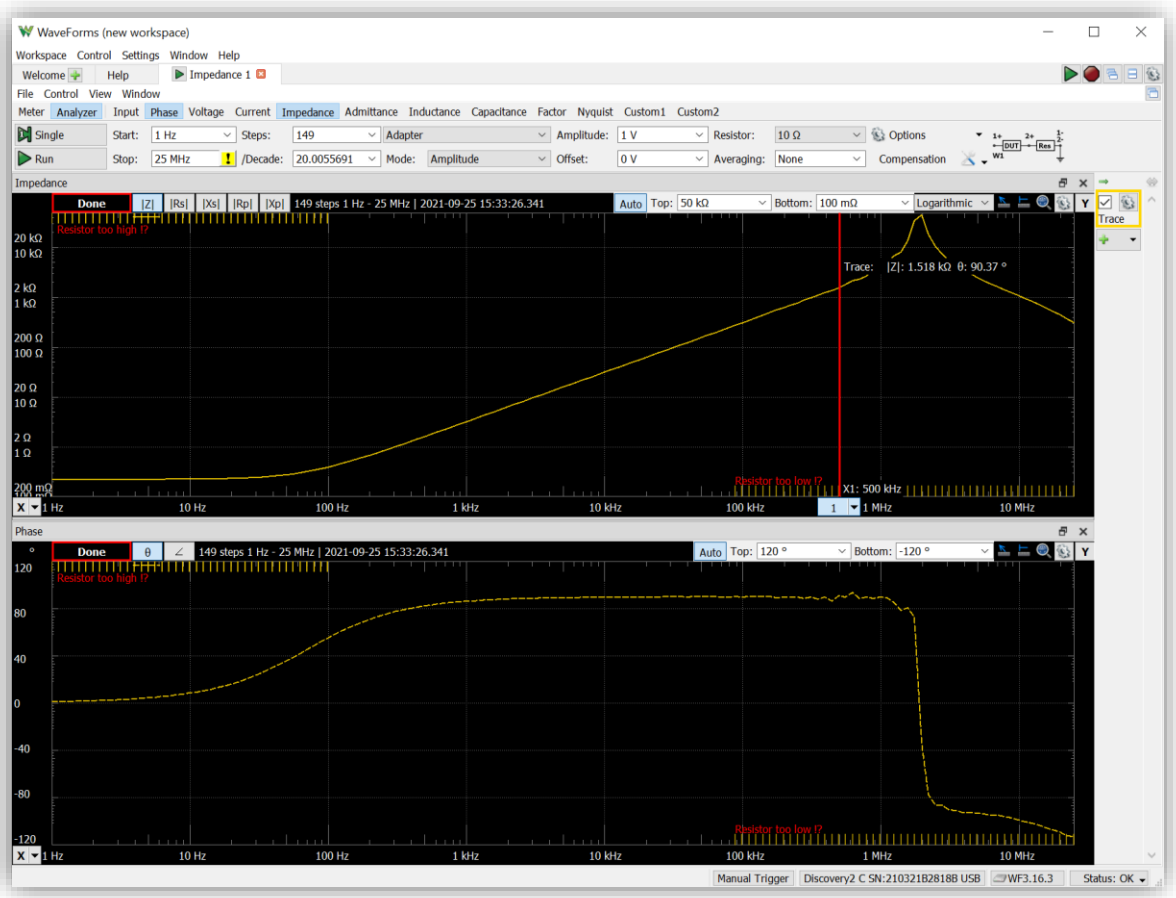


Figure 3. Inductor L_1 plot

At 500KHz, Inductance is:

$$L_1 = \frac{|Z|}{2\pi f_z} = \frac{1.518k\Omega}{2\pi \times 500kHz} = 483.194\mu H$$

Assuming the formula provide by TDK holds true, we can reverse calculation to get actual air gap used:

$$A_L = \frac{L}{n^2} = \frac{483.194uH}{64^2} = 117.967nH$$

$$s = \ell_g = \frac{A_L^{\frac{1}{K2}}}{K1} = (\frac{117.967}{29.7})^{\frac{1}{-0.676}} = 0.129987mm$$

- Computed dc winding resistance at a winding temperature of 25ºC

$$\rho@100°C = 1.724 \times 10^{-6}$$
$$A_w(26\,AWG) = 0.00128cm^2$$

$$R_{DC} = \frac{\rho \times n \times MLT}{A_w} = \frac{(1.724 \times 10^{-6})\Omega cm \times (64 \times 3.51cm)}{(0.00128cm^2)} = 302.562m\Omega$$

- Computed dc winding resistance at a winding temperature of 100ºC

$$\rho@100°C = 2.3 \times 10^{-6}$$
$$A_w(26\,AWG) = 0.00128cm^2$$

$$R_{DC} = \frac{\rho \times n \times MLT}{A_w} = \frac{(2.3 \times 10^{-6})\Omega cm \times (64 \times 3.51cm)}{(0.00128cm^2)} = 403.65m\Omega$$

- Predicted copper loss of inductor based on its dc resistance and at the above operating point

$$P = {I_{DCrms}}^2 \times R_{DC} = 0.5882^2 \times 0.40365 = 139.7mW$$

- Computed saturation current at a core temperature of 100ºC

Effective magnetic path length	l_e = 34 mm
Relative effective permeability	μ_e = 1400
Effective magnetic cross section	A_e = 15 mm^2
Flux Density (100ºC)	B_s = 390 mT

$$R_{total} = \frac{\ell_m}{\mu_0 \times \mu_e \times (A_e)} + \frac{3 \times \ell_g}{\mu_0 \times (A_e)}$$

$$R_{total} = \frac{0.034}{4\pi \times 10^{-7} \times 1400 \times 15 \times 10^{-6}} + \frac{3(0.000129987)}{4\pi \times 10^{-7} \times 15 \times 10^{-6}}$$

$$R_{total} = 21.9765 \times 10^6$$

$$I_{sat} = \frac{B_{sat}A_e}{n} \times R_{total} = \frac{0.39 \times 15 \times 10^{-6}}{64} \times 21.9765 \times 10^6 = 2.00879A$$

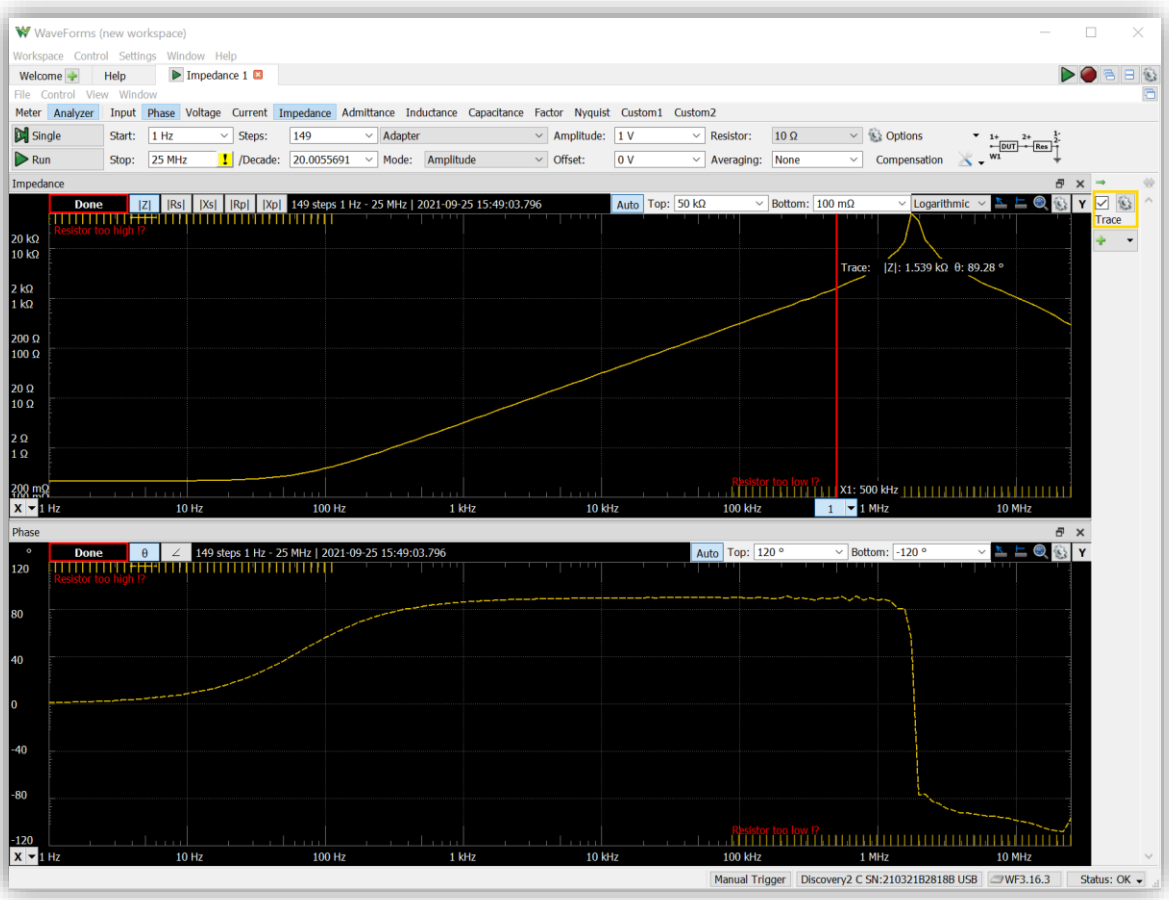


Figure 4. Inductor L_2 plot

At 500KHz, Inductance is:

$$L_2 = \frac{|Z|}{2\pi f_z} = \frac{1.539k\Omega}{2\pi \times 500kHz} = 489.879\mu H$$

Assuming the formula provide by TDK holds true, we can reverse calculation to get actual air gap used:

$$A_L = \frac{L}{n^2} = \frac{489.879uH}{66^2} = 112.461nH$$

$$s = \ell_g = \frac{A_L^{\frac{1}{K2}}}{K1} = (\frac{112.461}{29.7})^{\frac{1}{-0.676}} = 0.139511mm$$

- Computed dc winding resistance at a winding temperature of 25ºC

$$\rho@100°C = 1.724 \times 10^{-6}$$
$$A_w(26\,AWG) = 0.00128cm^2$$

$$R_{DC} = \frac{\rho \times n \times MLT}{A_w} = \frac{(1.724 \times 10^{-6})\Omega cm \times (66 \times 3.51cm)}{(0.00128cm^2)} = 312.017m\Omega$$

- Computed dc winding resistance at a winding temperature of 100ºC

$$\rho@100°C = 2.3 \times 10^{-6}$$
$$A_w(26\,AWG) = 0.00128cm^2$$

$$R_{DC} = \frac{\rho \times n \times MLT}{A_w} = \frac{(2.3 \times 10^{-6})\Omega cm \times (66 \times 3.51cm)}{(0.00128cm^2)} = 416.264m\Omega$$

- Predicted copper loss of inductor based on its dc resistance and at the above operating point

$$P = {I_{DCrms}}^2 \times R_{DC} = 0.8^2 \times 0.416264 = 266.4mW$$

- Computed saturation current at a core temperature of 100ºC

Effective magnetic path length	l_e = 34 mm
Relative effective permeability	μ_e = 1400
Effective magnetic cross section	A_e = 15 mm^2
Flux Density (100ºC)	B_s = 390 mT

$$R_{total} = \frac{\ell_m}{\mu_0 \times \mu_e \times (A_e)} + \frac{3 \times \ell_g}{\mu_0 \times (A_e)}$$

$$R_{total} = \frac{0.034}{4\pi \times 10^{-7} \times 1400 \times 15 \times 10^{-6}} + \frac{3(0.000139511)}{4\pi \times 10^{-7} \times 15 \times 10^{-6}}$$

$$R_{total} = 23.4923 \times 10^6$$

$$I_{sat} = \frac{B_{sat}A_e}{n} \times R_{total} = \frac{0.39 \times 15 \times 10^{-6}}{66} \times 23.4923 \times 10^6 = 2.08227A$$

Component stress analysis

Analyze your design to estimate the worst-case component stresses applied to the semiconductor switches and electrolytic capacitors in your converter. In particular, compute the entries in the two tables below, and include in your report. Do these elements operate within their ratings in your converter? How large are the design margins?

Table 1 Summary of Semiconductor Stress Analysis [3] [4]

Component	Rated V_{max}	Actual max V	$\frac{V}{V_{max}}$	Rated I_{av}	Actual avg I	$\frac{I}{I_{av}}$
MOSFET	60	29.5	0.492	9.6	0.588	0.061
Diode	60	29.5	0.492	3	0.800	0.267

MOSFET

Estimated Actual max V occurred at D' (Lossless)

$$\boldsymbol{V_{MOSFET\ ds(\max)} = V_g + \left(-V_{L1(D')}\right) = V_g - V_g + V_{C1} + V = V_g + V = 17 + 12.5}$$

$$\boldsymbol{V_{MOSFET\ ds(\max)} = 29.5V}$$

Estimated Actual avg I (Lossless)

$$\boldsymbol{I_{MOSFET(\text{avg})} = D(I_{L1} + I_{L2}) = D\left(\frac{D}{D'}\frac{V}{R} + \frac{V}{R}\right) = \frac{V}{R}\left(\frac{D}{D'}\right) = \frac{12.5}{15.625}\left(\frac{0.4237}{1 - 0.4237}\right)}$$

$$\boldsymbol{I_{MOSFET(\text{avg})} = 0.588A}$$

Diode

Estimated Actual max V occurred at D (Lossless)

$$\boldsymbol{V_{Diode\ (\max)} = V_{L2} + V_{C2} = V_g + V = 17 + 12.5}$$

$$\boldsymbol{V_{Diode\ (\max)} = 29.5V}$$

Estimated Actual avg I (Lossless)

$$\boldsymbol{I_{Diode\ (\text{avg})} = D'(I_{L1} + I_{L2}) = D'\left(\frac{D}{D'}\frac{V}{R} + \frac{V}{R}\right) = \frac{V}{R} = \frac{12.5}{15.625}}$$

$$\boldsymbol{I_{Diode\ (\text{avg})} = 0.800A}$$

Table 2 Summary of Capacitor Stress Analysis [5]

Component	Rated V_{max}	Actual max V	$\frac{V}{V_{max}}$	Rated I_{rms}	Actual rms I	$\frac{I}{I_{av}}$
C_1	50	17.0	0.340	0.870	0.710	0.816
C_2	50	12.5	0.250	0.870	0.678	0.779

C_1

Estimated Actual max V (Lossless)

$$\boldsymbol{V_{C1(max)} = V_g = 17V}$$

Estimated Actual rms I (Lossless)

$$\boldsymbol{I_{C1(avg)} = D(I_{L1}) + D'(I_{L2}) = 0.4237(0.5882) + 0.5763(0.8) = 0.710A}$$

C_2

Estimated Actual max V (Lossless)

$$\boldsymbol{V_{C1(max)} = V = 12.5V}$$

Estimated Actual rms I (Lossless)

$$\boldsymbol{I_{C1(avg)} = D\left(\frac{V}{R}\right) + D'\left(I_{L1} + I_{L2} - \frac{V}{R}\right) = 0.4237(0.8) + 0.5763(0.5882 + 0.8 - 0.8)}$$

$$\boldsymbol{I_{C1(avg)} = 0.678A}$$

Power Stage Testing

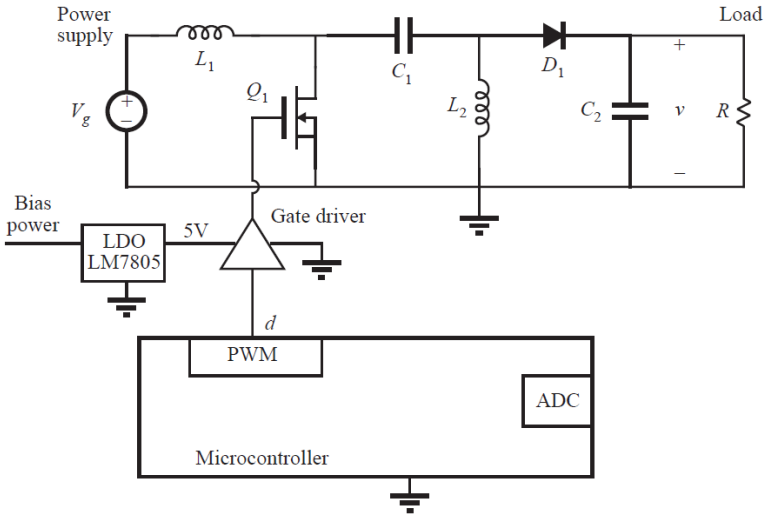


Figure 1 SEPIC circuit schematic.

Losses Element such as:

- Inductor Resistance R_{L1}, R_{L2},
- Capacitor Series Resistance ESR_{C1}, ESR_{C2},
- MOSFET ON Resistance R_{ON}
- Diode Forward Voltage Drop V_{ON}

All elements are subject to change depends on the size of R_{Load}.
By observing the waveform, the Gate Driver has around 100nS Time Rise Delay, and around 80nS Time Fall Delay.

With Bias power connect to Power supply, LDO 7805 and Texas Instrument LaunchPAD, we have around 1.785W static power drop, we will need to put this in efficiency equation.

The goal of Duty Cycle adjustment is to achieve the desired/expected output with compensated value that overcome the Losses in Real Time.

Theoretical Lossless Duty Cycle:

$$D = \frac{V_{out}}{V_{in} + V_{out}} = \frac{12.5}{17 + 12.5} = 0.4237$$

$$D = \frac{V_{out}}{V_{in} + V_{out}} = \frac{12.25}{17 + 12.25} = 0.4188$$

Compensated Duty Cycle Value to achieve expected Voltage Output:

Input (V)	Output	Load (Ω)	Duty Cycle		Output
	Desired		Lossless	Reading	Reading
17	12.5	15	0.4237	0.4453	12.507

```
PWM_setPeriod(myPwm, 119);                    // Set period for ePWM1
PWM_setCmpA(myPwm, 51);                      // Set compare A value
PWM_setCmpAHr(myPwm, (unsigned int)(184 << 8));  //Value can be varied between 1-255
```

Input (V)	Output	Load (Ω)	Duty Cycle		Output
	Desired		Lossless	Reading	Reading
17	12.25	15	0.4188	0.4395	12.254

```
PWM_setPeriod(myPwm, 119);                    // Set period for ePWM1
PWM_setCmpA(myPwm, 51);                      // Set compare A value
PWM_setCmpAHr(myPwm, (unsigned int)(103 << 8));  //Value can be varied between 1-255
```

Input (V)	Output	Load (Ω)	Duty Cycle		Output
	Desired		Lossless	Reading	Reading
17	12.25	60	0.4188	0.4194	12.250

```
PWM_setPeriod(myPwm, 119);                    // Set period for ePWM1
PWM_setCmpA(myPwm, 49);                      // Set compare A value
PWM_setCmpAHr(myPwm, (unsigned int)(56 << 8));  //Value can be varied between 1-255
```

- For your power stage testing with the input voltage at 17 V and the output voltage at approximately 12.25 V and load resistance of 15, document the following experimental waveforms: MOSFET drain-to-source voltage, diode anode voltage, and output capacitor voltage.

Figure 5. MOSFET drain-to-source voltage

Channel 1 as reference of Gate Waveform of MOSFET.

By observing the graph of Channel 2. Both have:
Voltage Ripple Top $\Delta V \approx 232.56mV$
Voltage Ripple Bottom $\Delta V \approx 232.56mV$
At D' Voltage is average at around 29.749V, which is close to 29.5V, our expected value.

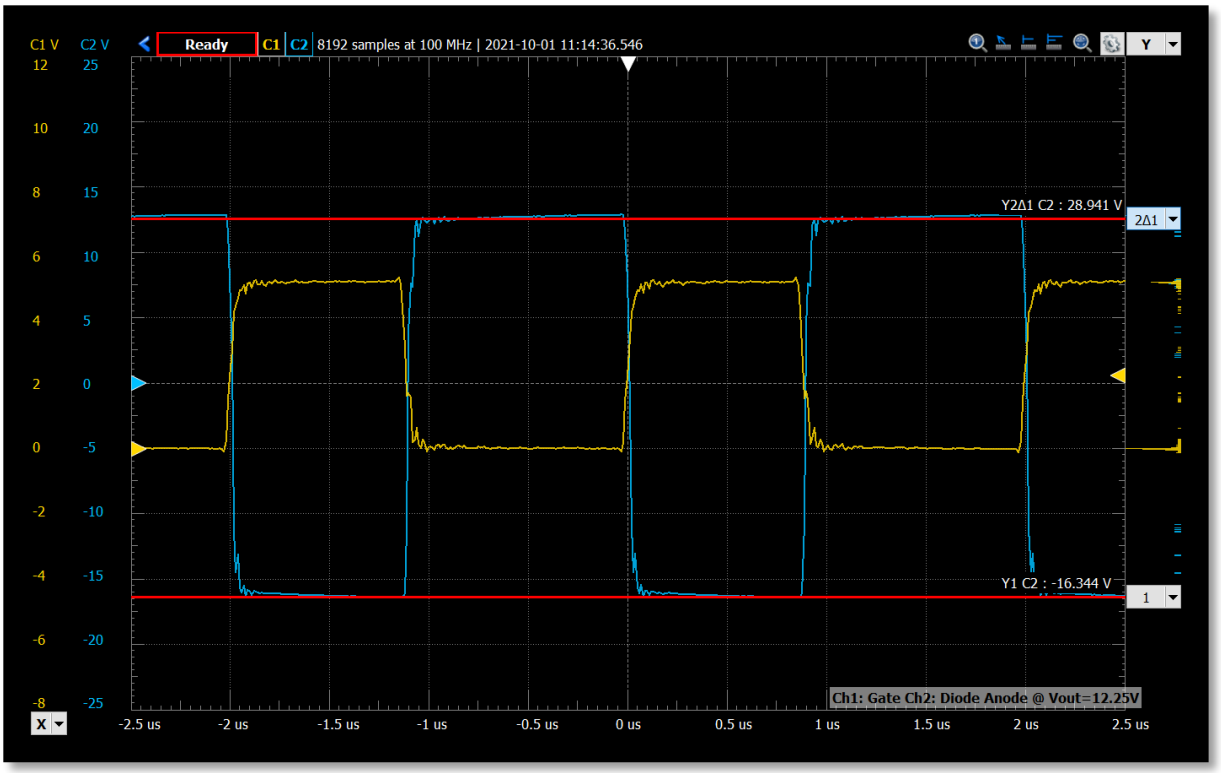


Figure 6. Diode Anode Voltage (L_2 Voltage)

Channel 1 as reference of Gate Waveform of MOSFET.

By observing the graph of Channel 2. Which is basically Voltage of Inductor L_2
At D, V_{L2} = -16.344V
At D', V_{L2} = 12.597V, which is Output Voltage V + Diode Voltage V_{fd}.
Diode Voltage V_{fd} is around 0.343V

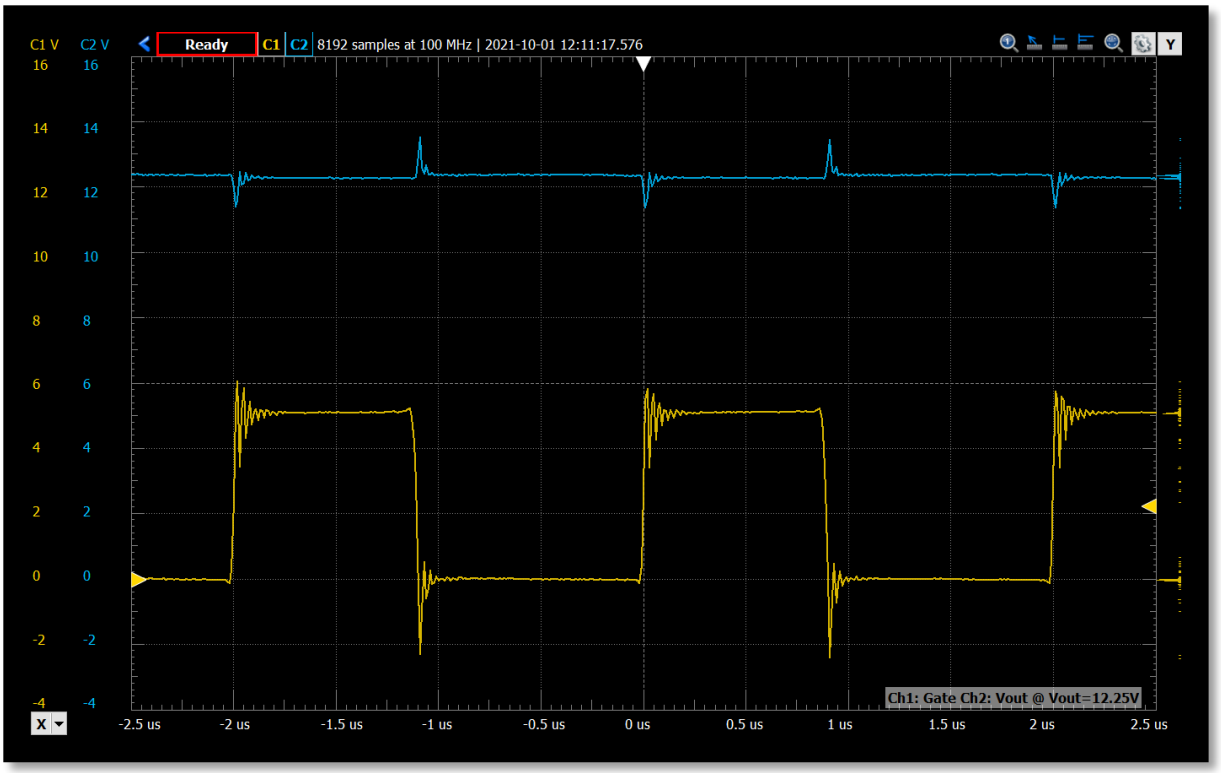


Figure 7. Output Capacitor Voltage

Channel 1 as reference of Gate Waveform of MOSFET.

We can observe switching noise on the Rising and Falling Edge of the waveform, that is due to imperfect layout and depends on where the ground of the Oscilloscope probed to.

- For your power stage testing with the input voltage at 17 V and the output voltage at approximately 12.25 V and load resistance of 15, document your multimeter measurements of input voltage, input current, output voltage, output current, and converter efficiency.

INPUT VOLTAGE (V)		INPUT CURRENT (A)	LOAD (Ω)		DUTY CYCLE	OUTPUT VOLTAGE (V)		OUTPUT CURRENT (A)	LAUCHPAD POWER (W)	EFFICIENCY (%)
DESIRED	READING		DESIRED	READING		DESIRED	READING			
17	17.001	0.7635	15	15.13	0.4395	12.25	12.251	0.8105	1.785	88.69

$$\eta(\%) = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN} + P_{LaunchPAD}} \times 100 = \frac{12.251 \times 0.8105}{17.001 \times 0.7635 - 1.785} \times 100\% = 88.69\%$$

- For your power stage testing with the input voltage at 17 V, load resistance increased to 60, and duty cycle unchanged, document your multimeter measurements of input voltage, input current, output voltage, and output current. Adjust the duty cycle such at the output voltage is 12.25 V, document your multimeter measurements, and compute the converter efficiency at this operating point. Briefly discuss the reason for the change in efficiency.

INPUT VOLTAGE (V)		INPUT CURRENT (A)	LOAD (Ω)		DUTY CYCLE	OUTPUT VOLTAGE (V)		OUTPUT CURRENT (A)	LAUCHPAD POWER (W)	EFFICIENCY (%)
DESIRED	READING		DESIRED	READING		DESIRED	READING			
17	17.001	0.2931	60	59.62	0.4395	N/A	13.266	0.2228	1.785	92.42

$$\eta(\%) = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN} + P_{LaunchPAD}} \times 100 = \frac{13.266 \times 0.2228}{17.001 \times 0.2931 - 1.785} \times 100\% = 92.42\%$$

INPUT VOLTAGE (V)		INPUT CURRENT (A)	LOAD (Ω)		DUTY CYCLE	OUTPUT VOLTAGE (V)		OUTPUT CURRENT (A)	LAUCHPAD POWER (W)	EFFICIENCY (%)
DESIRED	READING		DESIRED	READING		DESIRED	READING			
17	17.001	0.2661	60	59.62	0.4194	12.25	12.25	0.2057	1.785	91.99

$$\eta(\%) = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN} + P_{LaunchPAD}} \times 100 = \frac{12.250 \times 0.2057}{17.001 \times 0.2661 - 1.785} \times 100\% = 91.99\%$$

The losses elements are functions of R_{Load}, with R_{Load} increased, that means Output Current I_{out} reduced, which equivalent less Power Drop, that brings up the overall efficiencies.

Current Waveform Measurement

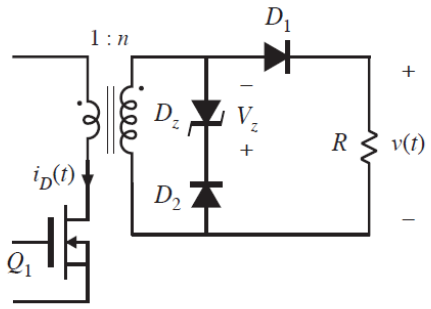


Figure 2 Transistor current sense circuit.

- Document your current sense circuit design calculations (Fig. 2) to select values for the resistance R and secondary turns n.

The turns ratio of the current sense transformer I chose is 1:50, with Rsense = 100Ω

$$v(t) = \frac{I_D(t)}{n} R_{sense}$$

Expected Ratio

$$\frac{v}{I_D} = \frac{R_{sense}}{n} = \frac{100}{50} = 2$$

Based on the previous Reading value, we can approximate the actual reading of the following:

- Approximate actual Inductor **L_1** Current

$$I_{L1} = (\frac{D}{1-D})^2 \frac{V_g}{R} = (\frac{0.4395}{1-0.43959})^2 \frac{17.001}{15.13} = 0.6909A$$

- Approximate actual Inductor **L_2** Current

$$I_{L2} = (\frac{D}{1-D}) \frac{V_g}{R} = (\frac{0.4395}{1-0.4395}) \frac{17.001}{15.13} = 0.8811A$$

- Approximate actual Inductor **L_1** Current Ripple **ΔI_{L1}**

$$\Delta I_{L1} = \frac{V_g D T_s}{2L_1} = \frac{17.001 \times 0.4395 \times 2\mu S}{2 \times 483.194\mu H} = 15.4636mA$$

- Approximate actual Inductor **L_2** Current Ripple **ΔI_{L2}**

$$\Delta I_{L2} = \frac{V_g D T_s}{2L_1} = \frac{17.001 \times 0.4395 \times 2\mu S}{2 \times 489.879\mu H} = 15.2526mA$$

Expected I_{max} which happened at D:

$$I_{D\,max} \approx I_{L1} + \Delta I_{L1} + I_{L2} + \Delta I_{L2}$$

$$I_{D\,max} \approx 0.6909 + 0.0154636 + 0.8811 + 0.0152526 = 1.60272A$$

Expected max v(t):

$$v(t) = \frac{I_D(t)}{n} R_{sense} = \frac{1.60272}{50} \times 100 \approx 3.20543V$$

- Document your measurements of the MOSFET drain current using your current sense circuit: include your oscilloscope waveform of the voltage v(t) in Fig. 2 at the full power point defined earlier. Specify the scale factor from measured voltage v(t) to the actual drain current, and use this scale factor to compute the actual peak drain current. Compare this maximum current to the predicted sum of peak inductor currents at this operating point. Also find the average drain current, according to the sensed waveform v(t), and compare to the sum of the converter dc input and output currents.

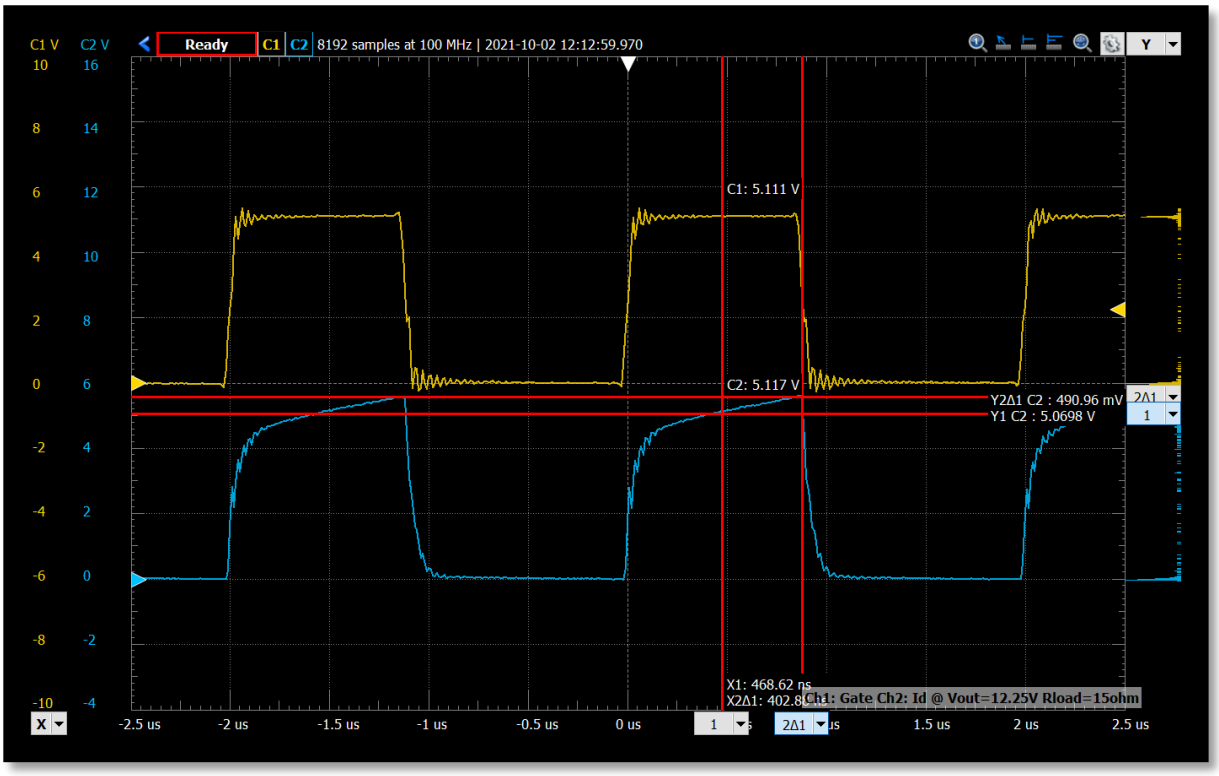


Figure 8. Output Capacitor Voltage (Zoom-in)

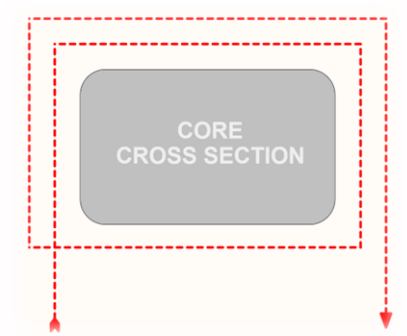
At middle of D, the Current equivalent to $I_{L1} + I_{L2}$,

The actual effective ratio is approximate:

$$n_{eff} \approx \frac{I_D R_{sense}}{v} = \frac{(I_{L1} + I_{L2})R_{sense}}{v} = \frac{(0.6909 + 0.8811)100}{5.0698} = 31$$

$$1 : n_{eff} \approx 1 : 31$$

The reasons of this variation because of the geometry of how the primary turn is rounded and solder on the Board, which by observed it is around 1.5 turn as depicted below:



The actual primary turn is approximate:

$$\frac{n_{pri}}{50} = \frac{1}{n_{eff}}$$

$$n_{pri} = \frac{50}{31} = 1.6129$$

If we want the max v(t) less than 3V, we can maintain the transformer construction and change the resistor R_{sense}

$$R_{sense} \leq \frac{n \times v}{I_{D\,max}} = \frac{31 \times 3}{1.60272} = 58.0264\Omega$$

Power Rating Requirement of new R_{sense}:

$$P_{Rsense} \geq (\frac{I_{D\,max}}{n})^2 R_{sense} = \left(\frac{1.60272}{31}\right)^2 \times 58.0264 = 0.1551W$$

Example: The average MOSFET current:

$$\frac{v(t) \times n_{eff}}{R_{sense}} \times D = \frac{5.0698 \times 31}{100} \times 0.4395 \approx 0.691A$$

- Document your measured MOSFET drain current and output capacitor voltage waveforms. The capacitor voltage waveform should be shown with ac coupling at a vertical (voltage scale) appropriate to determine the peak-to-peak capacitor voltage ripple. Estimate the capacitor ESR using ESR ≈ Δv/Δi during the switching transition. Also estimate the power loss induced in the ESR, $P_C = I^2_{rms}ESR$. Give the datasheet rated rms capacitor current, and estimate the power loss that would be consumed in the ESR by this rated rms current.

Figure 9. Output Capacitor Voltage (Zoom-in)

$$ESR \approx \frac{\Delta V_{out}}{\Delta i} \approx \frac{\Delta V_{out}}{I_{L1} + I_{L2}} \approx \frac{86.563mV}{1.572A} \approx 55.0655m\Omega$$

Power Loss of Capacitor C_2:

$$P_c = {I_{rms}}^2 \times ESR = [(I_{L1} + I_{L2})D']^2 \times ESR$$

$$P_{c2} = [(1.572)0.5605]^2 \times 55.0655m\Omega = 42.75mW$$

Note: In datasheet the rated rms current is 870mArms, which we are slightly over. Add another capacitor in parallel will share the load.

$$P_{c2} = [0.870]^2 \times 55.0655m\Omega = 41.68mW$$

Open-Loop Behavior in PV System

- Plot your Part 5 measured data of
  - PV voltage vs. D
  - Battery current vs. D
  - PV power vs. D
  - V_{batt} / V_{pv} vs. D

D	PV Voltage	PV Current	PV Power	Battery Voltage	Battery Current	V_{batt} / V_{pv}
0.10	20.5650	0.0030	0.0617	12.5390	0.0043	0.6097
0.20	20.5790	0.0040	0.0823	12.5270	0.0057	0.6087
0.30	20.5080	0.0110	0.2256	12.5480	0.0128	0.6119
0.40	18.5490	0.4350	8.0688	12.8840	0.5652	0.6946
0.45	16.3630	0.5200	8.5088	12.6710	0.6280	0.7744
0.50	12.0410	0.3180	3.8290	12.6250	0.2592	1.0485
0.60	7.8200	0.3210	2.5102	12.4700	0.1750	1.5946
0.70	4.9700	0.3130	1.5556	12.4530	0.1060	2.5056
0.80	2.8520	0.3670	1.0467	12.4880	0.0810	4.3787
0.90	1.2710	0.4500	0.5720	12.4760	0.0329	9.8159
1.00	0.1820	0.3740	0.0681	12.4620	0.0010	68.4725

Measurement at: 12:00pm 10/02/2021 New York

I added in Duty Cycle 0.45 in the readings, that is our optimum duty cycle to achieve 12.25V, 10W Power transfer, just to confirm if we can get the most out of the Panel at that duty cycle.

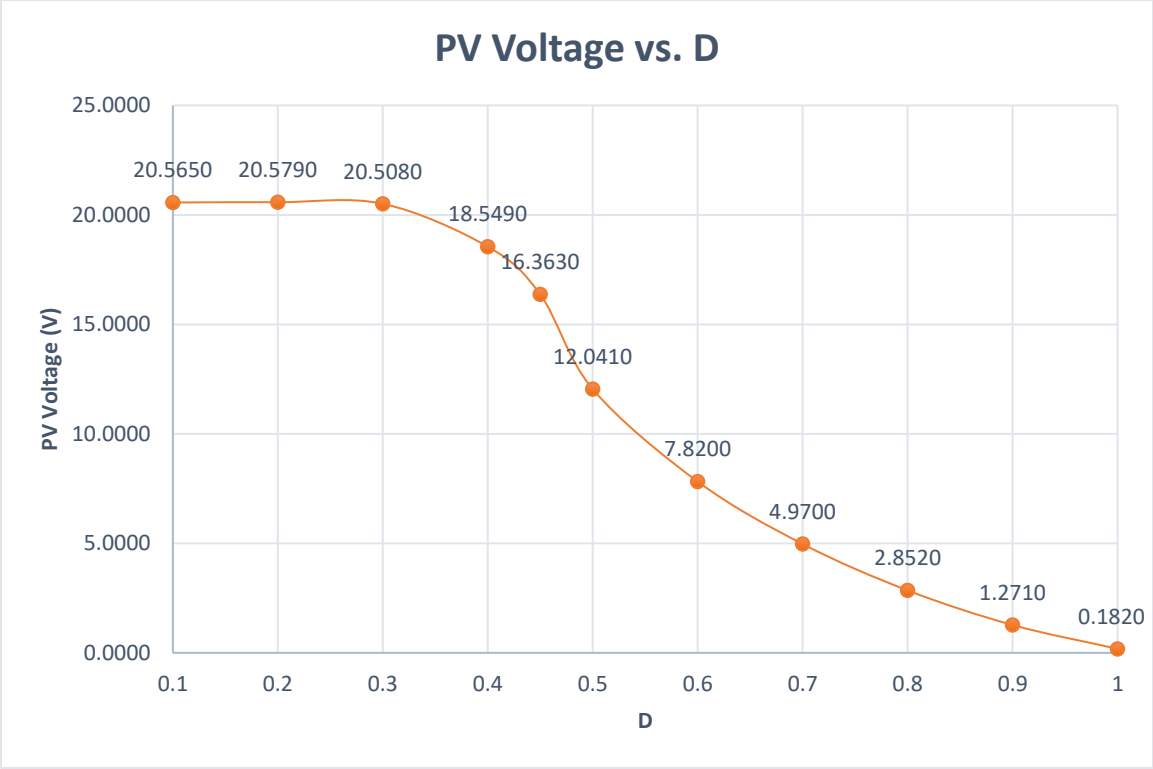


Figure 10. Panel Voltage vs. Duty Cycle

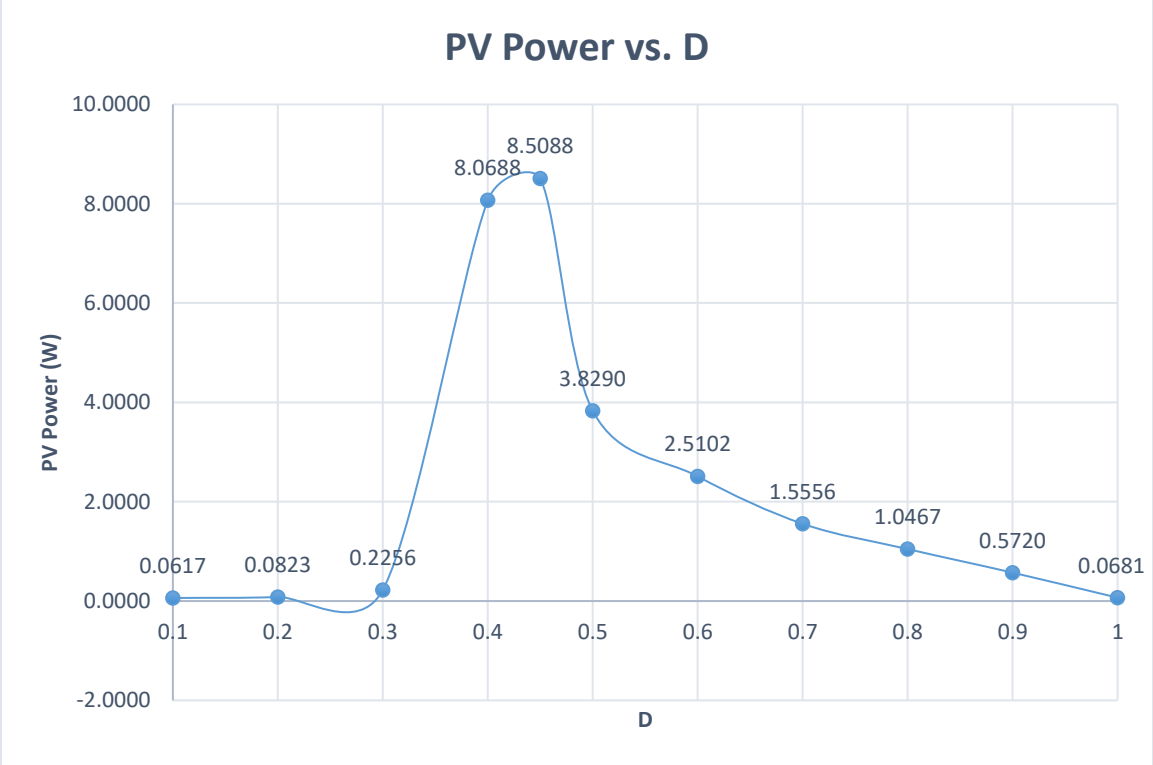


Figure 11. Panel Power vs. Duty Cycle

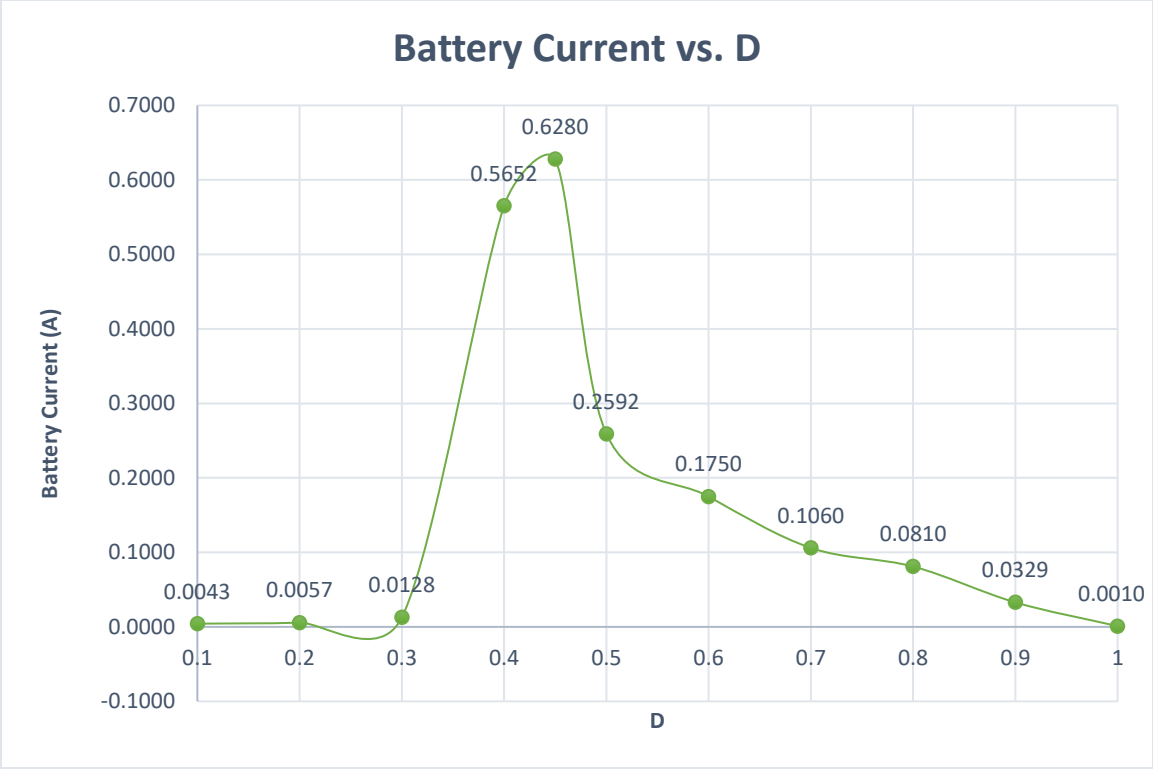


Figure 12. Battery Current vs. Duty Cycle

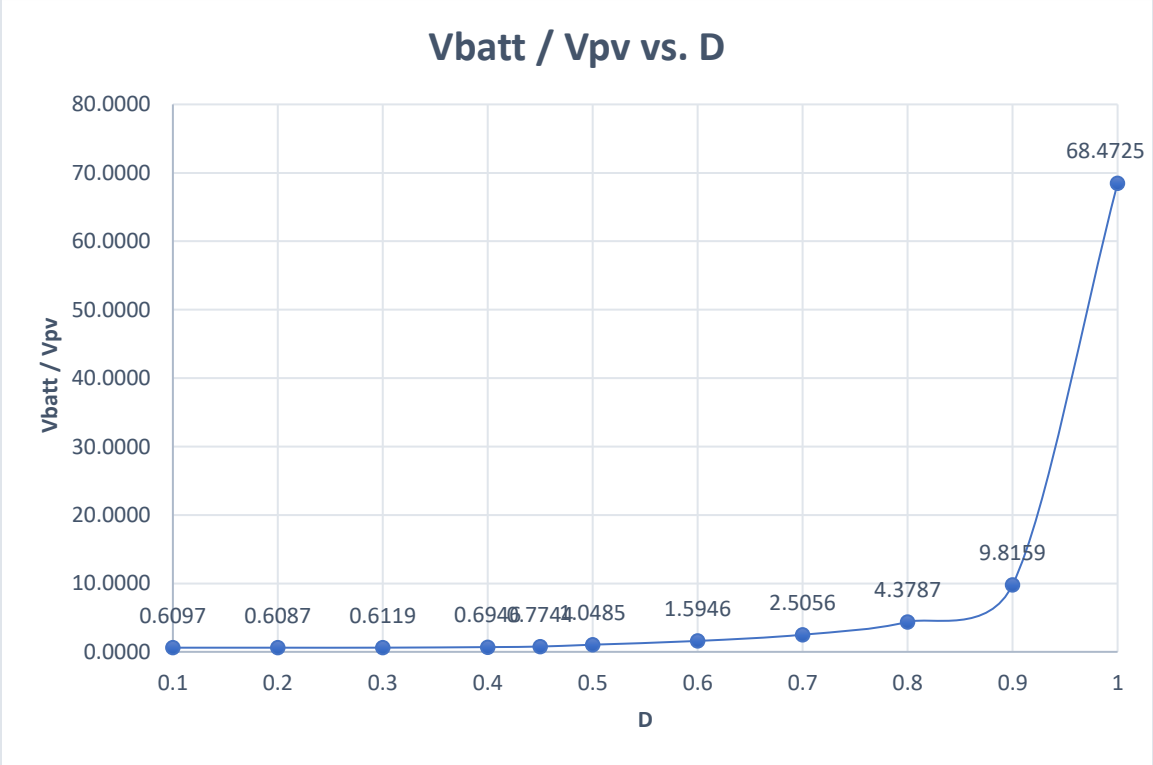
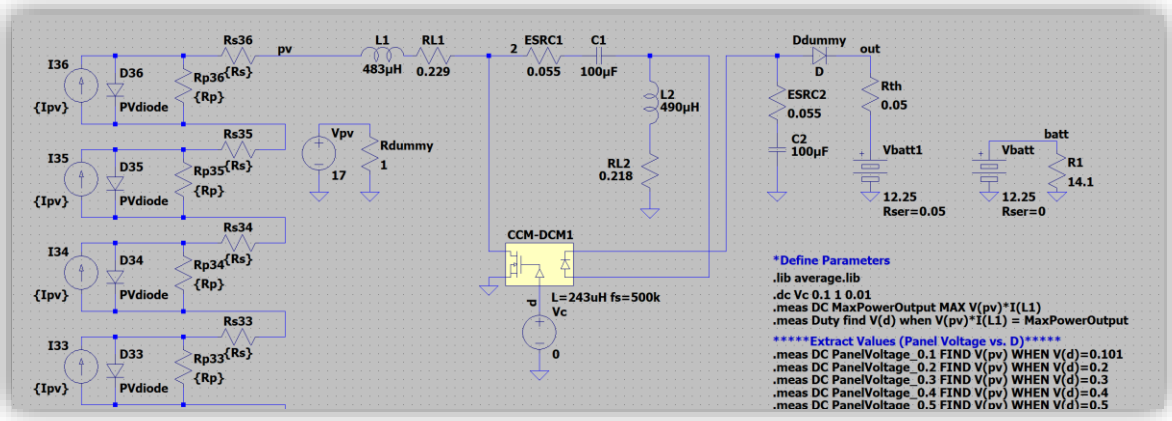


Figure 13. Battery Voltage / Panel Voltage vs. Duty Cycle

- Perform a dc simulation of this part, using LTspice or Simulink. Use your model developed in Experiment 1 for the PV panel, and use the Spice averaged switch model CCM-DCM1 (or your own Simulink equivalent) in place of the MOSFET and diode. Use a Thevenin equivalent for the battery. Sweep the duty cycle, and generate simulated versions of plots (i) - (iv) above.



For some reason, I have to put a Dummy Diode to prevent Current flowing back at low Duty Cycle range (when output lower than Battery Voltage).

I used the following commands to extract values from the graphs.

```
*Define Parameters
.lib average.lib
.dc Vc 0.1 1 0.01
.meas DC MaxPowerOutput MAX V(pv)*I(L1)
.meas Duty find V(d) when V(pv)*I(L1) = MaxPowerOutput

*****Extract Values (Panel Voltage vs. D)*****
.meas DC PanelVoltage_0.1 FIND V(pv) WHEN V(d)=0.101
.meas DC PanelVoltage_0.2 FIND V(pv) WHEN V(d)=0.2
.meas DC PanelVoltage_0.3 FIND V(pv) WHEN V(d)=0.3
.meas DC PanelVoltage_0.4 FIND V(pv) WHEN V(d)=0.4
.meas DC PanelVoltage_0.45 FIND V(pv) WHEN V(d)=0.45
.meas DC PanelVoltage_0.5 FIND V(pv) WHEN V(d)=0.5
.meas DC PanelVoltage_0.6 FIND V(pv) WHEN V(d)=0.6
.meas DC PanelVoltage_0.7 FIND V(pv) WHEN V(d)=0.7
.meas DC PanelVoltage_0.8 FIND V(pv) WHEN V(d)=0.8
.meas DC PanelVoltage_0.9 FIND V(pv) WHEN V(d)=0.9
.meas DC PanelVoltage_1.0 FIND V(pv) WHEN V(d)=1.0

*****Extract Values (Panel Power vs. D)*****
.meas DC PanelPower_0.1 FIND V(pv)*I(L1) WHEN V(d)=0.101
.meas DC PanelPower_0.2 FIND V(pv)*I(L1) WHEN V(d)=0.2
.meas DC PanelPower_0.3 FIND V(pv)*I(L1) WHEN V(d)=0.3
.meas DC PanelPower_0.4 FIND V(pv)*I(L1) WHEN V(d)=0.4
.meas DC PanelPower_0.45 FIND V(pv)*I(L1) WHEN V(d)=0.45
.meas DC PanelPower_0.5 FIND V(pv)*I(L1) WHEN V(d)=0.5
.meas DC PanelPower_0.6 FIND V(pv)*I(L1) WHEN V(d)=0.6
.meas DC PanelPower_0.7 FIND V(pv)*I(L1) WHEN V(d)=0.7
.meas DC PanelPower_0.8 FIND V(pv)*I(L1) WHEN V(d)=0.8
.meas DC PanelPower_0.9 FIND V(pv)*I(L1) WHEN V(d)=0.9
.meas DC PanelPower_1.0 FIND V(pv)*I(L1) WHEN V(d)=1.0

*****Extract Values (Battery Current vs. D)*****
.meas DC BatteryCurrent_0.1 FIND I(Rth) WHEN V(d)=0.101
.meas DC BatteryCurrent_0.2 FIND I(Rth) WHEN V(d)=0.2
.meas DC BatteryCurrent_0.3 FIND I(Rth) WHEN V(d)=0.3
.meas DC BatteryCurrent_0.4 FIND I(Rth) WHEN V(d)=0.4
.meas DC BatteryCurrent_0.45 FIND I(Rth) WHEN V(d)=0.45
.meas DC BatteryCurrent_0.5 FIND I(Rth) WHEN V(d)=0.5
.meas DC BatteryCurrent_0.6 FIND I(Rth) WHEN V(d)=0.6
.meas DC BatteryCurrent_0.7 FIND I(Rth) WHEN V(d)=0.7
.meas DC BatteryCurrent_0.8 FIND I(Rth) WHEN V(d)=0.8
.meas DC BatteryCurrent_0.9 FIND I(Rth) WHEN V(d)=0.9
.meas DC BatteryCurrent_1.0 FIND I(Rth) WHEN V(d)=1.0

*****Extract Values (Battery Voltage / Panel Votlage vs. D)*****
.meas DC Vbatt_Vpv_0.1 FIND V(batt)/V(pv) WHEN V(d)=0.101
.meas DC Vbatt_Vpv_0.2 FIND V(batt)/V(pv) WHEN V(d)=0.2
.meas DC Vbatt_Vpv_0.3 FIND V(batt)/V(pv) WHEN V(d)=0.3
.meas DC Vbatt_Vpv_0.4 FIND V(batt)/V(pv) WHEN V(d)=0.4
.meas DC Vbatt_Vpv_0.45 FIND V(batt)/V(pv) WHEN V(d)=0.45
.meas DC Vbatt_Vpv_0.5 FIND V(batt)/V(pv) WHEN V(d)=0.5
.meas DC Vbatt_Vpv_0.6 FIND V(batt)/V(pv) WHEN V(d)=0.6
.meas DC Vbatt_Vpv_0.7 FIND V(batt)/V(pv) WHEN V(d)=0.7
.meas DC Vbatt_Vpv_0.8 FIND V(batt)/V(pv) WHEN V(d)=0.8
.meas DC Vbatt_Vpv_0.9 FIND V(batt)/V(pv) WHEN V(d)=0.9
.meas DC Vbatt_Vpv_1.0 FIND V(batt)/V(pv) WHEN V(d)=1.0
```

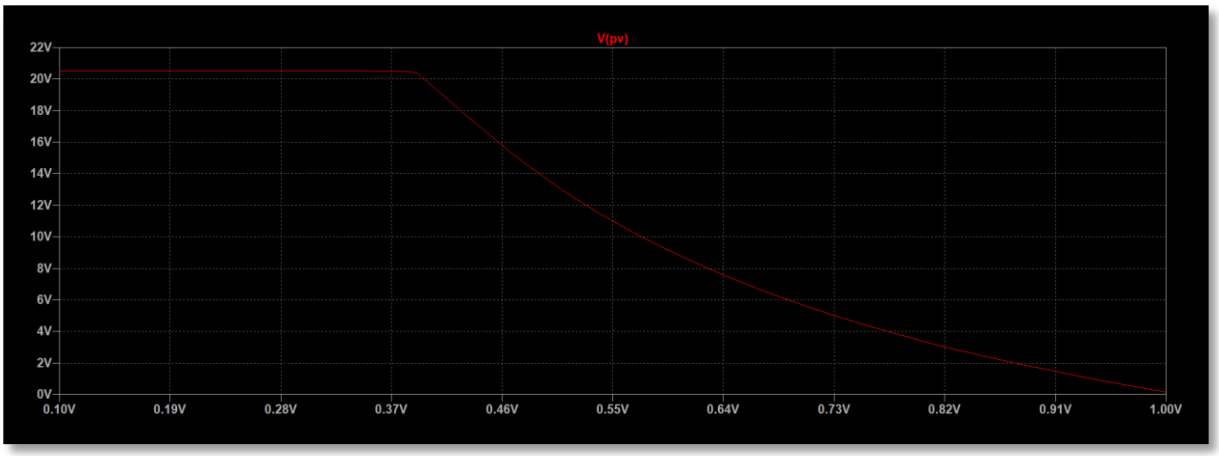


Figure 14. Panel Voltage vs. Duty Cycle (LTSpice)

```
panelvoltage_0.1: v(pv)=20.5476 at 0.101
panelvoltage_0.2: v(pv)=20.5378 at 0.2
panelvoltage_0.3: v(pv)=20.5215 at 0.3
panelvoltage_0.4: v(pv)=19.7606 at 0.4
panelvoltage_0.45: v(pv)=16.4405 at 0.45
panelvoltage_0.5: v(pv)=13.4441 at 0.5
panelvoltage_0.6: v(pv)=8.96316 at 0.6
panelvoltage_0.7: v(pv)=5.79278 at 0.7
panelvoltage_0.8: v(pv)=3.43315 at 0.8
panelvoltage_0.9: v(pv)=1.61165 at 0.9
panelvoltage_1.0: v(pv)=0.162692 at 1
```

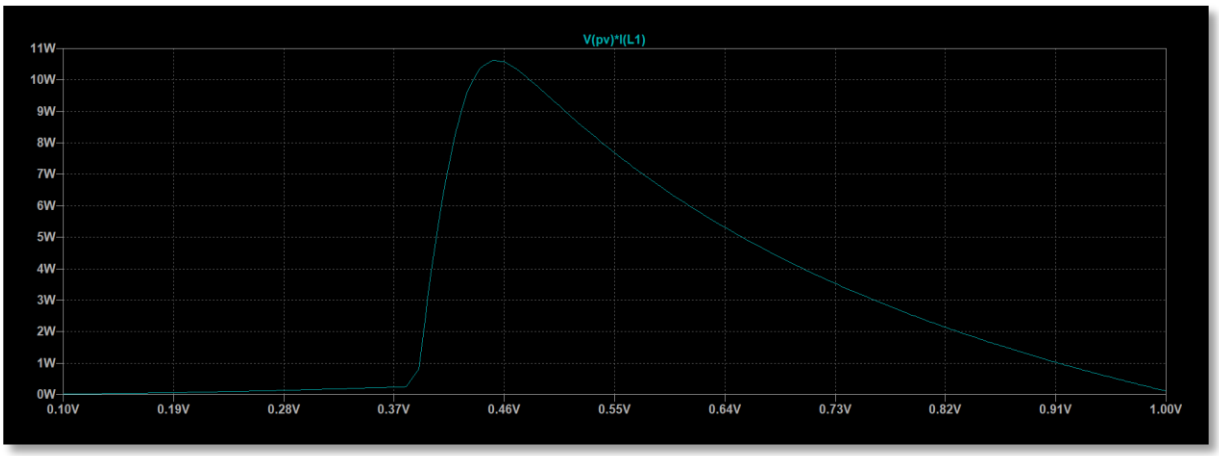


Figure 15. Panel Power vs. Duty Cycle (LTSpice)

```
panelpower_0.1: v(pv)*i(l1)=0.0177393 at 0.101
panelpower_0.2: v(pv)*i(l1)=0.06943 at 0.2
panelpower_0.3: v(pv)*i(l1)=0.155962 at 0.3
panelpower_0.4: v(pv)*i(l1)=3.81503 at 0.4
panelpower_0.45: v(pv)*i(l1)=10.6265 at 0.45
panelpower_0.5: v(pv)*i(l1)=9.33833 at 0.5
panelpower_0.6: v(pv)*i(l1)=6.27746 at 0.6
panelpower_0.7: v(pv)*i(l1)=4.07171 at 0.7
panelpower_0.8: v(pv)*i(l1)=2.41956 at 0.8
panelpower_0.9: v(pv)*i(l1)=1.13816 at 0.9
panelpower_1.0: v(pv)*i(l1)=0.115081 at 1
```

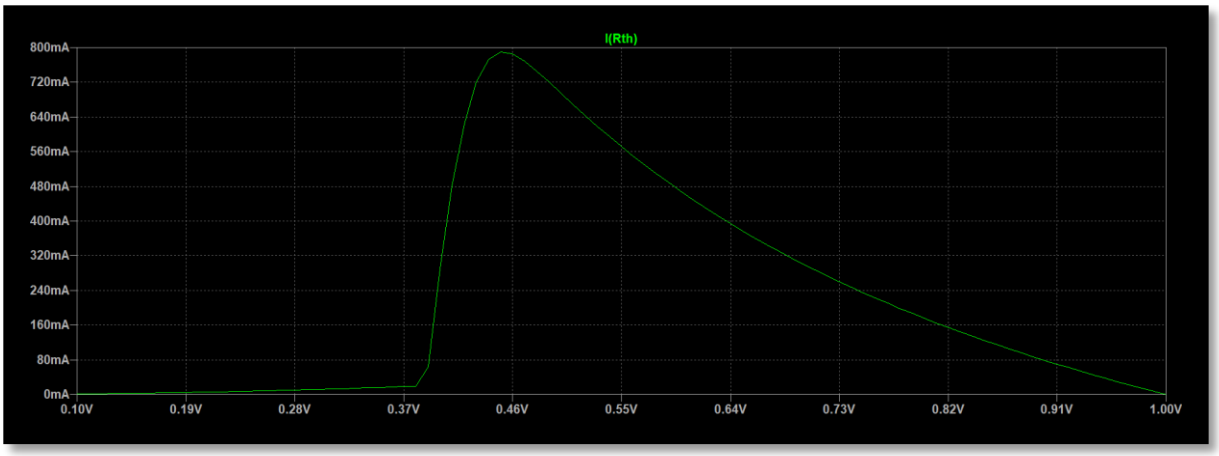


Figure 16. Battery Current vs. Duty Cycle (LTSpice)

```
batterycurrent_0.1: i(rth)=0.00137365 at 0.101
batterycurrent_0.2: i(rth)=0.00536106 at 0.2
batterycurrent_0.3: i(rth)=0.0120207 at 0.3
batterycurrent_0.4: i(rth)=0.289593 at 0.4
batterycurrent_0.45: i(rth)=0.79 at 0.45
batterycurrent_0.5: i(rth)=0.694157 at 0.5
batterycurrent_0.6: i(rth)=0.466585 at 0.6
batterycurrent_0.7: i(rth)=0.301035 at 0.7
batterycurrent_0.8: i(rth)=0.176053 at 0.8
batterycurrent_0.9: i(rth)=0.0784676 at 0.9
batterycurrent_1.0: i(rth)=-3.55271e-014 at 1
```

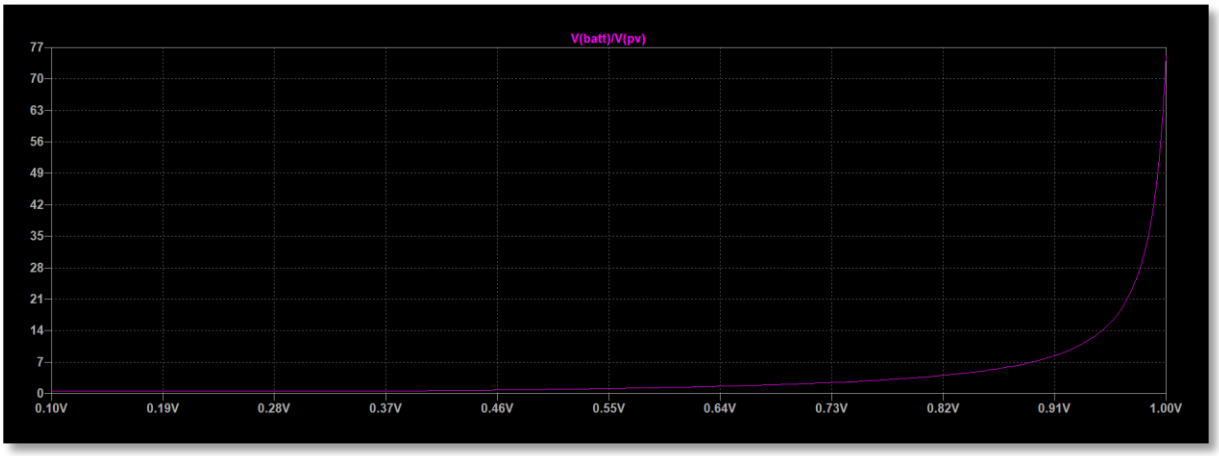


Figure 17. Battery Voltage / Panel Voltage vs. Duty Cycle (LTSpice)

```
vbatt_vpv_0.1: v(batt)/v(pv)=0.596177 at 0.101
vbatt_vpv_0.2: v(batt)/v(pv)=0.59646 at 0.2
vbatt_vpv_0.3: v(batt)/v(pv)=0.596935 at 0.3
vbatt_vpv_0.4: v(batt)/v(pv)=0.619921 at 0.4
vbatt_vpv_0.45: v(batt)/v(pv)=0.74511 at 0.45
vbatt_vpv_0.5: v(batt)/v(pv)=0.911182 at 0.5
vbatt_vpv_0.6: v(batt)/v(pv)=1.36671 at 0.6
vbatt_vpv_0.7: v(batt)/v(pv)=2.1147 at 0.7
vbatt_vpv_0.8: v(batt)/v(pv)=3.56815 at 0.8
vbatt_vpv_0.9: v(batt)/v(pv)=7.60091 at 0.9
vbatt_vpv_1.0: v(batt)/v(pv)=75.2957 at 1
```

- How do your measured and simulated plots compare with the theoretical model of the SEPIC? If you choose the optimum duty cycle, how much power can you obtain? How does this compare with the direct energy transfer approach used to charge the battery in Experiment 1?

At the time of measurement, 12:00pm 10/02/2021 New York, the Solar Panel might not be at its maximum output, it was a semi cloudy day, so the best I got was 8.5W which is exactly on 0.45 Duty Cycle, the shapes of the reading plots are identical to what I have simulated in LTSpice. Notice that at duty cycle below ~0.37 the SEPIC cannot make higher output than the battery voltage, hence nothing should flow in the battery, the minor output of the Panel Power at low duty cycle are the losses of the lossy elements of the Converter itself.

With LTSpice, the maximum Power point vs. Duty can also obtained with the following command:

```
.meas DC MaxPowerOutput MAX V(pv)*I(L1)
.meas Duty find V(d) when V(pv)*I(L1) = MaxPowerOutput

maxpoweroutput: MAX(v(pv)*i(l1))=10.6265 FROM 0.1 TO 1
duty: v(d)=0.45 at 0.45
```

It also proves that at 0.45 Duty Cycle can achieve Maximum Power Transfer. And with optimum Sun Reading, I should get 10.6265W out of it. At Experiment one direct energy transfer, I have around 16.4Vdc and 0.64A battery charging current, which is around 10.496W, with the SEPIC it is also proofed that can achieve slightly higher charging power and maintain optimum Output voltage to keep Battery healthy.

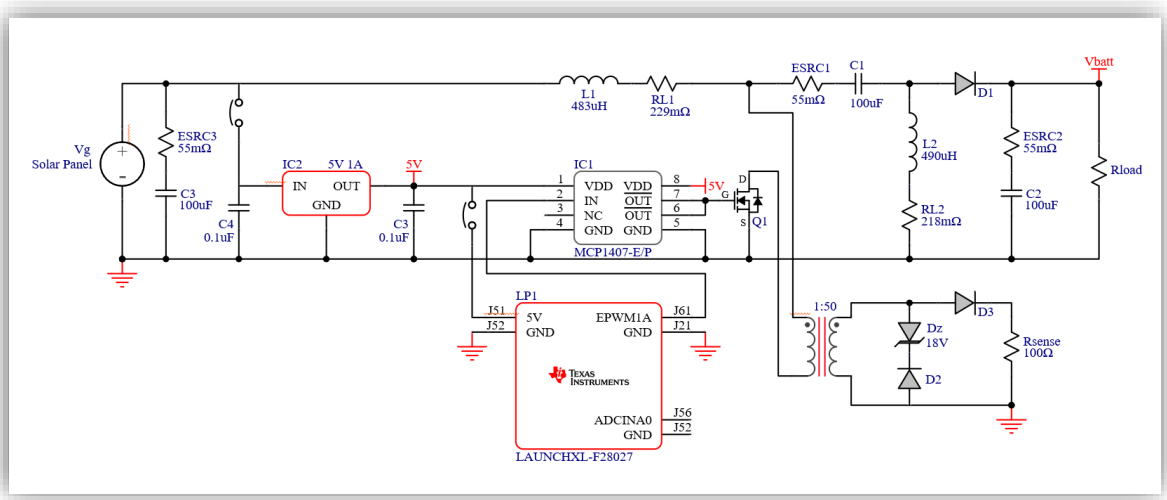


Figure 18. Diagram of my SEPIC including losses elements.

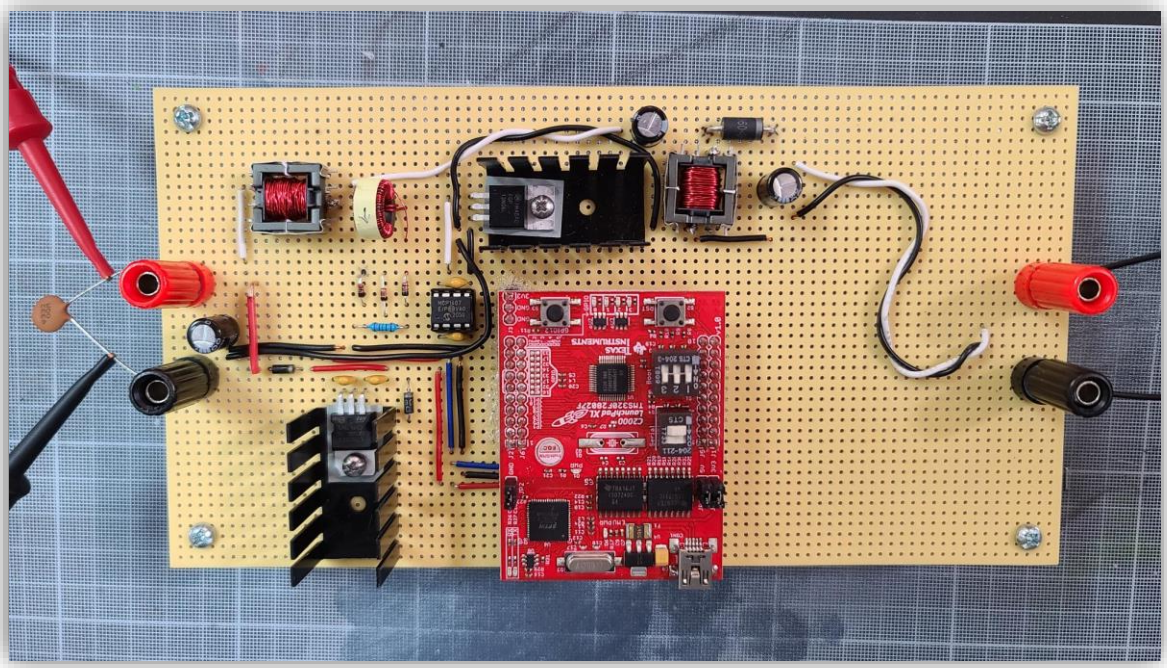


Figure 19. My SEPIC

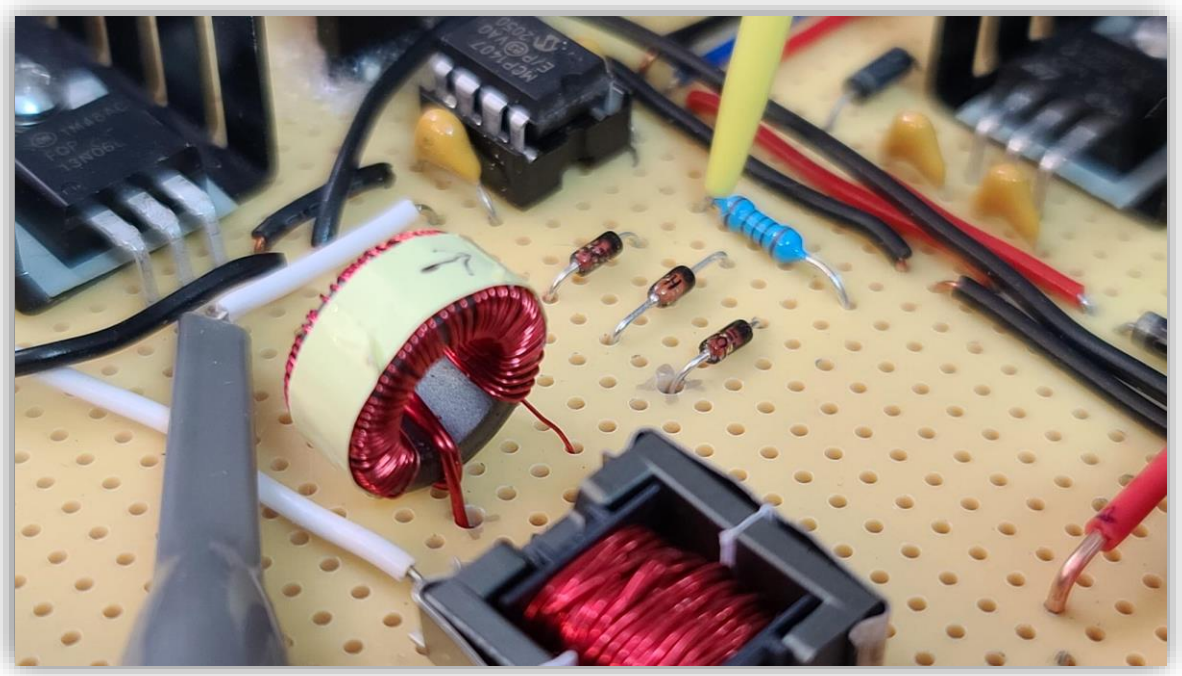


Figure 20. Current Sensing Transformer and Sensing Circuit

Figure 21. Setup on 10/02/2021 12:00pm New York

Sources:
[1] https://www.tdk-electronics.tdk.com/inf/80/db/fer/efd_15_8_5.pdf
[2] https://www.tdk-electronics.tdk.com/download/531516/449506bb84194c3510018ae82f66b4cc/pdf-ecoresgeneralinformation.pdf
[3] https://datasheet.octopart.com/FQP13N06L-ON-Semiconductor-datasheet-137330032.pdf
[4] https://datasheet.octopart.com/SB320-ON-Semiconductor-datasheet-80929452.pdf
[5] https://www.mouser.com/datasheet/2/315/PANA_S_A0012465572_1-2522329.pdf