Milestone #1
Power Stage Design

Capstone Design Project
Coursera Specialization in Power Electronics
University of Colorado, Boulder

Milestones for Weeks 1-2

This is the submission of Milestone 1, documenting your preliminary power stage design. Your submission will be graded by three other learners, according to the instructions and rubrics defined in this document.

Please read these review criteria and follow them closely, both in your submission and in your grading of the submissions of other learners. Everybody must review at least three peer submissions; many learners choose to review more than three, to help their fellow learners.

You will be allowed to submit only once, so be sure that all parts are correct and complete.

1 Approach

Make a screen shot of your LTspice circuit, and paste it into the field below. Add a few sentences describing your converter approach, and how it is able to operate at point 1 (supply USB at 5 V), point 2 (supply USB at 20 V), and point 3 (charge battery), all with the same three-cell LiPo battery. The battery ground and USB ground should be connected. The schematic screen shot should include only your circuit—it is not necessary to include the header part provided in **milestone1.asc** (simulation commands and parameters, control signals, battery and bus models, measurement commands).

1.1 Rubric 1

Is the approach briefly described, and is a schematic included? Is the approach capable of operating at points 1, 2, and 3 described above?

- Yes [70 points]
- No [0 points]

1.2 Rubric 2

Optional comments by reviewer, no points.

2 Inductor Design

In the power stage, each inductor should be designed following the Kg method presented in Course 5 of this specialization. You must use a ferrite core (or ferrite cores) with core material having the following LTspice $B - H$ loop parameters: Hc = 10, Br = 0.12, Bs = 0.33 (so the saturation flux density is approximately 0.33 Tesla). The inductors must not saturate in steady-state operation at the worst-case operating point. For *each inductor* in your power converter report the following:

1. Worst-case operating point for the inductor design: state Vbat, Vout, and Iout
2. DC value IL of the inductor current at the worst-case operating point: include equations used to calculate IL, and report IL value as a number with units.
3. Selected inductance L: include equations used to calculate L, and report inductance L as a number with units.
4. Required Kg: include equations used to calculated Kg, and report the value as a number with units.
5. Selected core size: justify how you selected the core size, and report the selected core size. You must use cores in the magnetics design tables of standard cores provided in the course (file "AppendixD.pdf").
6. Selected air gap lg: include equations used to calculate lg and report the value of lg as a number with units.
7. Selected number of turns n and wire gauge AWG: include equations used to select n and AWG and report the values as numbers.
8. Predicted Bmax in steady-state operation at the worst-case operating point: include equations used to calculate Bmax, and report the value found as a number with units. Does the inductor saturate at the worst-case operating point?
9. Report the total weight of the cores used in the design as a number in grams. The weights of all standard cores are listed in the magnetics design tables. Include only the weight of the ferrite, not the copper or other parts of the inductors.

Enter your inductor design report as text in the space provided below. You may include your report as an *easily readable* image of your work (hand-written or entered on a computer). It is highly recommended that you make it obvious to the reviewers where to find your answer to each enumerated section above.

2.1 Rubric 1

Worst-case operating point for the inductor design: state Vbat, Vout, and Iout

- Section 1 is not included [0 points]
- Section 1 is included and the worst-case operating point is not selected correctly for at least one of the inductors in the power stage. [2 points]
- Section 1 is included and the worst-case operating point is selected correctly for all inductors in the power stage. [5 points]

2.2 Rubric 2

DC value IL of the inductor current at the worst-case operating point: include equations used to calculate IL, and report IL value as a number with units.

- Section 2 is not included [0 points]
- Section 2 is included but the calculation of IL is incorrect for at least one of the inductors. [2 points]
- Section 2 is included and calculations of IL are correct for all inductors in the power stage. [5 points]

2.3 Rubric 3

Selected inductance L: include equations used to calculate L, and report inductance L as a number with units.

- Section 3 is not included. [0 points]
- Section 3 is included but the calculation if L is incorrect for at least one of the inductors. [2 points]
- Section 3 is included and calculations of L are correct for all inductors in the power stage. [5 points]

2.4 Rubric 4

Required Kg: include equations used to calculated Kg, and report the value as a number with units.

- Section 4 is not included. [0 points]
- Section 4 is included but the calculations of Kg are incorrect for at least one of the inductors. [2 points]
- Section 4 is included and calculations of Kg are correct for all inductors in the power stage. [5 points]

2.5 Rubric 5

Selected core size: justify how you selected the core size, report the selected core size.

- Section 5 not included [0 points]
- Section 5 is included but a justification is not provided or is incorrect or employs nonstandard cores for at least one of the inductors. [2 points]
- Section 5 is included and correct justification is provided for core selection for all inductors in the power stage. All cores are selected from the course magnetics design tables of standard cores. [5 points]

2.6 Rubric 6

Selected air gap lg: include equations used to calculate lg and report the value of lg as a number with units.

- Section 6 is not included [0 points]
- Section 6 is included but calculation of lg is not provided or is incorrect for at least one of the inductors. [2 points]
- Section 6 is included and calculation of lg is correct for all inductors in the power stage. [5 points]

2.7 Rubric 7

Selected number of turns n and wire gauge AWG: include equations used to select n and AWG and report the values as numbers.

- Section 7 is not included. [0 points]
- Section 7 is included but calculations of n and AWG are not provided or are incorrect for at least one of the inductors. [2 points]
- Section 7 is included and calculations of n and AWG are correct for all inductors in the power stage. [5 points]

2.8 Rubric 8

Predicted Bmax in steady-state operation at the worst-case operating point: include equations used to calculate Bmax, and report the value found as a number with units. Is Bmax < 0.33 T?

- Section 8 is not included [0 points]
- Section 8 is included but calculations of Bmax are not provided or are incorrect, or Bmax ≥ 0.33 T for at least one of the inductors. [2 points]
- Section 8 is included and calculations of Bmax are correct and Bmax < 0.33 T for all inductors in the power stage. [5 points]

2.9 Rubric 9

Report the total weight of the cores used in the design as a number in grams. The weights of all standard cores are listed in the magnetics design tables.

- Section 9 is not included, or total core weight reported is greater than or equal to 50 g. [0 points]
- Total core weight reported is less than 50 g but greater than or equal to 20 g. [2 points]

- Total core weight reported is less than 20 g but greater than or equal to 10 g. [5 points]
- Total core weight reported is less than 10 g but greater than or equal to 5 g. [8 points]
- Total core weight reported is less than 5 g. [10 points]

3 Capacitor Design

In the power stage, each capacitor should be selected following the principles presented in Course 1 of this specialization. The capacitor voltage ripple at the battery and USB terminals must be no greater than 0.1 V peak-to-peak in steady-state operation at the worst-case operating point. For any internal power stage capacitors, you may make your own choice for voltage ripple. For *each capacitor* in your power converter report the following:

- Worst-case operating point for the capacitor design: state Vbat, Vout, and Iout
- Selected capacitance C: include equations used to calculate C, and report capacitance C as a number with units. For capacitors internal to the converter, report the ripple requirement that was chosen.
- Report the sum of all power stage capacitances used in the design as a number in microfarads.

Enter your capacitor design report as text in the space provided below. You may include your report as an *easily readable* image of your work (hand-written or entered on a computer).

3.1 Rubric 1

Worst-case operating point for the capacitor design: state Vbat, Vout, and Iout.

- Section 1 is not included. [0 points]
- Section 1 is included and the worst-case operating point is not selected correctly for at least one of the capacitors in the power stage. [2 points]
- Section 1 is included and the worst-case operating point is selected correctly for all capacitors in the power stage. [5 points]

3.2 Rubric 2

Selected capacitance C: include equations used to calculate C, and report capacitance C as a number with units. For capacitors internal to the converter, report the ripple requirement that was chosen.

- Section 2 is not included. [0 points]
- Section 2 is included but the calculation of C is incorrect for at least one of the capacitors. [2 points]
- Section 2 is included and calculations of C are correct for all capacitors in the power stage. [5 points]

3.3 Rubric 3

Report the sum of all power stage capacitances used in the design as a number in microfarads.

- Section 3 is not included, or total capacitance reported is greater than or equal to 1000 microfarads. [0 points]
- Total capacitance reported is less than 1000 microfarads but greater than or equal to 500 microfarads. [2 points]
- Total capacitance reported is less than 500 microfarads but greater than or equal to 200 microfarads. [5 points]
- Total capacitance reported is less than 200 microfarads but greater than or equal to 100 microfarads. [8 points]
- Total capacitance reported is less than 100 microfarads. [10 points]

4 Semiconductor Design

In the power stage, each transistor or diode should be selected following the principles presented in Course 1 of this specialization. You must use semiconductors included in the LTspice library of components. The worst-case maximum voltage applied by your converter to each semiconductor device (including switching ripple) must be no greater than 2/3 of the rated voltage of the device. For *each transistor or diode* in your power converter report the following:

1. Worst-case operating point for the semiconductor design: state Vbat, Vout, and Iout that leads to the peak voltage reported in part 2 below.
2. Peak applied voltage: report the maximum voltage applied by the converter to the semiconductor device (include ripple), and the required device voltage rating.
3. Selected device: report the part number that you selected, with its voltage and current ratings. For MOSFETs, also report the nominal on-resistance.

Enter your semiconductor design report as text in the space provided below. You may include your report as an *easily readable* image of your work (hand-written or entered on a computer).

4.1 Rubric 1

Worst-case operating point for the semiconductor design: state Vbat, Vout, and Iout that leads to the peak voltage reported in part 2 below.

- Section 1 is not included. [0 points]
- Section 1 is included and the worst-case operating point is not selected correctly for at least one of the semiconductors in the power stage. [2 points]
- Section 1 is included and the worst-case operating point is selected correctly for all semiconductors in the power stage. [5 points]

4.2 Rubric 2

Peak applied voltage: report the maximum voltage applied by the converter to the semiconductor device (including ripple), and the required device voltage rating.

- Section 2 is not included. [0 points]
- Section 2 is included but the calculation of peak voltage is incorrect for at least one of the semiconductor devices. [2 points]
- Section 2 is included and calculations of peak voltage are correct for all power stage semiconductors. [5 points]

4.3 Rubric 3

Selected devices: report the part numbers that you selected, with voltage and current ratings. For MOSFETs, also report the nominal on-resistance.

- Section 3 is not included. [0 points]
- Section 3 is included but at least one calculated peak voltage is greater than 2/3 of the reported semiconductor voltage rating. [2 points]
- Section 3 is included and all calculated peak voltages are no greater than 2/3 of the reported semiconductor voltage ratings. [5 points]

5 Simulations

Place your LTspice files into a dedicated folder. Make sure all simulations run correctly using the files in that folder. Remove all .raw files, but include all files necessary to run the required simulations (all .sch. .asy, .lib files). Create a .zip file of the folder and upload this .zip file here.

Your LTspice files must include the Milestone1 LTspice template **milestone1.sch**, which tests your converter prototype at the three operating points:

1. USB 5V at 2A, Vbatt = 12.6V
2. USB 20V at 3A, Vbatt = 9.6V
3. Battery charging, USB 20 V at 60W, Vbatt = 11.1V

You should adjust the parameters **t1**, **t2**, and **Tend** as necessary so that the template measurements of the three operating points are made in steady state. Your simulation should use the control signal parameters **Vref1_5V**, **Vref1_20V**, etc., to set the open-loop duty cycle(s) of your converter(s) as necessary to reach the three operating points defined above, and you should adjust these parameters as well. Also define the flux density scale factor **BscaleL1** (if you have two inductors then add **BscaleL2**), and switching period parameter **Ts** so that the template produces accurate measurements.

5.1 Rubric 1

The LTspice file can be downloaded and run. The simulation correctly employs the provided template. No dependent sources or independent sources are used, other than those provided in the template. All inductors are implemented using the LTspice saturating inductor model.

- No LTspice file provided, or zip files are incomplete such that the simulation will not run. In this case, enter zero for the remaining rubrics. [0 points]
- The LTspice simulation runs. However, one or more of the following rules are violated:
  - The simulation correctly employs the provided template.
  - No dependent sources or independent sources are used, other than those provided in the template.
  - All inductors are implemented using the LTspice saturating inductor model.

  [4 points]
- The LTspice simulation runs. The LTspice simulation conforms to all of the following rules:
  - The simulation correctly employs the provided template.
  - No dependent sources or independent sources are used, other than those provided in the template.
  - All inductors are implemented using the LTspice saturating inductor model.

  [10 points]

5.2 Rubric 2

For this and all remaiuning rubrics, run a transient (**.tran**) simulation, plot v(out) and inductor current waveform(s), and inspect measurement results in the output .log file.

At time t1, is the converter in steady state at operating point 1, and is the **Vout_5V** measurement within the range 5 V ± 0.1V?

- Yes [5 points]
- No [0 points]

5.3 Rubric 3

At time t2, is the converter in steady state at operating point 2, and is the **Vout_20V** measurement within the range 20 V ± 0.1V?

- Yes [5 points]
- No [0 points]

5.4 Rubric 4

At time t2, is the converter in steady state at operating point 2, and are the peak-to-peak ripple measurements **Vin_ripple_20V** and **Vout_ripple_20V** less than or equal to 0.1 V?

- Yes [5 points]
- No [0 points]

5.5 Rubric 5

At time t2, is the converter in steady state at operating point 2, and are maximum flux density measurements **Bmax_L1** (and **Bmax_L2**, etc. for any additional inductors) all less than or equal to 0.33 T (indicating that inductors do not saturate)?

- Yes [5 points]
- No [0 points]

5.6 Rubric 6

This rubric should receive credit only if the converter is in steady-state and meets dc voltage requirements at t = t2, operating point 2. Otherwise check the 0 points option.

- Measured efficiency **eff_20V** is less than 80%. [0 points]
- Measured efficiency **eff_20V** is greater than or equal to 80% but is less than 85%. [2 points]
- Measured efficiency **eff_20V** is greater than or equal to 85% but is less than 90%. [5 points]
- Measured efficiency **eff_20V** is greater than or equal to 90% but is less than 95%. [8 points]
- Measured efficiency **eff_20V** is greater than or equal to 95%. [10 points]

5.7 Rubric 7

At time Tend, is the converter in steady state at operating point 3, and is bus charging current measurement **Ibus_chg** within the range 3 A ± 0.1V?

- Yes [10 points]
- No [0 points]