Milestone #3

Power Stage Design

Capstone Design Project in Power Electronics
ECEA 5715
University of Colorado, Boulder

Milestones for Weeks 5-6

This is the submission of Milestone 3, documenting your final design of the closed-loop controlled converter that meets the project requirements. You are expected to construct a complete switching circuit model of the closed-loop converter and verify the design using transient (time-domain) simulations. Your submission will be graded by three other learners, according to the instructions and rubrics defined in this document.
Please read these review criteria and follow them closely, both in your submission and in your grading of the submissions of other learners. Everybody must review at least three peer submissions; many learners choose to review more than three, to help their fellow learners.
You will be allowed to upload your submission only once, so be sure that all parts are correct and complete.

1 Approach

Upload a screen shot of the LTspice circuit model of your closed-loop controlled converter. The screen shot should include only your circuit. It is not necessary to include the template header provided in milestone3.asc (simulation commands and parameters, control signals, battery and bus models, measurement commands).
Add a brief description of your final closed-loop converter design including:

1. A summary of the converter topology and the control techniques employed.
2. A summary of how you implemented current limiting in your design.
3. The magnetic cores used in the design and the total weight of the cores in grams.
4. The sum of all power stage capacitances used in the design in microfarads.

1.1 Rubric 1

Is the approach briefly described, and is a schematic included?

- Yes [40 points]
- No [0 points]

1.2 Rubric 2

What is the reported total weight of the cores used in the design as a number in grams?

- Weight not reported, or total core weight reported is greater than or equal to 50 g. [0 points]
- Total core weight reported is less than 50 g but greater than or equal to 20 g. [3 points]
- Total core weight reported is less than 20 g but greater than or equal to 10 g. [8 points]
- Total core weight reported is less than 10 g but greater than or equal to 5 g. [12 points]
- Total core weight reported is less than 5 g. [15 points]

1.3 Rubric 3

What is the reported sum of all power stage capacitances used in the design in microfarads?

- Total capacitance not reported and not visible on the schematic, or total capacitance reported is greater than or equal to 1000 microfarads. [0 points]
- Total capacitance reported is less than 1000 microfarads but greater than or equal to 500 microfarads. [3 points]
- Total capacitance reported is less than 500 microfarads but greater than or equal to 200 microfarads. [8 points]
- Total capacitance reported is less than 200 microfarads but greater than or equal to 100 microfarads. [12 points]
- Total capacitance reported is less than 100 microfarads. [15 points]

1.4 Rubric 4

Based on the schematic, is the converter bidirectional and is it capable of both step-up and step-down operation?

- Yes [30 points]
- No [0 points]

1.5 Rubric 5

Optional comments by reviewer, no points.

2 Simulations

Place your Milestone 1 LTspice files into a dedicated folder. Make sure all simulations run correctly using the files in that folder. Remove all .raw files, but include all files necessary to run the required simulations (all .sch. .asy, .lib files). Create a .zip file of the folder and upload this .zip file.
The folder must include a single schematic (.sch) file that contains the template header from milestone3.sch and the circuit model of your closed-loop controlled converter. Note that the template header milestone3.sch ignores simulation results for the first Tskip = 0.5 ms. This is to allow any converter capacitors to be initially charged from the battery before the converter commences normal operation including current limiting. The template header tests your converter prototype at three operating points, in this order:

1. USB output 5V at 2A, Vbatt = 12.6V, steady-state operation expected at time=t1-Tskip
2. USB output 20V at 2.25A, Vbatt = 9.6V, steady-state operation expected at time=t2-Tskip
3. USB output 20V at 3A, Vbatt = 9.6V, steady-state operation expected at time=Tend-Tskip

In addition, the template tests the converter under a step load transient from 2.25A to 3A at at time=t2 for the output USB output voltage equal to 20V.
In the template header you should adjust the parameters **t1**, **t2**, and **Tend** as necessary so that the template measurements of the steady-state operating points and the step-load transient are made correctly. Your simulation should use the control signal parameters **Vref1_5V**, **Vref1_20V**, (and **Vref2_5V**, **Vref2_20V** if the second control signal source is used), to set the reference(s) for your control loop(s) as necessary to reach the steady-state operating points defined above, and you should adjust these parameters as well. Also define the switching period parameter **Ts** so that the template produces accurate measurements.

2.1 Rubric 1

The LTspice file can be downloaded and run. The simulation correctly employs the provided template. No dependent sources or independent sources or other excluded components are used, other than those provided in the template. All inductors are implemented using the LTspice saturating inductor model, and include inductor series resistances.

- No LTspice file provided, or zip files are incomplete such that the simulation will not run, or simulation does not converge. In this case, enter zero for the remaining rubrics. [0 points]
- The LTspice simulation runs. However, one or more of the following rules are violated:
  - The simulation correctly employs the provided template.
  - No dependent sources or independent sources or other excluded components are used, other than those provided in the template.
  - All inductors are implemented using the LTspice saturating inductor model, and inductor series resistances are included.

[5 points]

- The LTspice simulation runs. The LTspice simulation conforms to all of the following rules:
  - The simulation correctly employs the provided template.
  - No dependent sources or independent sources or other excluded components are used, other than those provided in the template.
  - All inductors are implemented using the LTspice saturating inductor model, and inductor series resistances are included.

[20 points]

2.2 Rubric 2

For this and all remaining rubrics, run a transient (**.tran**) simulation, plot v(out) and inductor current waveform(s), and inspect measurement results in the output .log file.
At time=t1-Tskip, is the converter in steady state, and is **Vout_5V** measurement within the range 5 V ± 0.1V?

- Yes [15 points]
- No [0 points]

2.3 Rubric 3

Efficiency. This rubric should receive credit only if the converter is in steady-state and meets dc voltage requirements (20 V ± 0.1 V) at the end of simulation at t=Tend-Tskip. Otherwise check the 0 points option.

- Measured efficiency **eff_20V** is less than 80%. [0 points]
- Measured efficiency **eff_20V** is greater than or equal to 80% but is less than 85%. [4 points]
- Measured efficiency **eff_20V** is greater than or equal to 85% but is less than 90%. [10 points]
- Measured efficiency **eff_20V** is greater than or equal to 90% but is less than 95%. [16 points]
- Measured efficiency **eff_20V** is greater than or equal to 95%. [20 points]

2.4 Rubric 4

Verification of step-load transient response. This rubric should receive credit only if the converter is in steady-state and meets dc voltage requirements (20 V ± 0.1 V) at time=t2-Tskip, and at the end of simulation at time=Tend-Tskip. Otherwise check No.
Inspect measurement results in the output .log file for the minimum voltage **Vout_20V_min** found after the step load transient at time=t2-Tskip. Is **Vout_20V_min** greater than or equal to 19.5 V?

- Yes [20 points]
- No [0 points]

2.5 Rubric 5

At at the end of simulation, at time=Tend-Tskip, is the converter in steady state, is the output dc voltage **Vout_20V** in the range 20 V ± 0.1 V, and are the input voltage peak-to-peak ripple **Vin_ripple_20V** and the output voltage peak-to-peak ripple **Vout_ripple_20V** both less than or equal to 0.1V? Check No if any of these requirements are not met.

- Yes [10 points]
- No [0 points]

2.6 Rubric 6

Verify current limiting. Based on inspection of the inductor current waveforms, does any of the inductors saturate at any time during simulation?

- No [15 points]
- Yes [0 points]

2.7 Rubric 7

Optional comments by reviewer, no points.