SOC LAB3 Report

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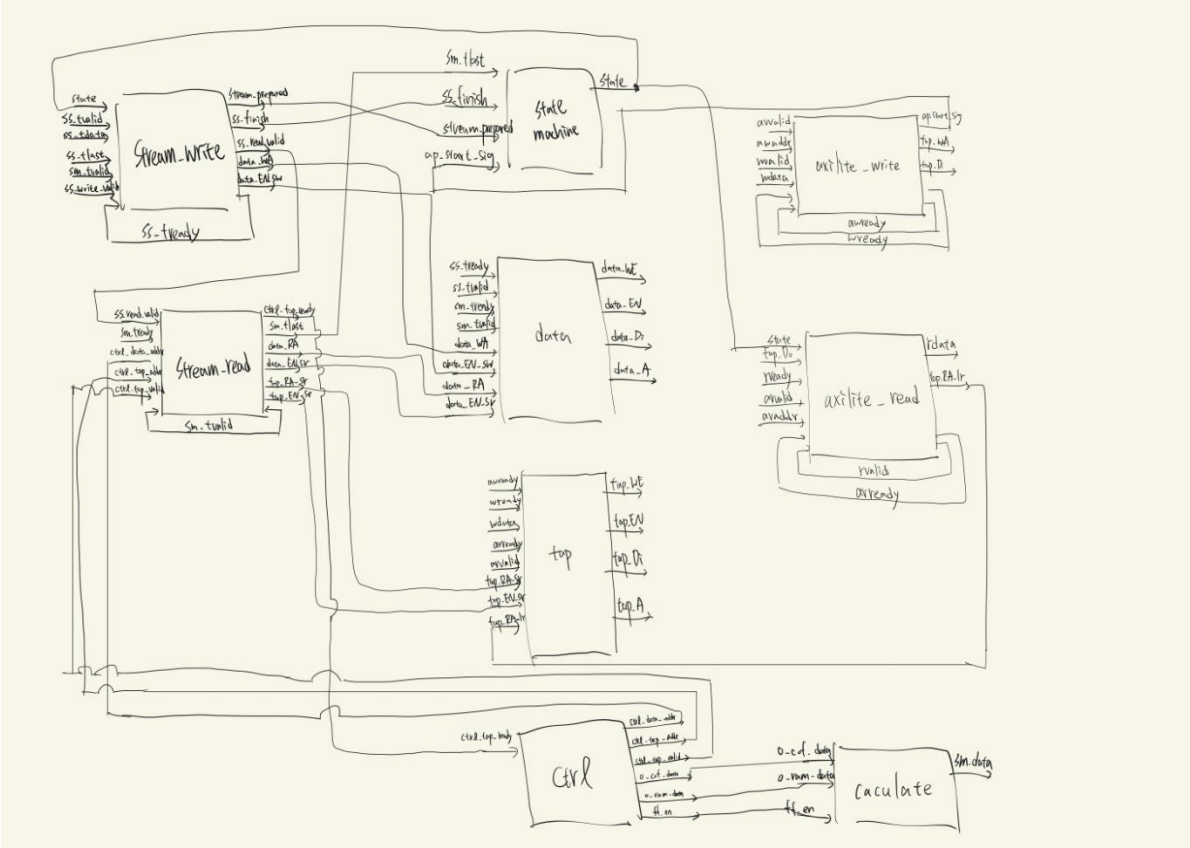
1.Block Diagram



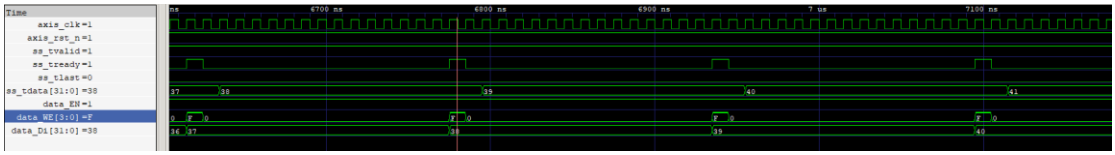
2.Describe operation

How to receive data-in and tap parameters and place into SRAM:

Data:

透過 AXI4_Stream 控制 data，當 data producer 要傳送至 data consumer 時，put initial TDATA、TLAST on the bus，透過 TVALID 告知 consumer 資料已經準備好了，接收端透過 TREADY 表達可以開始接收，因此當 TVALID 和 TREADY 皆為 HIGH 時，資料開始 transfer。

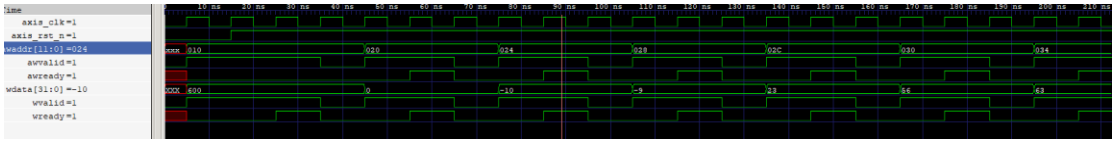
透過 stream 傳進 fifo，當要資料時 data_En 和 data_WE 皆為 HIGH 時開始將 ss_tdata 寫入 data_Di



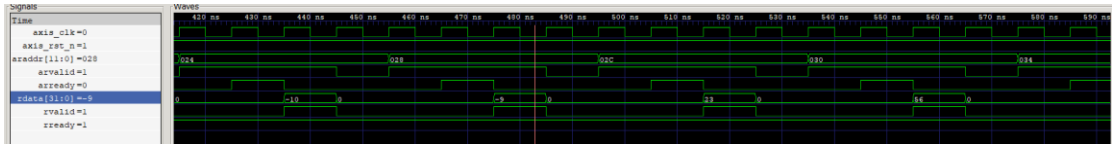
Tap:

透過 AXI4_Lite 控制 AW 為 Write request、W 為 Write data、AR 為 Read request、R 為 Read data。當 awvalid 和 awready 同時皆為 HIGH 時 address 才會開始 transfer(write request)，當 wvalid 和 wready 皆為 HIGH 時 data 才會進行 handshake(write)。同理，當 arvalid 和 arready 同時皆為 HIGH 時 address 才會開始 transfer(read request)，當 rvalid 和 rready 皆為 HIGH 時 data 才會進行 handshake(read)。

Write:



Read:



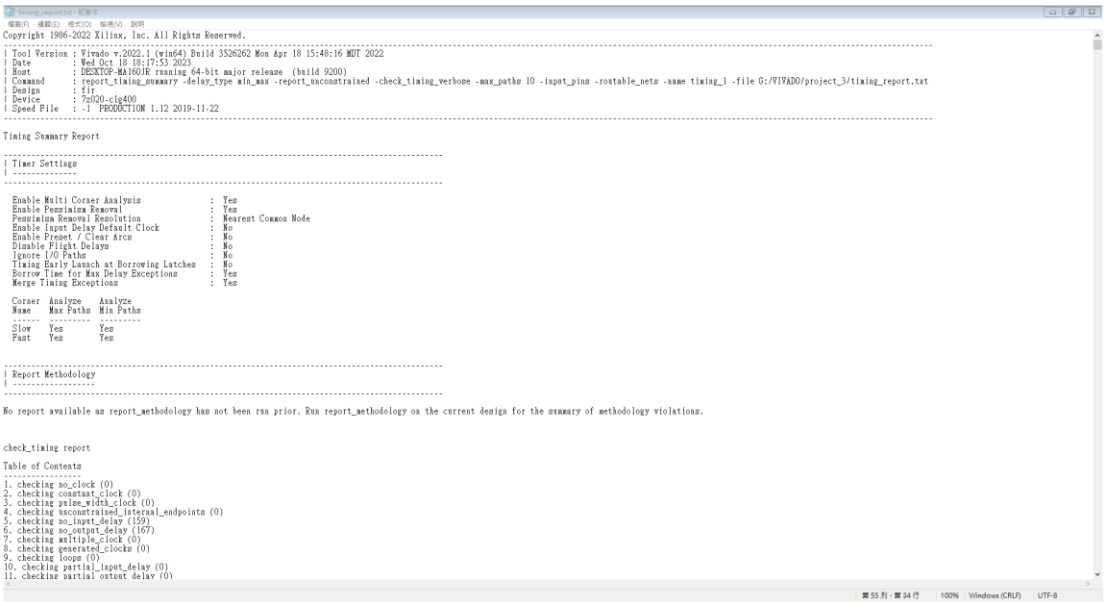
How ap_done is generated:

ap_done 這個訊號即表示做完，因此期會在 ss_tlast 和 sm_tlast 皆為 HIGH 時，ap_done 才會為 HIGH。

3.Resource

Resource	Estimation	Available	Utilization %
LUT	287	53200	0.54
FF	310	106400	0.29
DSP	3	220	1.36
IO	329	125	263.20
BUFG	1	32	3.13

4.Time report



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Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
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| Tool Version : Vivado v.2022.1 (win64) Build 3526262 Mon Apr 18 15:48:16 MDT 2022
| Date         : Wed Oct 18 18:17:53 2023
| Host         : DESKTOP-MA160JR running 64-bit major release  (build 9200)
| Command      : report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbose -max_paths 10 -input_pins -routable_nets -name timing_1 -file G:/VIVADO/project_3/timing_report.txt
| Design       : fir
| Device       : 7z020-clg400
| Speed File   : -1  PRODUCTION 1.12 2019-11-22
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Timing Summary Report

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| Timer Settings
| --------------
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  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No
  Ignore I/O Paths                           :  No
  Timing Early Launch at Borrowing Latches   :  No
  Borrow Time for Max Delay Exceptions       :  Yes
  Merge Timing Exceptions                    :  Yes

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes


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| Report Methodology
| ------------------
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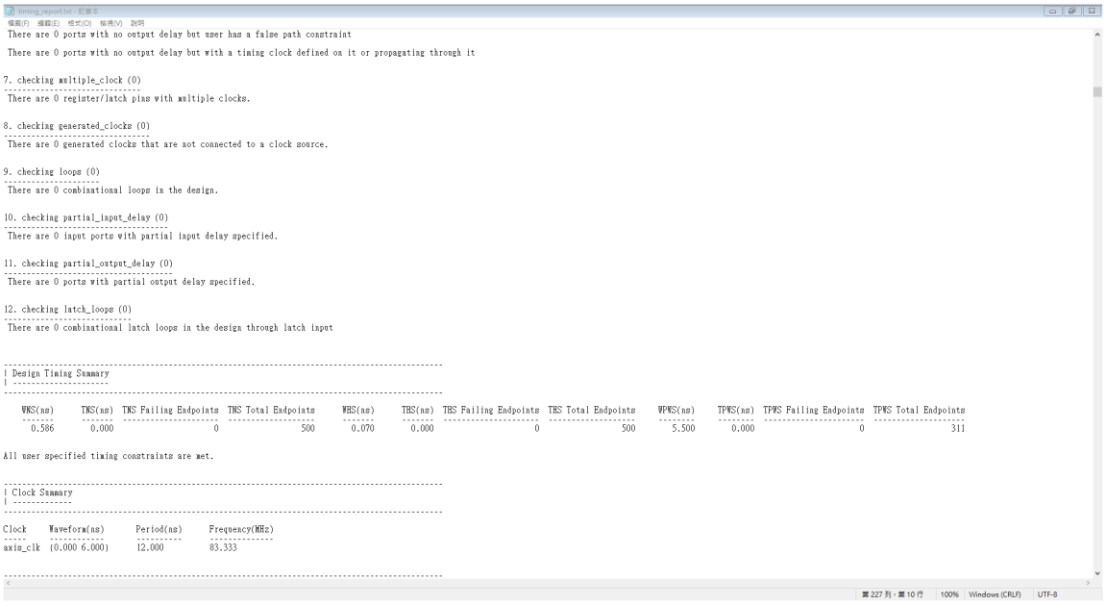
No report available as report_methodology has not been run prior. Run report_methodology on the current design for the summary of methodology violations.


check_timing report

Table of Contents
-----------------
1. checking no_clock (0)
2. checking constant_clock (0)
3. checking pulse_width_clock (0)
4. checking unconstrained_internal_endpoints (0)
5. checking no_input_delay (159)
6. checking no_output_delay (167)
7. checking multiple_clock (0)
8. checking generated_clocks (0)
9. checking loops (0)
10. checking partial_input_delay (0)
11. checking partial_output_delay (0)
```



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There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it


7. checking multiple_clock (0)
------------------------------
There are 0 register/latch pins with multiple clocks.


8. checking generated_clocks (0)
--------------------------------
There are 0 generated clocks that are not connected to a clock source.


9. checking loops (0)
---------------------
There are 0 combinational loops in the design.


10. checking partial_input_delay (0)
------------------------------------
There are 0 input ports with partial input delay specified.


11. checking partial_output_delay (0)
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There are 0 ports with partial output delay specified.


12. checking latch_loops (0)
----------------------------
There are 0 combinational latch loops in the design through latch input


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| Design Timing Summary
| ---------------------
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    WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total Endpoints      WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total Endpoints     WPWS(ns)      TPWS(ns)  TPWS Failing Endpoints  TPWS Total Endpoints
    -------      -------  ---------------------  -------------------      -------      -------  ---------------------  -------------------     --------      --------  ----------------------  --------------------
      0.586        0.000                      0                  500        0.070        0.000                      0                  500        5.500         0.000                       0                  311

All user specified timing constraints are met.

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| Clock Summary
| -------------
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Clock     Waveform(ns)       Period(ns)      Frequency(MHz)
-----     ------------       ----------      --------------
axis_clk  {0.000 6.000}      12.000          83.333

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```

```
All user specified timing constraints are met.

------------------------------------------------------------------------------------------------
| Clock Summary
| -------------
------------------------------------------------------------------------------------------------

Clock     Waveform(ns)       Period(ns)      Frequency(MHz)
-----     ------------       ----------      --------------
axis_clk  {0.000 6.000}      12.000          83.333

------------------------------------------------------------------------------------------------
| Intra Clock Table
```

tuns | Timing

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.586 ns	Worst Hold Slack (WHS):	0.070 ns	Worst Pulse Width Slack (WPWS):	5.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	500	Total Number of Endpoints:	500	Total Number of Endpoints:	311

All user specified timing constraints are met.

5.Simulation waveform