SOC Design

Lab 4-1 Execute Code in User Memory

Group no: 5

Members:

M11207415 陳謝鎧

M11207002 陳泊佑

M11107426 廖千慧

M11207328 吳奕帆

# **Prepare firmware code & RTL:**

## Generate data in header file – fir.h:

### Define taps parameters and inputsignal as lab3 in header file.

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## C code – fir.c:

### Implement FIR function in c code.

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## Firmware management in main(): (Already designed)

### In testbench/counter\_la\_fir.c, parameter reg\_mprj\_xfer will be initially to 1, and will not start fir until the external signal is given to 0.

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## Linker for address arrangement: (Already designed)

### In firmware/section.ids, mpjram is our bram, it’s original address is at 0x38000000, and it’s size is 4 KB.

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## Design BRAM in user\_project

### Estimated the required size of RAM

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### Design the controller connected with wishbone bus and ack response need to after Delay (10 delays)

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## Compilation

### Run\_clean

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### Run\_sim

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### Compilation

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# Synthesis & Verification

### Waveform – Wishbone’s ack will have a 10cycle delay when writing.

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### Timing report

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### Synthesis report

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### Timing Report

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# 心得:

#### 在Lab4-0中我們練習了Caravel SOC simulation，在Lab4-1中學習設計能夠在Caravel RISC-V core中跑的firmware code (exemem-fir)，以及在user project中整合RAM，使其能和firmware及testbench交互作用。

#### 在設計過程中的compilation時曾發生過 ”Time out, Test LA failed (RTL)”，在github上也看到有人發問同樣的問題，我參考了底下留言的建議，去檢查確實我們的Bram Module接腳是否有正確的與Wishbone連接，確實沒有，因此我們很快找出問題點並將其修正。

#### 之後在vivado中跑bram.v和user\_proj\_example.counter.v的合成驗證時也出現了error，error內容為 ” use of undefined macro ‘MPRJ\_IO\_PADS’ in user\_proj\_example.counter.v.” 以及 ” net type must be explicitly specified for ‘wb\_clk\_i’ when defult\_nettype is none.” 同樣的在github上已經有同學遇到了此問題，也有同學很熱心且詳細的在底下解答，由於MPRJ\_IO\_PADS這個參數是定義於rtl/header/defines.v裡面，但我們在合成時只使用了bram.v和user\_proj\_example.counter.v，因此我們需自行定義MPRJ\_IO\_PADS參數於user\_proj\_example.counter.v中。而第二個error是由於 ‘default nettype none造成的，因此我們將none改為wire即可順利的合成。