## Kai Henry Liu

Enschede, The Netherlands | EU and willing to relocate | <a href="mailto:kailong420@gmail.com">kailong420@gmail.com</a> | <a href="https://www.linkedin.com/in/kai77">https://www.linkedin.com/in/kai77</a>

#### **EDUCATION**

University of Twente Enschede, NL

Pre-Master, Major Embedded Systems & Computer Engineering, focus digital hardware Expected Feb 2025 Relevant Coursework: Signal processing, Digital logic & Computer organization (VHDL, Assembly ARC), Algorithms & Data structures (C++).

Hanze
Bachelor of Engineering, Major Electrical engineering; focus mechatronics

Groningen, NL Expected Aug 2025

Relevant Coursework: Networking & Communication, Digital logic/design, Analogue circuit analysis,

C programming, Python programming, Data Analysis & AI.

#### **WORK EXPERIENCE**

NXP Semiconductors Nijmegen, NL

Internship Verification & Validation digital hardware engineer (Comms based AMS ASIC SOC) (6m) Mar 2024 – Aug 2024

- Ownership of 3 testcases for verification with SystemVerilog in an UVM environment, introducing jitter for a low speed ethernet BUS, and proving the testcases their usefulness by using statistical fit and regression, as part of digital controller functional coverage.
- Data pipeline architecture and setup for new verification environment wherein the test boards are also included within the simulation, securing a solid base for AI model integration for further automated verification.
- Finding potential bugs in the ASIC design and the Synopsis Verification IP, proven with testcases and using waveforms in Cadence Xcelium.
- Created an algorithm in SystemVerilog for proving certain out of spec behavior and verified the algorithms correctness with Verilog assertions.

#### **UNIVERSITY & PERSONAL PROJECTS**

#### ALGORITHM PROGRAM DESIGN

(current)

• University project, currently working on an approximation algorithm for a special case of the dominating set vertex cover problem in C++. Which is NP hard.

#### RISC-V PROCESSOR ON FPGA

(1m)

- A reduced instruction set processor, built from the ground up, making every component like the ALU and carry lookahead adders with the HDL Verilog.
- Digital timing analysis, synthesis, Using FPGAS, with intel Quartus.

#### TEM CELL FOR EMC TESTING

(3m)

In collaboration with Astron the Dutch institute for radio astronomy

- Research on structures of TEM cells for reducing EMI while maintaining reasonable impedance characteristics by way of introducing selective slot antennas for passive frequency cancellation.
- Physical creation and testing of the actual concept using oscilloscopes & spectrum analyzers.

#### AI WEATHER PREDICTIONS

(3m)

- Gathering data from weather stations and live data using sensors, to predict rainfall.
- Did from start to finish: data collection and analysis, data wrangling, training, comparison of AI models, AI model selection, Hyper parameter finetuning. and do inference on the edge device.

### RESPITORY DEVICE FOR BABIES

(3m)

- Was a team lead for this biomedical university project in collaboration with the local academic hospital.
- The positive pressure respiratory devices currently can cause lung damage if not properly managed, instead we designed a negative pressure device concept. I did all the C programming, and system logic design.

#### SMART SYSTEMS VOICE CONTROLLER

(3m)

• Using a voice control app, programming the back end in python for AWS integration, includes AWS services; Alexa, lambda, IOT core and AWS management services. The end product lets you send signals remotely with your voice to turn multiple lights on and off, through a microcontroller connected with the web.

# ADDITIONAL

**Technical Skills**: working in Linux, C/C++(OOP) programming, Python programming, SystemVerilog(HDL) **Languages**: Native in Dutch, English and a Dutch national.