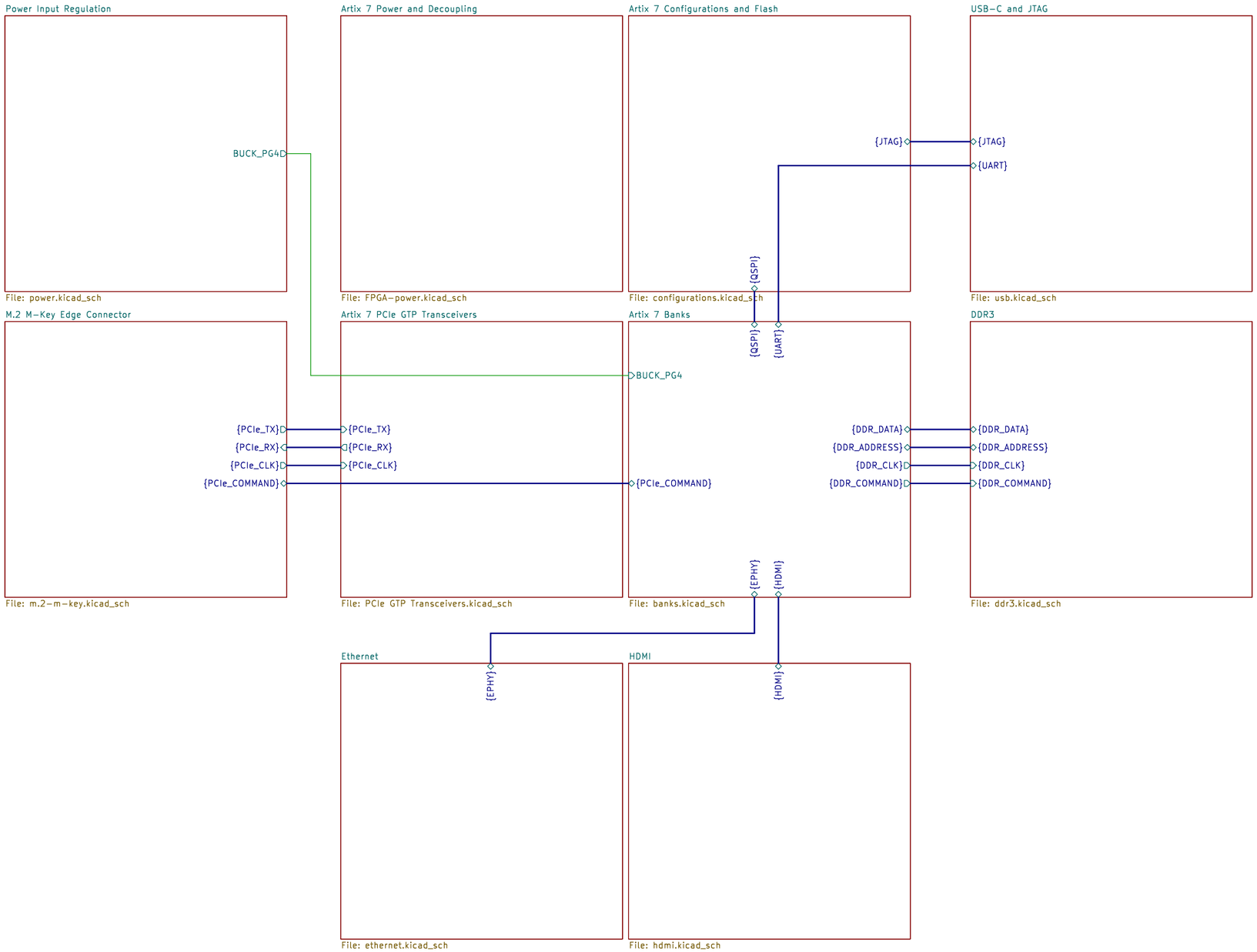


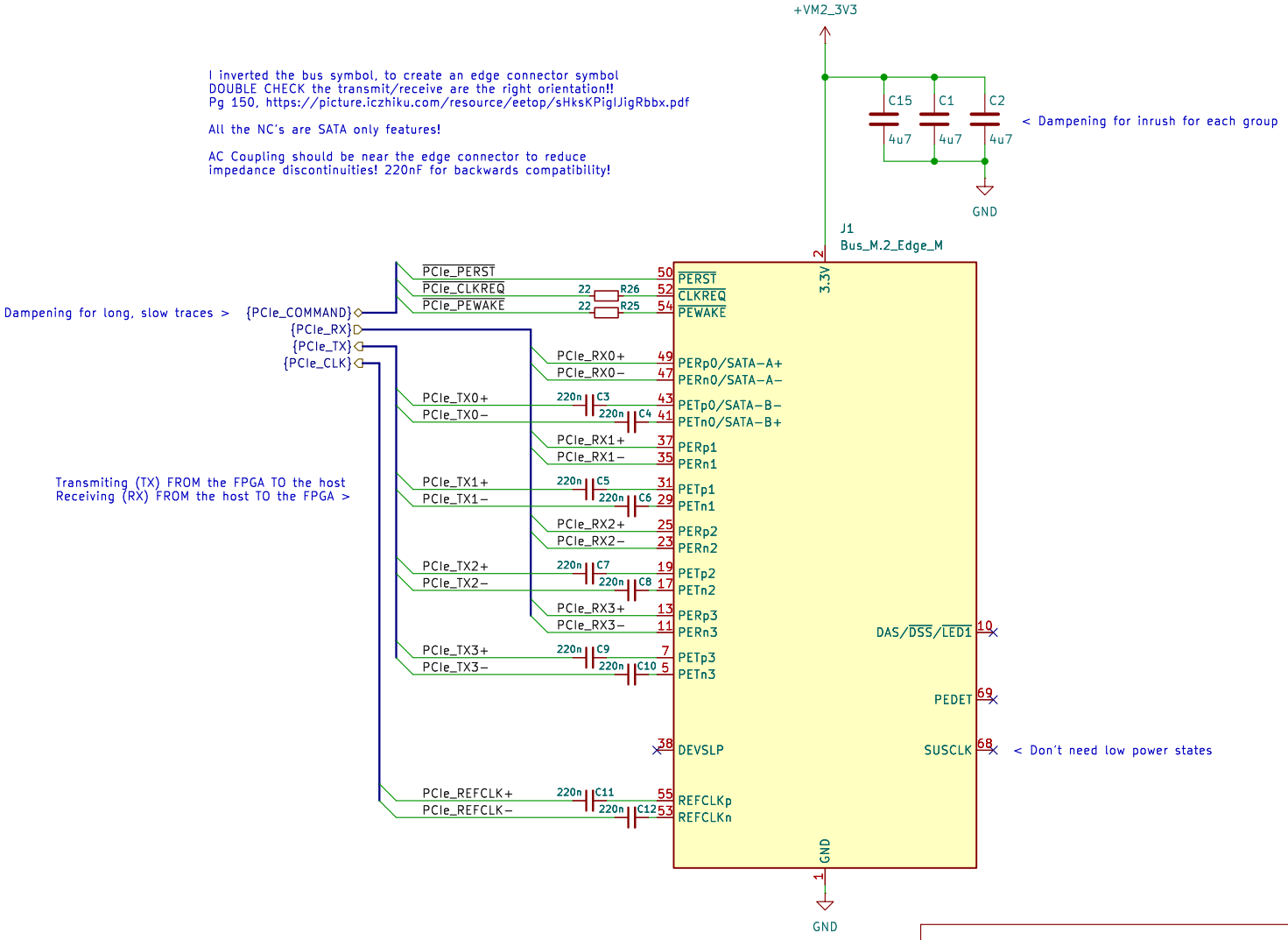
https://github.com/KaiPereira/M.2-FPGA-Accelerator

Kai Pereira

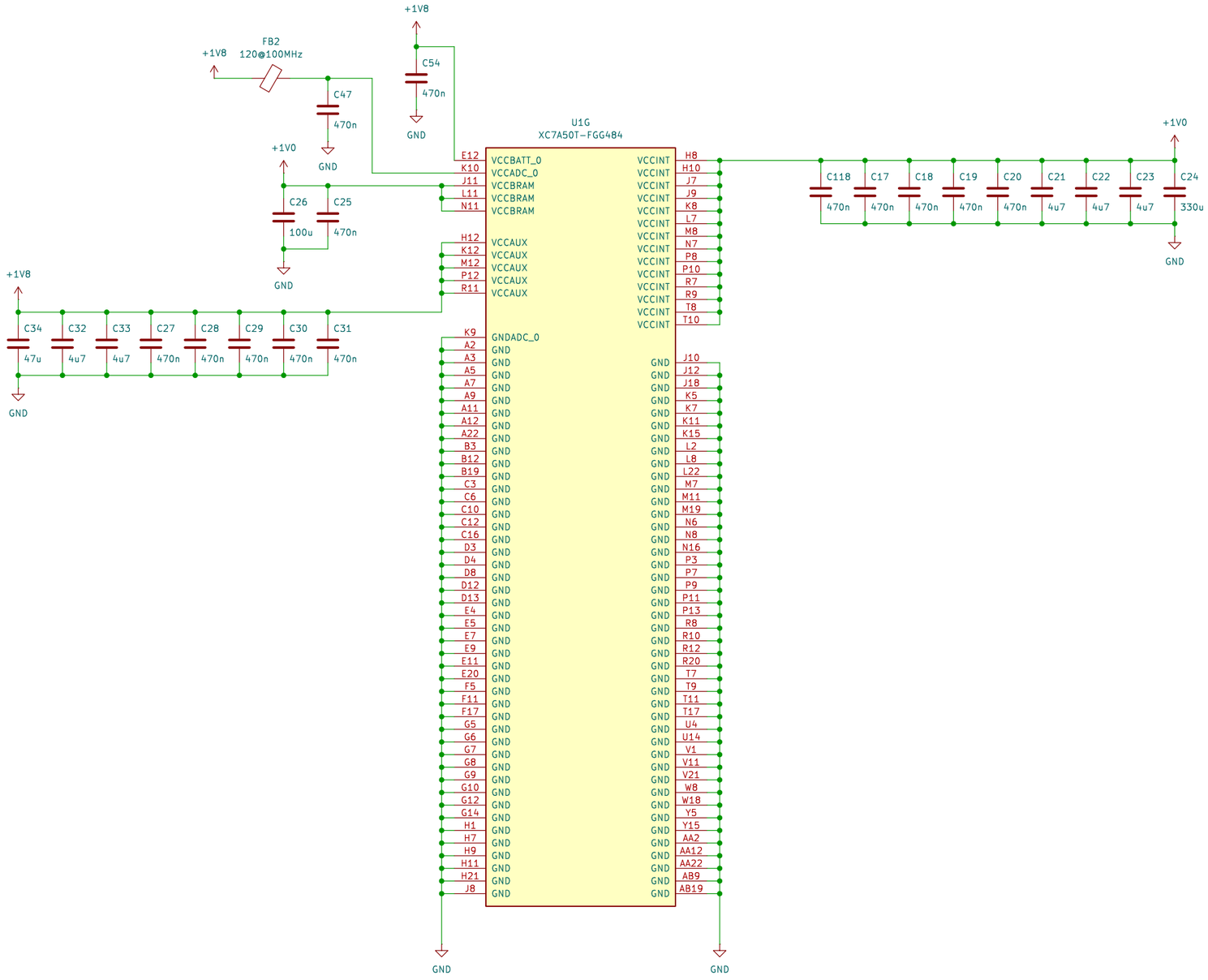
Sheet: /
File: PCB.kicad_sch

Title: M.2 FPGA Hardware Accelerator Devboard

Size: A3	Date:	**Rev: v1.0**
KiCad E.D.A. 9.0.6		Id: 1/11


I inverted the bus symbol, to create an edge connector symbol
DOUBLE CHECK the transmit/receive are the right orientation!!
Pg 150, https://picture.iczhiku.com/resource/eetop/sHksKPigIJigRbbx.pdf
All the NC's are SATA only features!
AC Coupling should be near the edge connector to reduce
impedance discontinuities! 220nF for backwards compatibility!
+VM2_3V3
C15
C1
C2
4u7
4u7
4u7
< Dampening for inrush for each group
GND
J1
Bus_M.2_Edge_M
Dampening for long, slow traces >
{PCIe_COMMAND}
{PCIe_RX}
{PCIe_TX}
{PCIe_CLK}
PCIe_PERST
PCIe_CLKREQ
PCIe_PEWAKE
22
R26
22
R25
50
52
54
PERST
CLKREQ
PEWAKE
2
3.3V
PCIe_RX0+
PCIe_RX0−
49
47
PERp0/SATA−A+
PERn0/SATA−A−
PCIe_TX0+
PCIe_TX0−
220n
C3
220n
C4
43
41
PETp0/SATA−B−
PETn0/SATA−B+
PCIe_RX1+
PCIe_RX1−
37
35
PERp1
PERn1
Transmiting (TX) FROM the FPGA TO the host
Receiving (RX) FROM the host TO the FPGA >
PCIe_TX1+
PCIe_TX1−
220n
C5
220n
C6
31
29
PETp1
PETn1
PCIe_RX2+
PCIe_RX2−
25
23
PERp2
PERn2
PCIe_TX2+
PCIe_TX2−
220n
C7
220n
C8
19
17
PETp2
PETn2
PCIe_RX3+
PCIe_RX3−
13
11
PERp3
PERn3
DAS/DSS/LED1
10
PCIe_TX3+
PCIe_TX3−
220n
C9
220n
C10
7
5
PETp3
PETn3
PEDET
69
38
DEVSLP
SUSCLK
68
< Don't need low power states
PCIe_REFCLK+
PCIe_REFCLK−
220n
C11
220n
C12
55
53
REFCLKp
REFCLKn
1
GND
GND
Sheet: /M.2 M−Key Edge Connector/
File: m.2−m−key.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 9.0.6
Id: 2/11

Simulate beads in LTSpice!



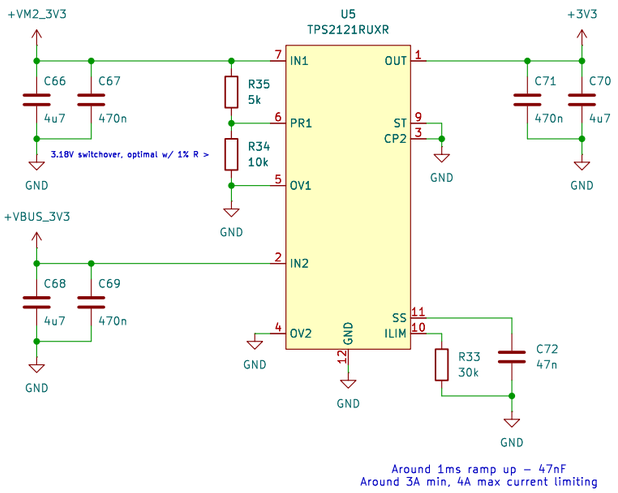
Sheet: /Artix 7 Power and Decoupling/		
File: FPGA-power.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 3/11

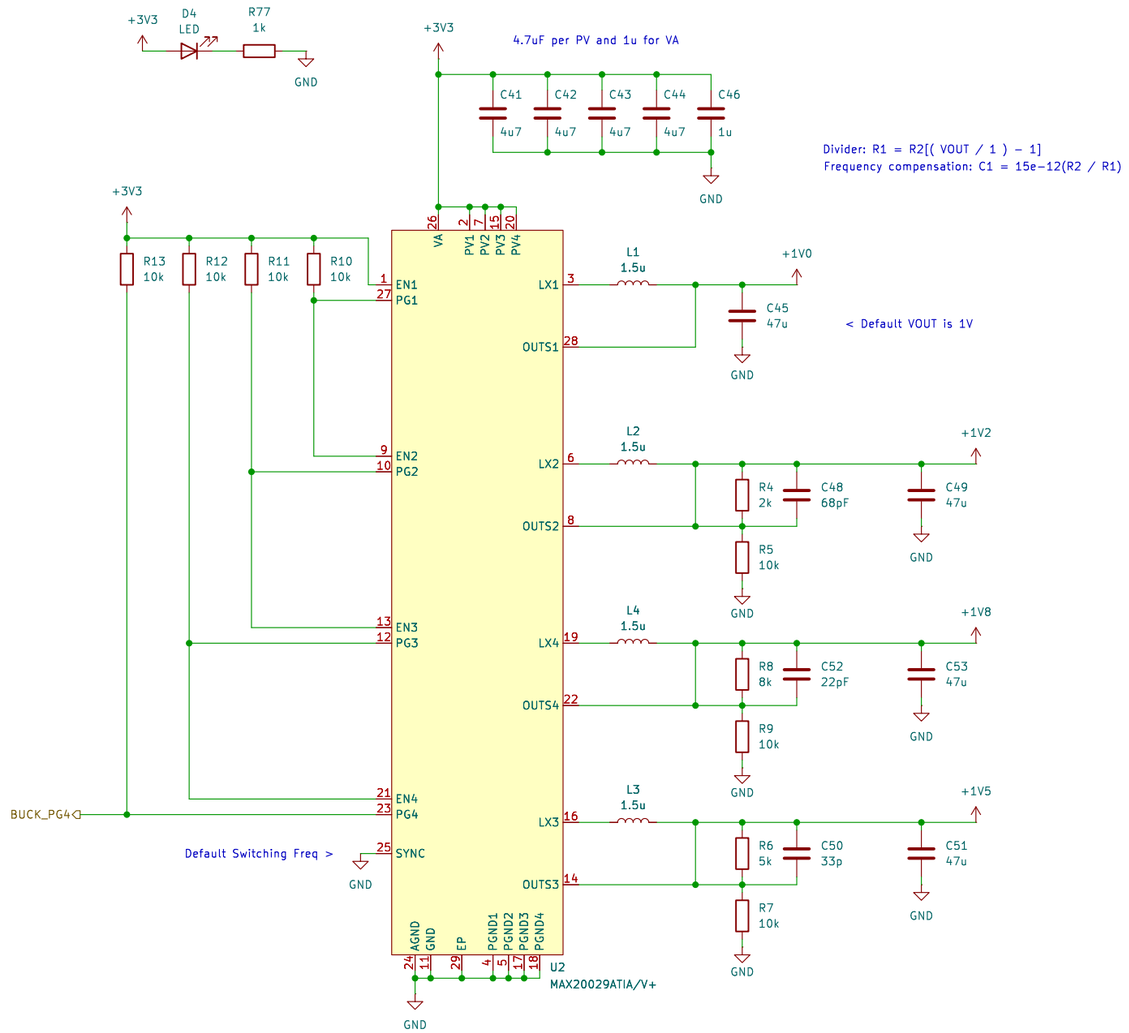
SEQUENCE VCC -> 1V0 -> 1V2 -> 1V8 -> 1V5

+VM2_3V3 is the M.2 3.3V power source
+VBUS_3V3 is the USB power source, bucked down

This circuit ensures that USB doesn't backfeed into the M.2 connector,
frying the motherboard, and also prioritizes reliable
M.2 connector power if both are plugged in!

Switchover is at 3.18V using PR1 voltage divider which is really optimal with
1% resistors because m.2 connector minimum voltage is 3.135V



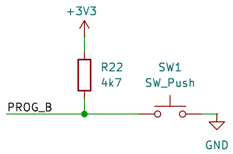


Sheet: /Power Input Regulation/
File: power.kicad_sch

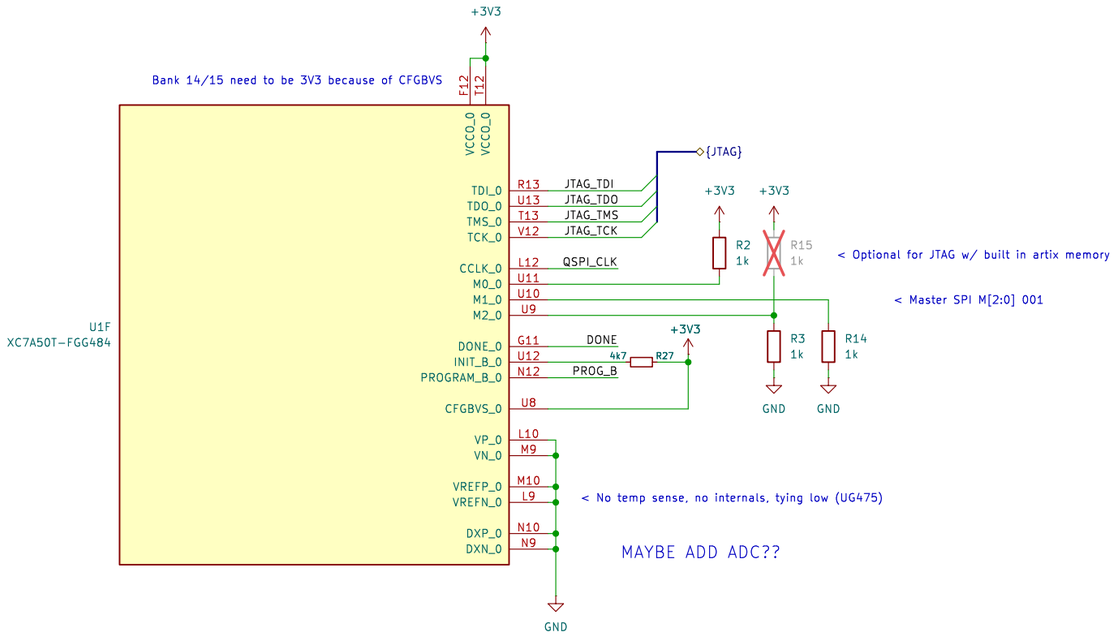
Title:

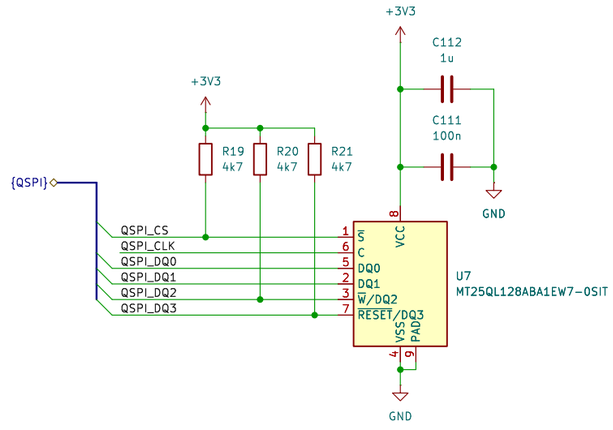
Size: A3 | Date: | **Rev:**
KiCad E.D.A. 9.0.6 | Id: 4/11

< DONE sinks current, LED turns off when done



< Manual configuration reset, it's a devboard so why not





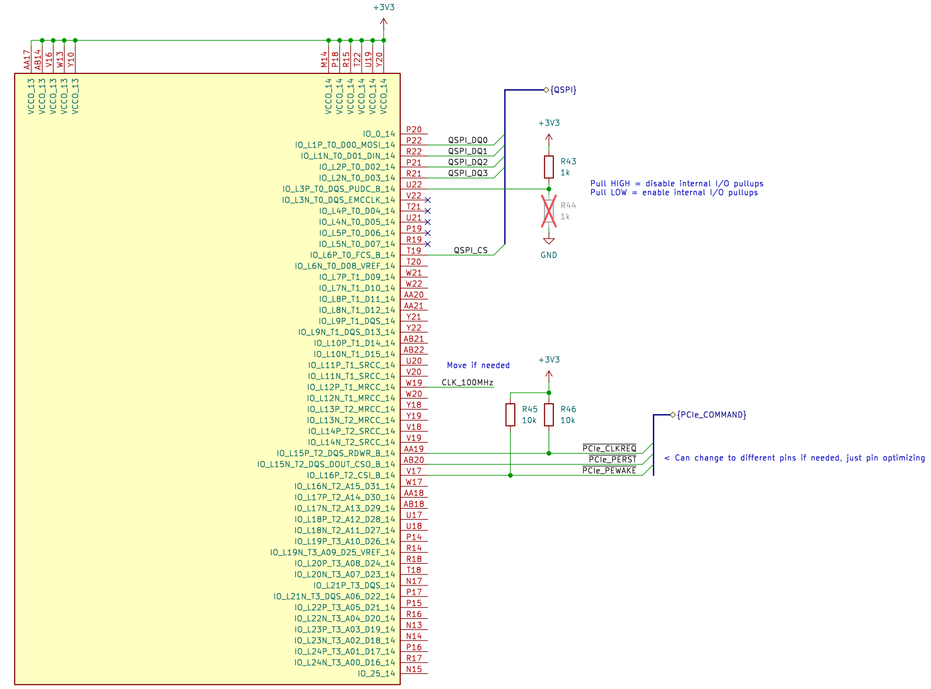
Sheet: /Artix 7 Configurations and Flash/
File: configurations.kicad_sch

Title:

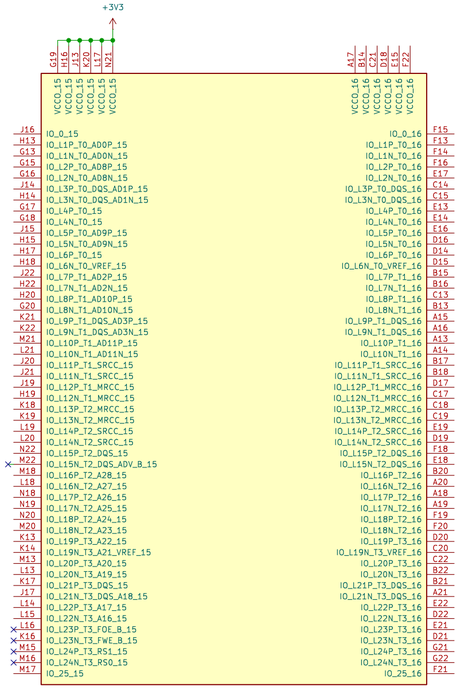
Size: A3 | Date: | **Rev:**

KiCad E.D.A. 9.0.6 | Id: 5/11

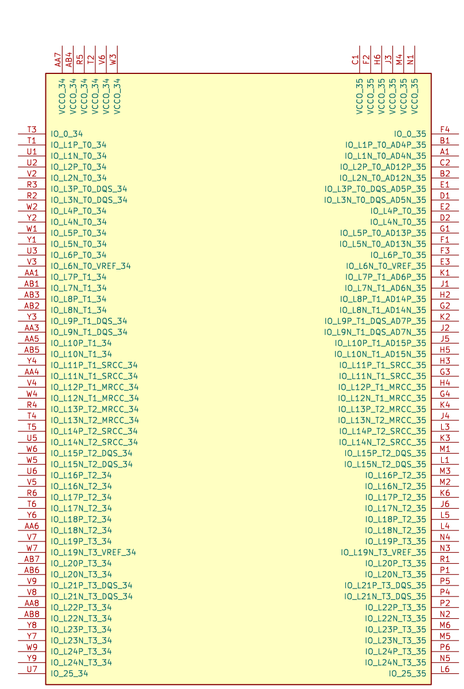
Most of the NC's are usable as I/O's too,
even if they're configurations ;)



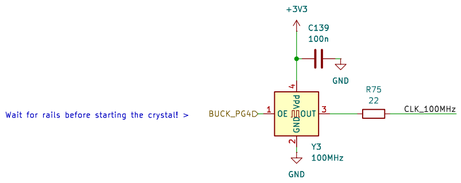
U1A
XC7A50T-FGG484



U1B
XC7A50T-FGG484



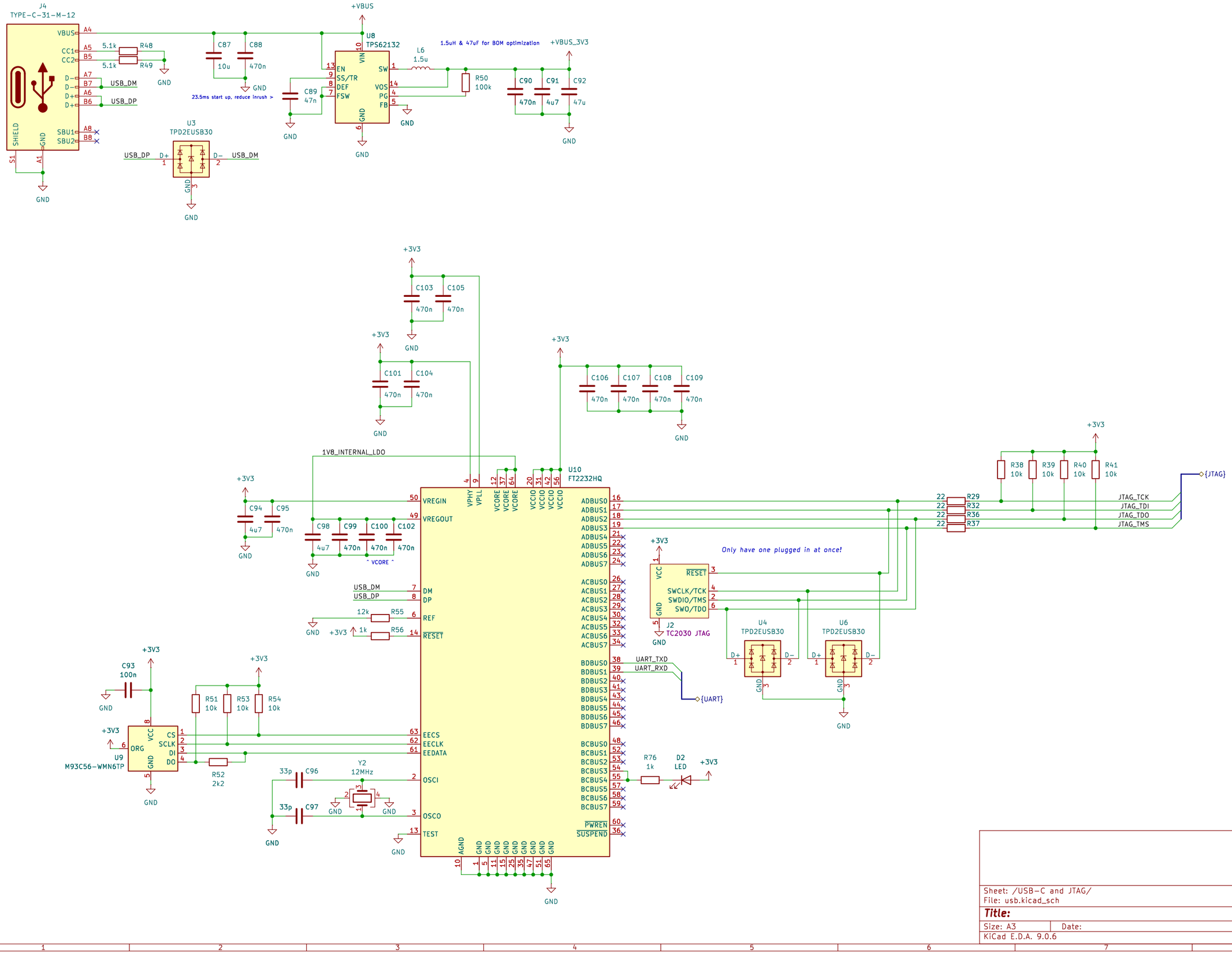
U1C
XC7A50T-FGG484



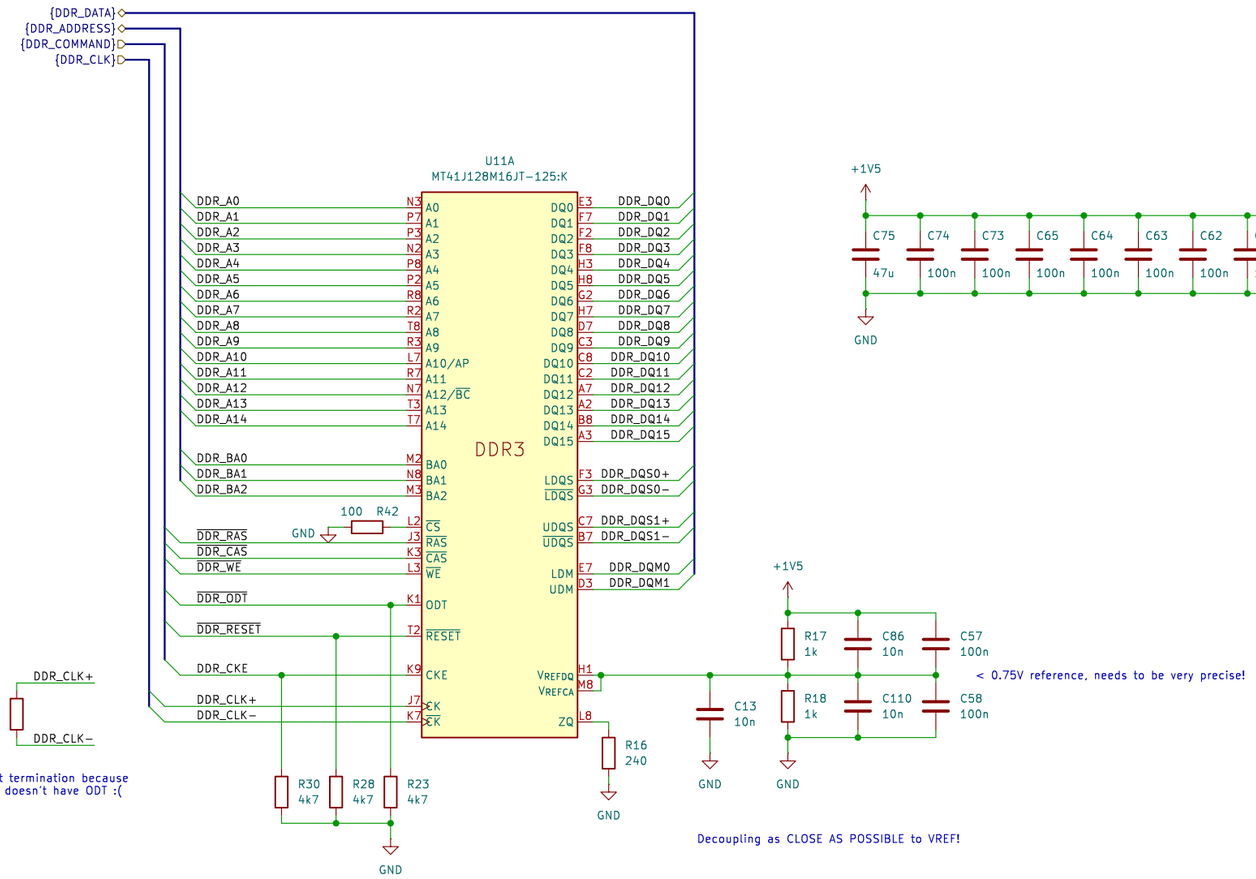
Sheet: /Artix 7 Banks/
File: banks.kicad_sch

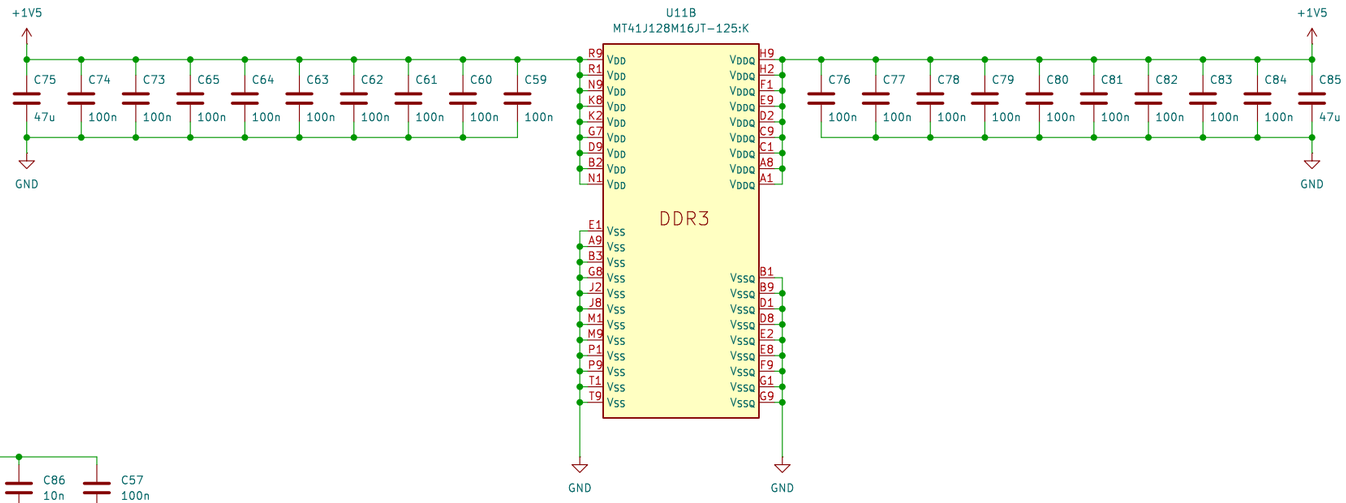
Title:

Size: A2	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 6/11


J4
TYPE-C-31-M-12
VBUS
CC1
CC2
D-
D-
D+
D+
SHIELD
GND
SBU1
SBU2
S1
A1
A4
A5
B5
A7
B7
A6
B6
A8
B8
5.1k
R48
5.1k
R49
USB_DM
USB_DP
GND
C87
10u
C88
470n
GND
23.5ms start up, reduce inrush >
+VBUS
U8
TPS62132
VIN
EN
SS/TR
DEF
FSW
SW
VOS
PG
FB
GND
C89
47n
L6
1.5u
1.5uH & 47uF for BOM optimization
+VBUS_3V3
R50
100k
C90
470n
C91
4u7
C92
47u
GND
U3
TPD2EUSB30
USB_DP
D+
1
D-
2
USB_DM
GND
3
GND
+3V3
C103
470n
C105
470n
GND
C101
470n
C104
470n
GND
C106
470n
C107
470n
C108
470n
C109
470n
GND
1V8_INTERNAL_LDO
U10
FT2232HQ
VPHY
VPLL
VCORE
VCORE
VCORE
VCCIO
VCCIO
VCCIO
VCCIO
VREGIN
VREGOUT
C94
4u7
C95
470n
C98
4u7
C99
470n
C100
470n
C102
470n
^ VCORE ^
DM
DP
REF
RESET
USB_DM
USB_DP
12k
R55
1k
R56
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
UART_TXD
UART_RXD
{UART}
R29
R32
R36
R37
22
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
{JTAG}
R38
10k
R39
10k
R40
10k
R41
10k
Only have one plugged in at once!
J2
TC2030 JTAG
VCC
RESET
SWCLK/TCK
SWDIO/TMS
SWO/TDO
GND
U4
TPD2EUSB30
U6
TPD2EUSB30
C93
100n
U9
M93C56-WMN6TP
ORG
VCC
CS
SCLK
DI
DO
GND
R51
10k
R53
10k
R54
10k
R52
2k2
EECS
EECLK
EEDATA
Y2
12MHz
33p
C96
33p
C97
OSCI
OSCO
TEST
R76
1k
D2
LED
AGND
GND
Sheet: /USB-C and JTAG/
File: usb.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. 9.0.6
Id: 7/11

MT41J128M16JT-125:K
16 Bit data width
8 Bank machines
Normal ordering

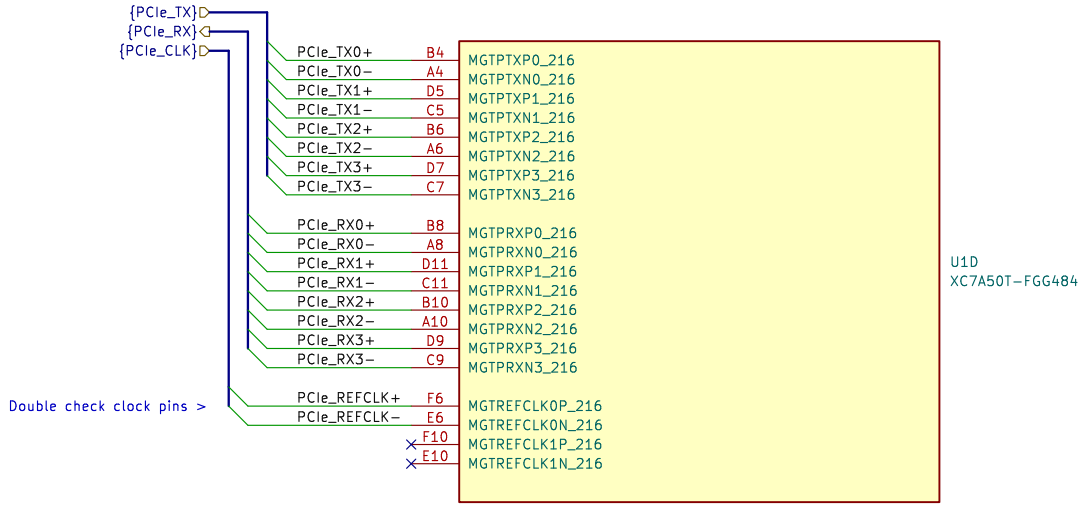




Sheet: /DDR3/
File: ddr3.kicad_sch

Title:

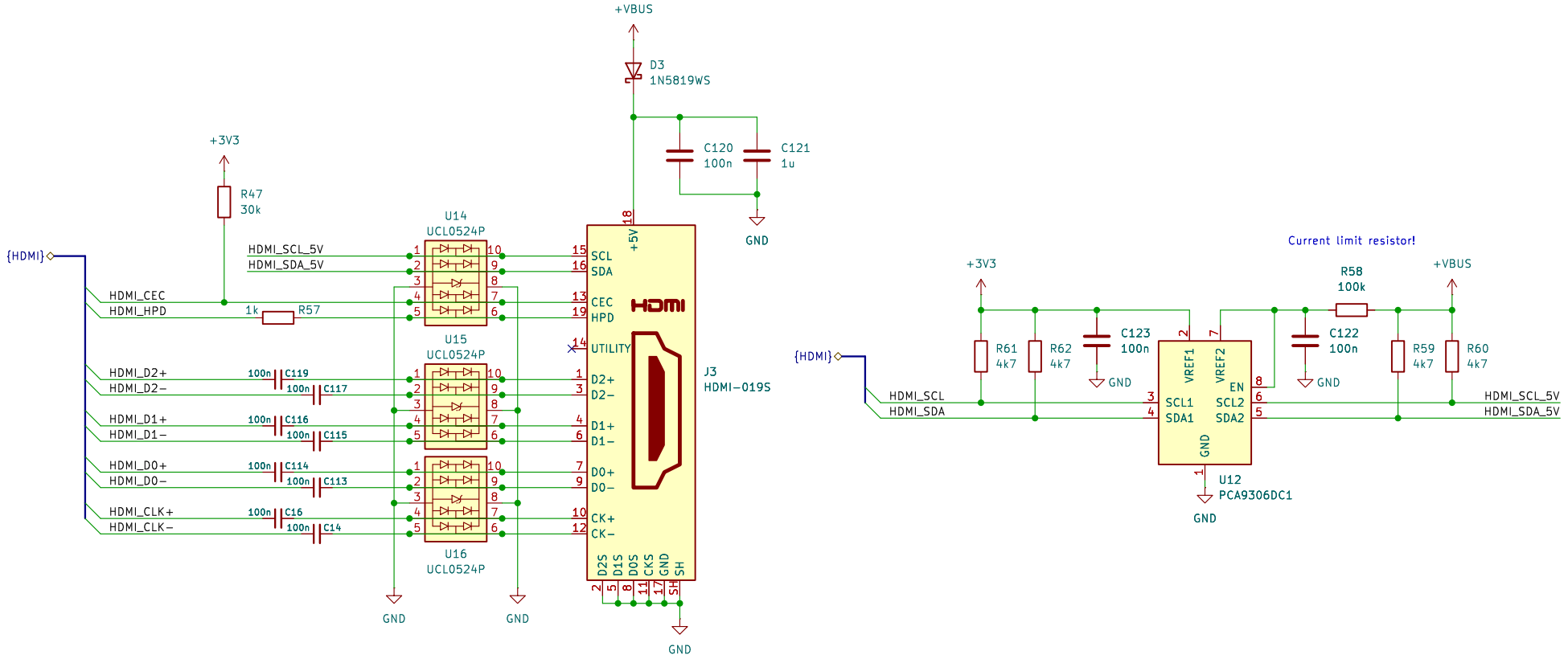
Size: A3	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 8/11



Sheet: /Artix 7 PCIe GTP Transceivers/
File: PCIe GTP Transceivers.kicad_sch

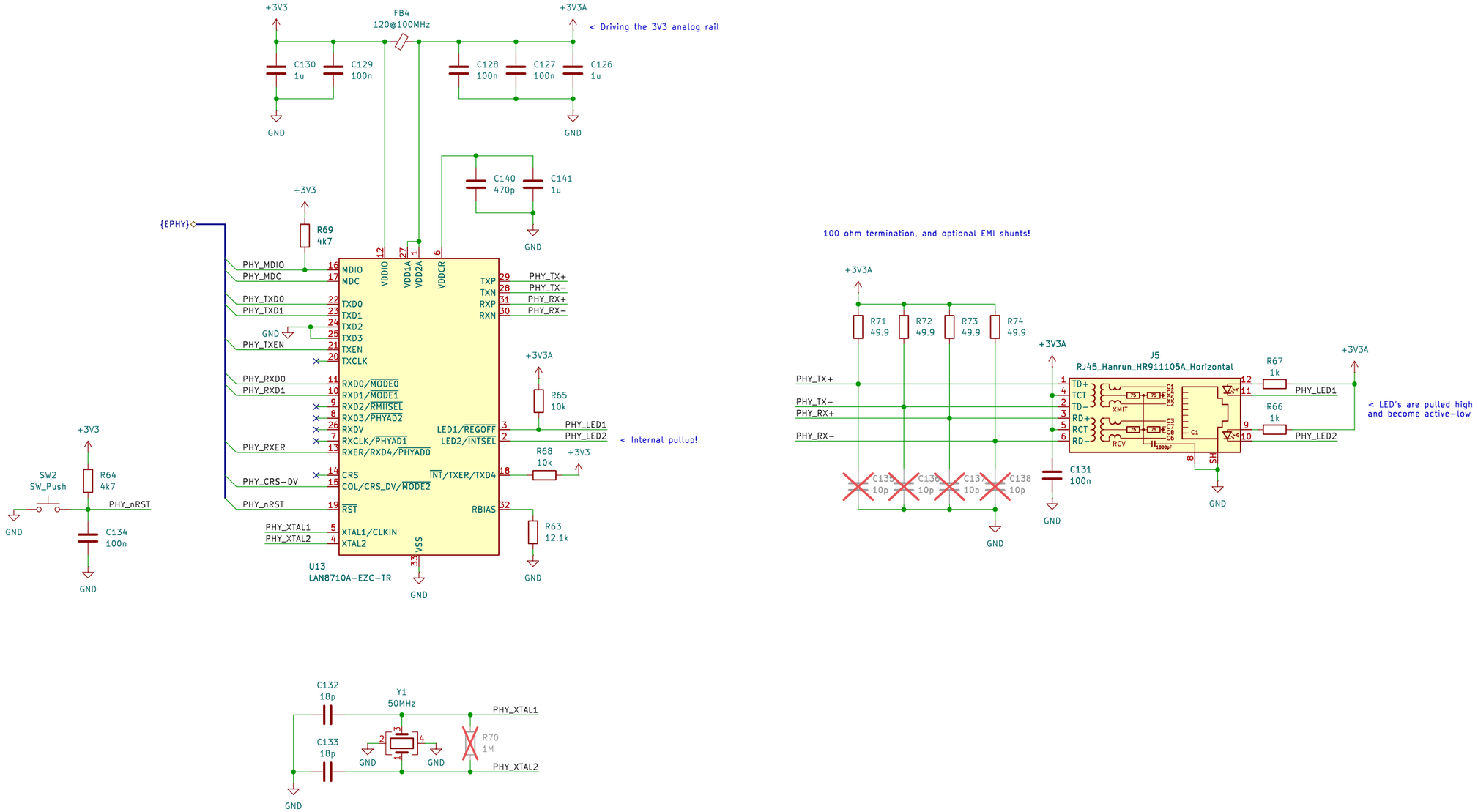
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 9/11



Sheet: /HDMI/		
File: hdmi.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 10/11

100 Mbps, RMII Ethernet!



Sheet: /Ethernet/	
File: ethernet.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. 9.0.6	Id: 11/11
	Rev: