The Role of Relative Capacitances in Impedance Sensing with Organic Electrochemical Transistors

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The role of relative capacitances in impedance sensing with organic electrochemical transistors

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Abstract

The organic electrochemical transistor (OECT) has attracted interest for use in biosensor technology due to its ability to transduce ionic to electronic signals and operate in aqueous environments. While OECTs have been broadly applied for detection and quantification of chemical analytes as well as impedance characterization of biological systems, there is still no general consensus on the ideal geometries, relative capacitances, and operational conditions for specific sensing scenarios. Here we show that for impedance sensing with a capacitive layer added to the gate (*e.g.*, a lipid bilayer), gate-limited OECTs produce the largest sensor response. We used an equivalent circuit model to study the OECT frequency response with non-permeable and ion-permeable membranes added to the gate and found that the transistor configuration, with respect to gate and channel capacitances, able to produce the largest sensor signal is determined by the capacitance to be sensed as well as the permeability of the membrane. The findings from the model were applied to design a gold gate OECT capable of detecting the formation of a supported lipid bilayer on the gate. Our results indicate that the high transconductance OECTs typically considered attractive do not deliver the largest sensor signals when used for impedance sensing. By presenting our results in settings similar to those used in practical experiments we hope that experimental scientists can find guidance on how to best design OECTs for impedance biosensing applications. The demonstration of a gold gate OECT functionalized with a lipid bilayer can act as inspiration for future implementations of tethered lipid bilayers in combination with OECTs.

Introduction

The organic electrochemical transistor (OECT)[1,2] is able to bridge the ionic-electronic signaling gap and therefore holds great potential for use in biosensor applications[3,4]. The OECT comprises a mixed ion-electron conductor channel where an electronic current flows between the source and drain electrodes. Since the channel material typically is an amorphous or nanocrystalline bulk, it is possible to make flexible and highly elastic devices amenable for use in wearable and soft electronics applications.[5–7] The bulk doping level, and thereby the electronic conductivity within the channel, is modulated by the exchange of ions supplied by the electrolyte, which is determined by the potential of the gate electrode. Since the (de-)doping process in the OECT channel utilizes ions from the surrounding electrolyte, the OECT is well suited for operation in aqueous environments such as cell cultures or in the liquid environments surrounding biomedical implants.[8–11] Several OECT sensing modes have been explored, such as enzymatic, direct faradaic reactions, or via mediators to name a few, allowing them to be used for detection of chemical analytes or recording of electrical activity in the brain.[3,4,12–15] When operating the OECT as a sensor, the current flowing through the channel – and defining the primary sensor signal – is modulated by changes in electrochemical potential of the solution. In faradaic configurations, redox sensing reactions at the gate-electrolyte interface (or channel-electrolyte interface) elicit ionic fluxes into or out of the channel, and thereby modulate the sensor signal. In non-faradaic, or "capacitive", sensing configurations[3,16–19], the OECT essentially comprises two double-layer capacitances, residing at the gate-electrolyte and channel-electrolyte interfaces, that incorporate the operating sensor mechanism and the analytes. The importance of the details and fundamental properties of these capacitances is therefore essential for understanding and further optimizing OECTs for sensor applications.[20]

In an attempt to better understand the capacitive mode of operation of OECT sensors, here, we study the addition of a capacitive layer between the channel and gate which alters the gating

efficacy of the transistor. Similar impedance sensing modes have been used to study the integrity of tight junction cell layers and black lipid membranes, as well as for the characterization of supported lipid bilayer (SLB) formed on the OECT channel.[16,21–24] The device geometry influences the transistor performance mainly through the transconductance, g_m.[25,26] The transconductance is an important figure-of-merit for the OECT, in general and for sensing in particular, since it describes the current modulation versus the applied gate potential ($g_m = \partial I_D / \partial V_G$) and thereby determines the amplification that the transistor can deliver. The altered gating efficacy in capacitive sensing effectively lowers or increases the transconductance, depending on the nature of the capacitance change.[27] Furthermore, the relative sizes and capacitances of the gate and channel have been shown to have optimal – and opposing – configurations depending on electrochemical or capacitive sensing applications.[28] Here, we have investigated in more detail how the channel and gate capacitances, governed by device geometry, together influence the OECT's capacitive sensing capabilities. We consider purely capacitive sensing where no ion leakage occurs as well as the addition of ion-permeable membranes. Many of the previously reported studies of ion-permeable barriers have placed the barrier on the transistor channel or in the electrolyte between gate and channel.[16,23,27,29] We have instead chosen to demonstrate a sensing mechanism with a supported lipid bilayer (*i.e.*, the sensing element) formed on the gate. Adding the capacitive/sensing layer on the gate – rather than on top of the channel – is perhaps not the most common approach, but we believe it is potentially a more versatile method to develop OECT-based sensors. While the OECT channel needs to be an organic semiconductor, there are more material options for the gate, and thus more functionalization options are available. By using a gold gate OECT we pave the way for sensors incorporating thiol-tethered SLBs, a well-studied system with many demonstrations of membrane protein reconstitution.[30]

Results and discussion

Transistor and sensor model

To model the effect of the gate capacitance and the impact of sensing reactions/polarizations on the output of OECTs, we draw inspiration from the Bernards model.[31] The core element of that model, here utilized in our work, is the idea that the doping level in the channel, and thereby the modulated current flowing between source and drain, is dependent on the ionic charge injected into the channel from the electrolyte. The channel can be interpreted as a capacitor connected to a variable resistor[4], as illustrated in Figure 1a. The charge accumulated in the capacitor determines the resistor value. The transistor drain current flows through this variable resistor and the resistor thus represents an equivalent circuit for the source-drain charge current pathway. The Bernards model also comprises an ionic circuit describing the dynamic operation of the transistor. The main elements in this ionic circuit are the channel capacitor and an internal resistance, R_i, describing both ion transport in the electrolyte phase and the resistance for holes escaping the channel in the de-doping process. The potential drop over a capacitor determines its charge by,

$$Q = CV \tag{1}$$

where Q is the charge accumulated on the capacitor and V is the potential drop over it. As the charge on the channel capacitor regulates the de-doping and thus the drain current, the potential drop over the channel capacitor is identified as the key parameter for the de-doping process of the channel. This approach is similar to the one applied by Faria *et al.* for evaluating OECTs as impedance biosensors.[27]

Considering an OECT in which no potential drop occurs at the gate-electrolyte interface, the potential applied between gate and channel is divided between C_{ch} and R_i (Figure 1b). Such a transistor can be realized by using a nonpolarizable gate. The simplest deviation from this ideal transistor case is the addition of a gate capacitor, representing either a conducting polymer or a polarizable metal gate, or even a capacitive layer added between gate and channel, such as a layer

of cells residing on top of the channel (Figure 1c). With the gate capacitor included, the fractional potential drop, U_{ch}, over the channel capacitor is described by,

$$U_{ch} = \frac{1}{j\omega C_{ch}} \bigg/ \left(\frac{1}{j\omega C_g} + \frac{1}{j\omega C_{ch}} + R_i \right)$$

(2)

where ω is the angular frequency of the applied gate signal and C_g the intrinsic gate capacitance (*i.e.*, based on materials and geometry). In sensing situations where a capacitive layer is added to the gate, thus lowering the gate capacitance, the resulting effective gate capacitance will be referred to as $C_{g,s}$ (for "gate, sensing"). The change in fractional potential drop caused by the transition from C_g to $C_{g,s}$ affects the de-doping level in the transistor channel for a specific applied gate potential, and thereby impacts the drain current.
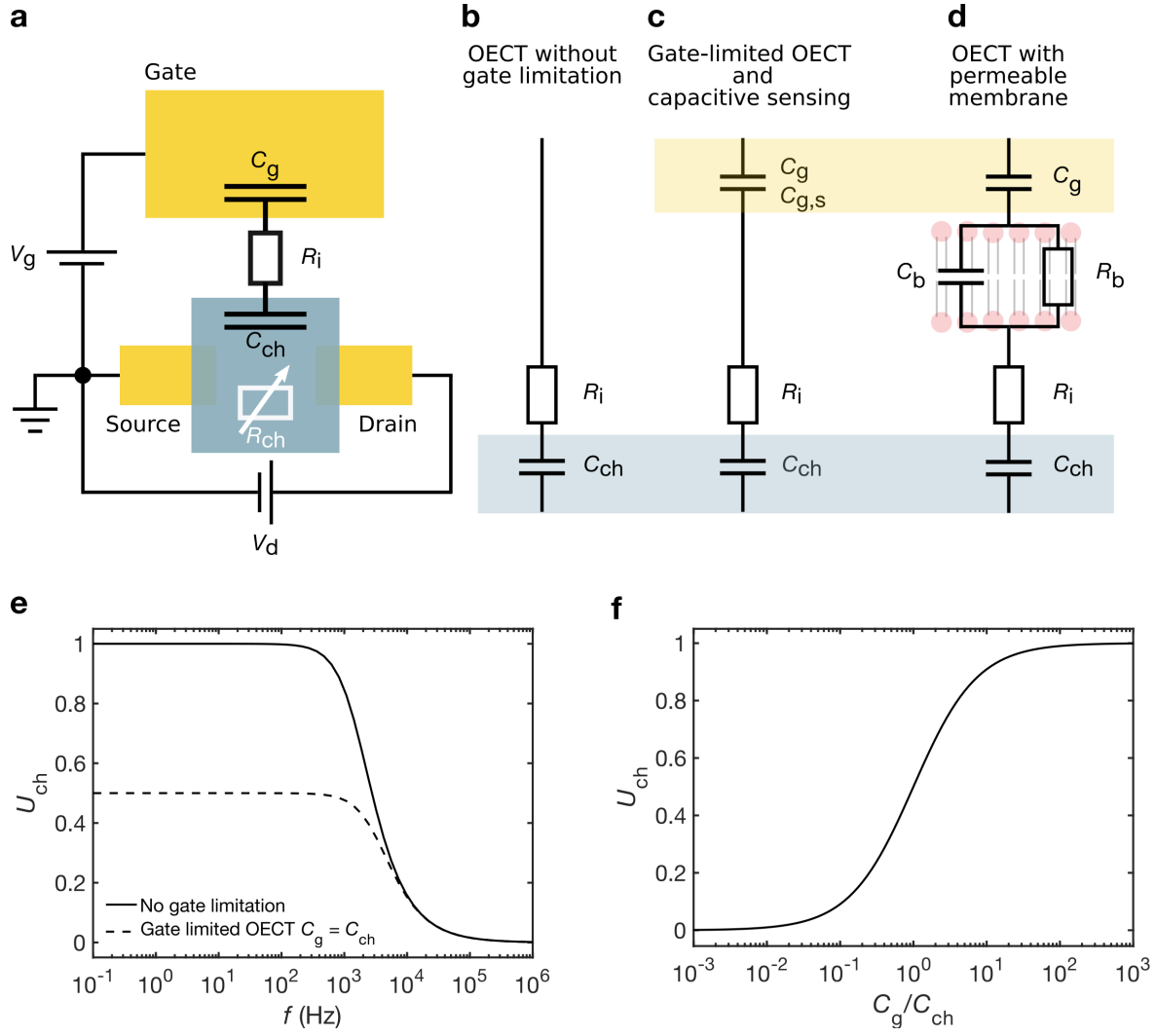
Figure 1. a) Top view schematic of gold gate OECT with ionic (black) and electronic (white) circuit elements. b-d) Equivalent circuits representing the ionic circuits used in the modelling of OECT sensing. e) Potential drop over channel capacitor versus frequency with (dashed) and without (solid) capacitive limitation at the gate. f) Steady-state potential drop over channel capacitor versus gate-to-channel capacitance ratio.

Some capacitive layers include leaky defects through which ions can penetrate, thus causing ions to drift from the electrolyte to the gate electrode. To model this transport, we add a two-part circuit element to the sensing circuit (Figure 1d). One common manifestation of such an ion-permeable layer is a supported lipid bilayer (SLB), which has been used in combination with OECTs.[23,24] To capture the transistor response with an SLB formed along the gate, we used a common SLB equivalent circuit comprising a capacitor, C_b (for "bilayer"), in parallel with a

resistor, R_b, connected in series with the gate capacitor.[32,33] With the bilayer present, the fractional potential drop over the channel capacitor becomes,

$$U_{ch} = \frac{1}{j\omega C_{ch}} \bigg/ \left(\frac{1}{j\omega C_g} + \frac{1}{j\omega C_b + 1/R_b} + R_i + \frac{1}{j\omega C_{ch}} \right) \quad (3)$$

OECTs with and without capacitive limitation at the gate

In Figure 1e the relative potential drop across the channel capacitor, U_{ch}, for an OECT with and without gate limitation is shown. The fraction of the gate potential that drops over the channel capacitor is frequency dependent. In the case of an OECT without gate limitation, at the lower end of the frequency scale, all applied potential drops across the channel capacitor. At high frequencies, the capacitor is effectively shorted ($U_{ch} \rightarrow 0$) and the applied potential drops instead across the series resistor, R_i. With no potential drop over the channel capacitor at high frequencies, the doping level in the channel will thus not be modulated, rendering the drain current unresponsive to the signal applied to the gate. The frequency response of the transistor is determined by C_{ch} and R_i together. For these calculations, we chose a channel capacitance $C_{ch} = 100$ nF and an internal resistance $R_i = 1000\ \Omega$, keeping within the same orders of magnitude as previously reported.[25,34] For transistors with other values for C_{ch} and R_i, the frequency responses are expected to differ from what is presented in Figure 1e, but the low- and high-frequency limiting cases of U_{ch} will hold.

If a capacitor, C_g, is included at the gate, the total potential drop is then shared between the two capacitors (dashed line in Figure 1e for the case $C_g = C_{ch}$). With the capacitors being connected in series, the same amount of charge is accumulated on each of them. The potential distribution between the capacitors is determined by their respective capacitances. Figure 1e (dashed line) shows the case $C_g = C_{ch}$. With equal capacitances, the potential drops across the capacitors are also equal (Eqn. 1), meaning half of the applied potential falls over the channel capacitor ($U_{ch} = 0.5$). Figure 1f shows how the fractional potential drop, U_{ch}, across the channel capacitor varies with gate-to-channel capacitance ratio as a DC signal is applied. When used for steady-state

measurements, such as recording of output characteristics or transfer curves, the gate-limited OECT is thus less de-doped at a given gate potential. A gate-limited OECT will exhibit a less steep transfer curve than an OECT without limitation at the gate. This smaller slope of the transfer curve translates directly into a lower transconductance of the transistor. At higher frequencies (for the conditions in Figure 1e and f, above 10 kHz) the differences between the transistors vanish, but neither the gate-limited OECT or the transistor without limitation at the gate are able to reproduce the signal applied to the gate due to insufficient de-doping of the channel. Gate and channel capacitances can be adjusted through their respective geometries. If the gate is made of the same conjugated polymer (*e.g.*, PEDOT:PSS) with the same thickness as the channel, the gate area, A_g, and channel area, A_{ch}, will determine C_g/C_{ch} according to $C_g/C_{ch} = A_g/A_{ch}$. With different materials used for channel and gate, the area itself is not sufficient to define the relationship between capacitances. In the case of a PEDOT:PSS channel transistor with a metal gate, the channel capacitance is set by channel area, channel thickness, T_{ch}, and the capacitance per unit volume, C^*, for the PEDOT film.[25] At the gate, the capacitance scales only with gate area, A_g, and the double layer capacitance per unit area, C_{dl}, of the material. The relationship between gate and channel capacitance is in this case is $C_g/C_{ch} = A_g C_{dl}/(A_{ch} T_{ch} C^*)$.

Capacitive sensing representing a non-permeable membrane on the gate: $C_{g,s}$
To model capacitive sensing we start by considering an ideal case, where the sensing event only causes the gate capacitance to drop to a lower value ($C_g \rightarrow C_{g,s}$), *i.e.*, no leakage is included. In practice, such capacitance alteration could be due to molecular in-binding at the gate (adding a non-conducting/dielectric layer on top of the gate electrode). With a decrease in gate electrode capacitance, a greater fraction of the total applied gate potential will drop at this modified gate-electrolyte interface. Figure 2a-c presents the potential drop over C_{ch} before and during sensing for three different sensor transistors ($C_g = 100C_{ch}$, $C_g = 10C_{ch}$, and $C_g = C_{ch}$), and for three different levels of capacitance reduction upon sensing ($C_{g,s}/C_g = 0.5$, $C_{g,s}/C_g = 0.1$, and $C_{g,s}/C_g = 0.01$). For the transistor with the largest gate capacitance ($C_g = 100C_{ch}$, Figure 2a) almost all of the potential falls

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over the channel capacitor. In this case ($C_g = 100C_{ch}$), when the sensing reaction reduces the gate capacitance to half its original value ($C_{g,s}/C_g = 0.5$) the fractional potential drop over the channel capacitor barely shifts at all. However, for larger capacitance reductions (*i.e.*, for $C_{g,s}/C_g = 0.1$ and $C_{g,s}/C_g = 0.01$) the effect is substantial for frequencies below 1 kHz. The transistors used to produce Figure 2b and 2c have gate capacitances ten times and equal to the channel capacitance, respectively, which causes a larger fraction of the applied potential to drop across the gate before sensing occurs. In these cases, despite the smaller absolute potential drops across the channel, relatively lower changes in capacitance upon sensing are more discernable; consider the clear difference in U_{ch} even for $C_{g,s}/C_g = 0.5$, which was barely noticeable for $C_g = 100C_{ch}$. It is also worth noting that for these transistors the sensitivity to record differential changes is very limited for large absolute changes in capacitance at the gate. As C_g approaches (or even goes lower than) C_{ch}, the initial U_{ch} decreases, leaving less and less dynamic range to record differential changes in $C_{g,s}$; consider how $C_{g,s}/C_g = 0.01$ causes U_{ch} to approach zero as C_g approaches C_{ch}.

In order to compare various transistor geometries with respect to their sensing capabilities we focus on the sensor response, defined herein as the difference in potential drop over the channel capacitor caused by the sensing event, $\Delta U = U_{ch}(C_g) - U_{ch}(C_{g,s})$ (see Eqn. 2), and highlighted by the arrows in Figure 2b. For purely capacitive sensing the maximum sensor response is obtained at low frequencies (up to approximately 1 kHz for the values chosen here for C_{ch} and R_i). Figure 2d shows the sensor response as a function of C_g/C_{ch} and $C_{g,s}/C_g$. The maximum achievable sensor response ΔU *increases* as the capacitance to be sensed $C_{g,s}$ *decreases*. In other words, the larger the *change* in gate capacitance induced during sensing, the larger the maximum ΔU. The peak sensor response is not tied to one specific C_g/C_{ch} value, but rather shifts with the capacitance to be sensed, $C_{g,s}$. In the investigated range, the peak sensor response shifts from $C_g/C_{ch} = 1$ for the smallest capacitance changes to $C_g/C_{ch} = 10$ for the largest.
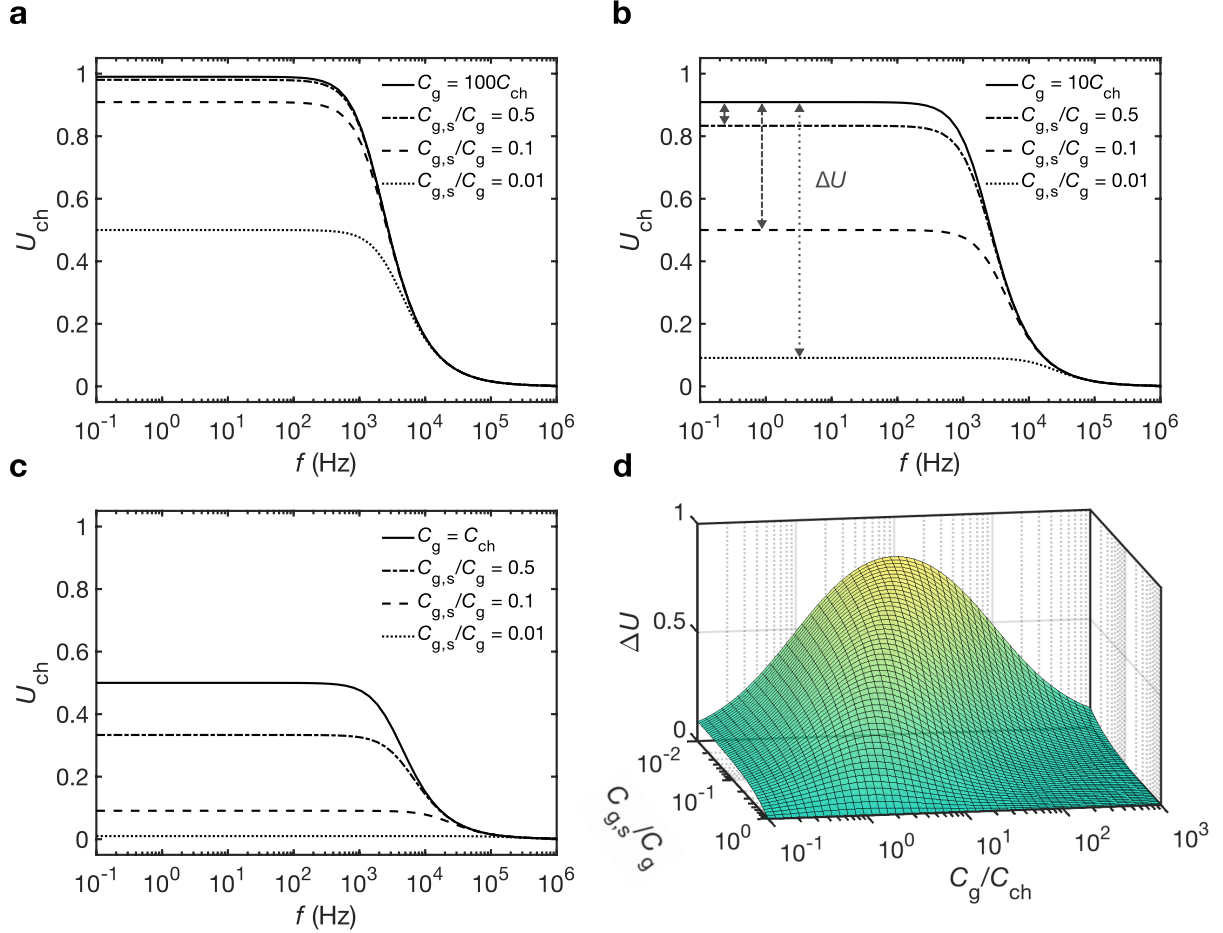
Figure 2. Fractional potential drop over the channel capacitor as a function of frequency for three different cases: (a) $C_g = 100C_{ch}$, (b) $C_g = 10C_{ch}$, and (c) $C_g = C_{ch}$. Solid lines represent potential drops before sensing. Potential drops over C_{ch} are also shown for capacitive sensing where $C_{g,s} = 0.5C_g$ (dash-dot), $C_{g,s} = 0.1\ C_g$ (dash), and $C_{g,s} = 0.01C_g$ (dot). Arrows in part b indicate the difference in relative potential drop used to construct part d. (d) Sensor response, ΔU, as a function of C_g/C_{ch} and $C_{g,s}/C_g$.

Capacitive-resistive sensing representing a permeable membrane on the gate: C_b-R_b

In many biosensing setups the capacitive layer added to the gate is expected to be permeable to ions to some extent. A change in ion permeability can in fact be the important part of the sensing reaction itself, for example in studies of cell layer integrity or when measuring membrane protein ion channel activity.[35–38] In this work we have chosen an equivalent circuit comprising a capacitor, C_b, and resistor, R_b, in parallel as our model system of an ion permeable lipid bilayer (Figure 1d). In order to model sensing with a lipid bilayer, we assume that the capacitance of the bilayer remains constant and that variations instead are found only in the parallel resistance, R_b. In this way, R_b directly represents the level of permeability. The reason for our focus on changes

in R_b is its importance for studies of channel proteins embedded in the cell membrane, *e.g.*, controlling the permeability, and biosensors based on this mechanism.[38,39] Investigating the sensor's dependence on bilayer resistance is also relevant considering the range of resistivity values reported for supported lipid bilayers, spanning several orders of magnitude. On the lower end of the scale there are resistivities on the order of 10 Ωcm^2,[39] and the more resistive bilayers can reach 10^6 Ωcm^2.[40] Figure 3a-b shows the potential drop over the channel capacitor with and without the bilayer model for $C_g = 10C_{ch}$ and $C_g = C_{ch}$. Again, the sensor response differs between transistor configurations. As the frequency decreases, the capacitor impedances increase toward infinity. However, R_b remains at a fixed value and thus exhibits decreasing contribution to the overall impedance with decreasing frequency. Therefore, changes in R_b would cause little or no change to the potential drop across C_{ch} at very low frequencies. The frequencies at which the bilayer can be detected depend on both R_b and C_g/C_{ch}, with higher resistances expanding the detection window to lower frequencies. Figure 3c provides insight on how the bilayer affects the gating of the transistor and the sensor response, here defined as $\Delta U = U_{ch}(C_g) - U_{ch}(C_b, R_b)$. The maximum sensor response is determined by the bilayer capacitance and the C_g/C_{ch} ratio, following the same principles as the non-permeable capacitive sensing discussed in the previous section. The width of the sensing frequency window depends on the bilayer resistance R_b. A high bilayer resistance makes the sensing window wider, since lower frequencies are required for the impedance from the capacitors to outweigh the bilayer resistance.

To compare sensor response between various transistors we use two measures: the maximum sensor response ΔU; and the total sensor response, see Materials and Methods for calculation details. In short, the total sensor response is the sum of the sensor responses, ΔU, calculated for frequencies in the range 0.1 Hz $\leq f \leq$ 1 MHz. Using logarithmically spaced frequency points, the total response is proportional to the geometric area between the curves as they are drawn in the examples in Figure 3a-b. A large area between the curves indicates a high sensor output and a wide sensing window. In Figure 3d the maximum sensor response is shown as function of C_g/C_{ch}

and R_b. The 3D maximum response surface (Figure 3c) displays a ridge growing with increasing R_b. Once R_b is sufficiently high to introduce a plateau in the U_{ch} curve – at approx. $U_{ch} = 0.5$ in Figure 3a and $U_{ch} = 0.1$ in Figure 3b – the maximum response does not increase further, nor does the peak position change beyond this point. However, the total sensor response (Figure 3d) continues to increase throughout the entire range of R_b investigated, since the sensing window (*i.e.*, the frequency range in which the membrane can be detected) grows to cover lower frequencies as R_b increases. As can be seen, both the maximum and total sensor responses vary with C_g/C_{ch}.
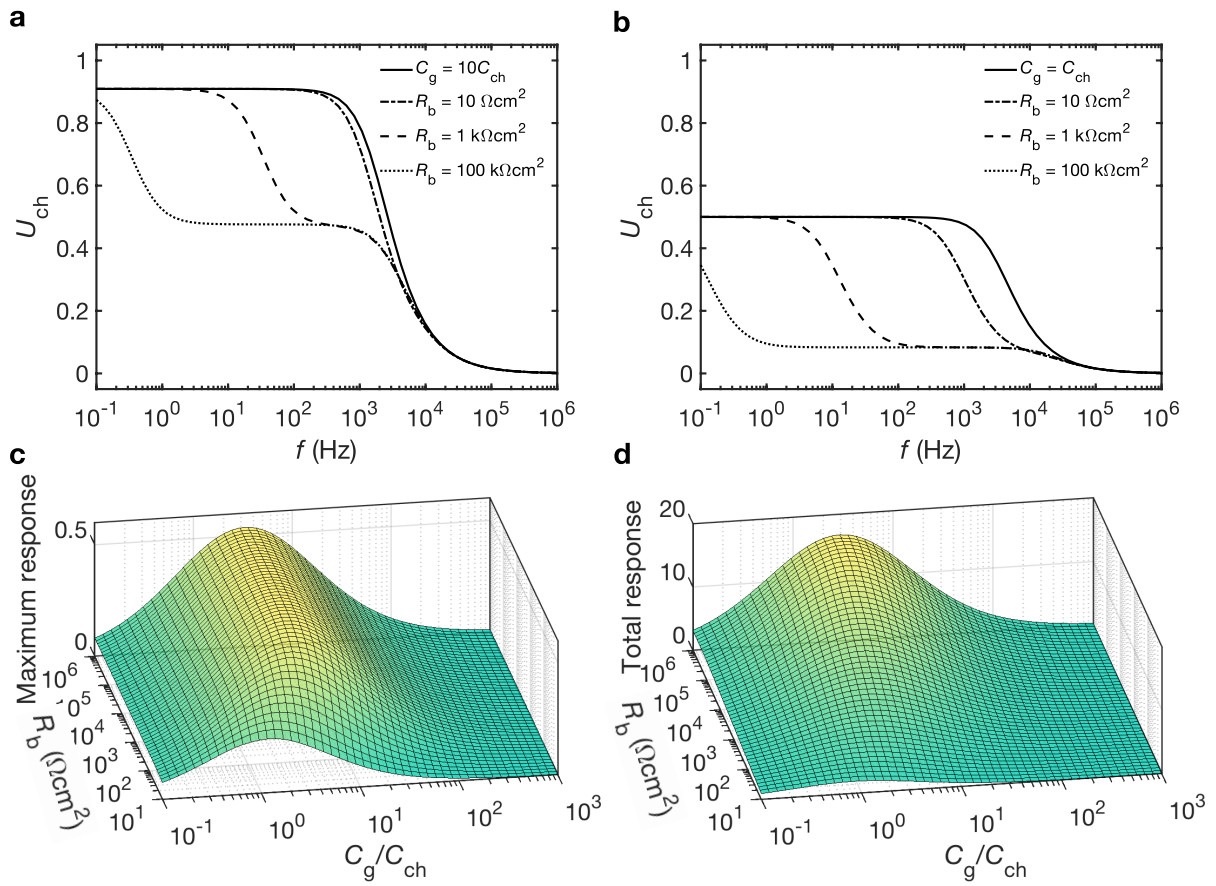

Figure 3. Potential drop over channel capacitor as a function of frequency for a gate-limited transistor with (a) $C_g = 10C_{ch}$ and (b) $C_g = C_{ch}$ (solid lines). The potential drop over the channel transistor is also shown with lipid bilayers added to the gate, $C_b = 0.1C_g$, and $R_b = 10\ \Omega\text{cm}^2$ (dash-dot), $R_b = 1\ \text{k}\Omega\text{cm}^2$ (dash), and $R_b = 100\ \text{k}\Omega\text{cm}^2$ (dot). 3D graphs show the maximum sensor response (c) and the sum of the sensor response (d) in the investigated frequency region (100 mHz ≤ f ≤ 1 MHz) as a function of R_b and C_g/C_{ch}.

Experimental impedance measurements of a lipid bilayer formed on the gate

We proceeded to compare our model with experimental impedance characterization of an OECT with an SLB on its gold gate. In preparation for functionalizing the gate with a lipid bilayer, as well as experimentally determining the bilayer resistance and capacitance, we performed an impedance characterization of a 1,2-dioleoyl-3-trimethylammonium-propane (DOTAP) lipid bilayer formed through vesicle fusion. The chemical structure of DOTAP is shown in Figure 4a. We chose DOTAP vesicle fusion on gold as a model system to demonstrate the possibility of producing OECTs with gold gates functionalized with SLBs. Future applications of gold gate OECTs could incorporate thiol-tethered SLBs, a well-studied lipid bilayer system.[30] The fusion was monitored using quartz crystal microbalance with dissipation monitoring (QCM-D) and the gold sensor surface was used as the working electrode while recording the impedance spectra (Figure S1). Figure 4c shows the impedance spectra measured in PBS buffer before and after vesicle fusion on the QCM-D sensor surface. To obtain values for electrode capacitance, bilayer capacitance, bilayer resistance, and solution resistance we used modified versions of the equivalent circuits presented in Figure 1c-d, where the transistor channel capacitance was excluded from the circuits. The resistance R_i represented the electrolyte resistance and C_g represented the double layer capacitance of the gold working electrode. Fitting the data to the equivalent circuit model gave a lipid bilayer capacitance, C_b, of 1.2 µF/cm^2, and a bilayer resistance R_b of 26 Ωcm^2. The double layer capacitance of the gold electrode was 28.5 µF/cm^2, meaning that the bilayer capacitance amounts to about 4% of the gold double layer capacitance . The lipid bilayer resistance was found to be in the lower end of values previously reported for supported lipid bilayers, but comparable to what has been obtained in QCM setups.[23,39] The bilayer capacitance, C_b, corresponds well with previously reported values for DOTAP bilayers formed through vesicle fusion.[41] Expecting a bilayer resistance on the order of 10 Ωcm^2, the transistor was designed to have similar gate and channel capacitances in accordance with the results shown in Figure 3b, *i.e.*, the $C_g = C_{ch}$ configuration. We chose this configuration with the express aim of detecting the lipid bilayer.

Several other C_g/C_{ch} ratios were tried (all close to 1:1; data not shown), but none had large enough C_g to fail to detect the bilayer. The OECT channel material was PEDOT:PSS and the gold gate was placed on the same substrate. To account for the different capacitances per unit area of PEDOT:PSS and gold, the geometric surface area of the gate was 25 times larger than that of the channel, resulting in a C_g/C_{ch} of about 4. Table S1 provides guidance on how to obtain different C_g/C_{ch} for the material combination of our OECT. The frequency response of the gold gate OECT was measured using a voltage divider amplifier circuit, as shown in Figure 4b (see Figure S2 and S3 for transfer and output characteristics of the gold gate OECT). 10 mV peak-to-peak sinusoidal signals, V_{in}, ranging from 1 Hz to 100 kHz were applied to the gate and the input and output signals were monitored with an oscilloscope. Figure 4d shows the frequency-dependent gain of the amplifier circuit. The alteration in curve shape induced by the lipids corresponds well with the low resistance bilayer modeled in Figure 3b, with limited sensor response at frequencies below 100 Hz and no U_{ch} plateau induced by the bilayer. For these limited bilayer resistances, the signature of the bilayer can be best characterized as slowing the transistor down, manifesting as the onset of gain decay shifting towards lower frequencies. This shift in decay onset can be observed in Figure 4d as well as in the modeled response in Figure 3b (10 Ωcm^2, dash-dot).
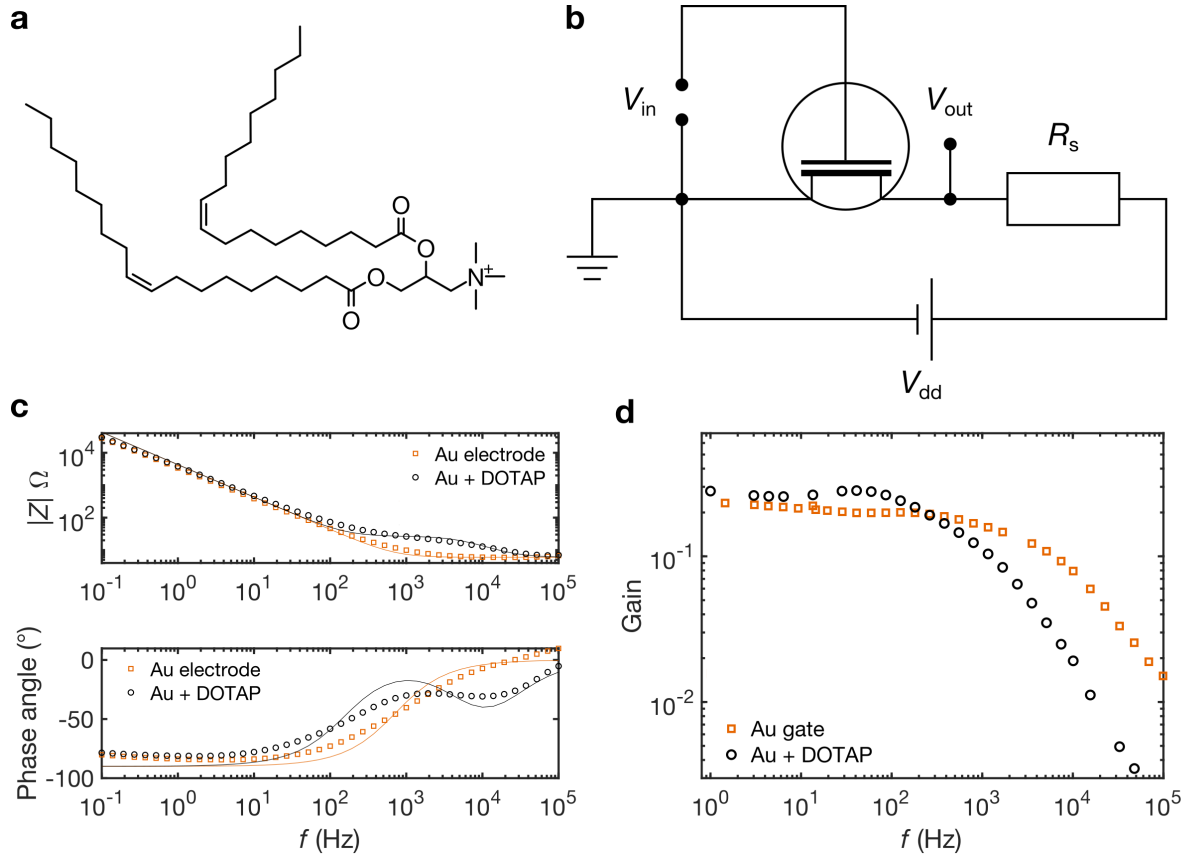
Figure 4. Experimental investigation of OECT with SLB on gold gate. (a) DOTAP chemical structure. (b) Amplifier circuit used to record OECT frequency response. (c) Impedance spectra recorded in buffer for QCM-D gold electrode and QCM-D gold electrode with a DOTAP lipid bilayer. Data fits shown as solid lines. (d) Gold gate OECT gain response before and after addition of DOTAP vesicles.

Materials and methods

Modelling

Sensor models were investigated using custom MATLAB software. The impedance of C_{ch} divided by the total equivalent circuit impedance was used as a measure of the partial potential drop over the channel capacitor. The impedances were calculated at 60 logarithmically spaced frequency points, and low frequency, maximum, and total sensor responses were calculated.

The channel capacitance, C_{ch}, was assumed to be 100 nF and the internal resistance R_i 1 kΩ. In the cases of gate-limited transistors and non-permable sensing at the gate C_g, and $C_{g,s}$ were determined directly from the C_g/C_{ch} and $C_g/C_{g,s}$ ratios. For ion-permeable sensing we assumed an area dependent gate capacitance with the double layer capacitance C_d = 28.5 μF/cm², in accordance

with the capacitance found for our gold QCM sensor. The C_g/C_{ch} ratio and the double layer capacitance was then used to determine the gate electrode area, in turn used to calculate the resulting lipid bilayer resistance for the investigated values of lipid bilayer resistivity, R_b. Line defects around electrode edges were not considered.

Vesicle preparation

The lipids (Avanti Polar Lipids) were dissolved in chloroform (Merck) to a weigh-to-volume ratio of 10 mg/ml. The stock solution was stored at -20 °C. Vesicle preparation was done in three steps: solvent evaporation, rehydration, and extrusion. For solvent evaporation, 100-200 µl of the vesicle solution was placed in a glass vial and gently dried using a nitrogen stream. The lipid cake was then rehydrated in PBS (phosphate buffered saline; tablets, Merck) to a lipid content of 1 mg/ml and stirred for at least 1 h. Extrusion was done using the Avanti Mini Extruder (Avanti Polar Lipids) equipped with a 100 nm pore diameter track-etched polycarbonate membrane (Nuclepore). The lipid suspension was pushed through the filter 11 times. Vesicles were stored cold (<8 °C) and used within 36 h.

Impedance measurements

Combined QCM and impedance measurements were done in a Qsense Analyzer equipped with an electrochemistry module. QSX338 sensors comprising a Au sensor surface with Ti adhesion layer were used. The sensors were cleaned for 7 min in a 5:1:1 mixture of DI water, hydrogen peroxide, and ammonia heated to 70 °C followed by extensive rinsing in DI water, drying, and a 20 min UV/ozone treatment. Prior to vesicle introduction a reference impedance spectrum was recording using a µAutolab (Metrohm) potentiostat. The rms amplitude was set to 10 mV and the signal was applied at the open circuit potential. Throughout the QCM experiment the flow rate was 100 µl/min, regulated by an Ismatec peristaltic pump. As the vesicles were introduced at a lipid content of 0.2 mg/ml in PBS, the impedance at 200 Hz was tracked. At the end of the experiment another impedance spectrum was recorded.

Transistor fabrication

Transistors were photolithographically patterned onto glass substrates. Thermally evaporated gold (50 nm) with a titanium (5 nm) adhesion layer was used for contacts, leads, and the gate electrode. The transistor channels were spin-coated from a commercially available PEDOT:PSS suspension (Clevios PH1000, Heraeus), with 5 % v/v polyethylene glycol (PEG) and 0.1% v/v 3-glycidoxypropyltrioxysilane (GOPS) added. Substrates were treated with oxygen plasma before spin-coating. The spin speed was 3000 rpm, resulting in a film thickness of about 60 nm. The PEDOT:PSS films were baked at 100 °C for 60 min before subsequent patterning with reactive ion etching (Vacutec) using CF_4. SU-8 (MicroChem) was used for encapsulation and was photolithographically patterned onto the devices as the final step. The gate electrode area was 0.1 mm², and channels were 20 μm long and 200 μm wide. Figure S2 and S3 show transfer and output characteristics.

Transistor measurements

The frequency dependence of the transistors was characterized using a voltage divider amplifier circuit. The driving potential was supplied using a power supply, and the gate signal was applied using an Agilent 33250A waveform generator. The amplitude of the sine signal was 10 mV, with a 0 V offset. A 1.2 kΩ resistor was connected in series with the transistor channel. The output potential was measured across the transistor channel. Gate and output signals were measured simultaneously with an Agilent Infiniium oscilloscope. Analysis to extract gain and phase angle was performed using custom MATLAB software. The driving potential was set such that the drain potential was -650 mV. The operational conditions were chosen based on a transfer curve recorded using a Keithley 4200 parameter analyzer. All transistor measurements were carried out in PBS and the lipid vesicles were allowed a 20 min fusion and stabilization period after being added onto the transistor.

Total sensor response calculation

The total sensor response for the model including a permeable membrane on the gate represents the geometrical area between the $U_{ch}(C_g)$ and $U_{ch}(C_{g,s})$ curves of Figure 4a-b, not the integral over

frequency. Rather, the frequency points were logarithmically spaced, and the total sensor response was defined as $\sum \Delta U_{ch}(f)$ over each of these logarithmically spaced points. This summation was chosen over integration to avoid giving too much weight to higher frequencies. The frequency range chosen was $0.1\ \text{Hz} \leq f \leq 1\ \text{MHz}$.

Conclusions

Capacitive sensing with OECTs is highly dependent on transistor geometry when a capacitive element is added to the gate. The transistors best suited for capacitive sensing are not what would typically be described as high-performance transistors exhibiting high transconductance. Instead, the largest sensing signals are obtained with gate-limited transistors, where gating of the transistor channel is already limited by the double layer capacitance at the gate electrode. The C_g/C_{ch} most favorable for sensing varies with the capacitance to be sensed, meaning the expected capacitance shift should be known beforehand when designing the transistor. For capacitive sensing where the capacitive layer is not added to the gate, the modification is best described by introducing a gate capacitance. The most favorable sensing is then achieved by starting from an ideal OECT with, for example, a nonpolarizable gate electrode, and then striving to make the channel capacitance large compared to the capacitance of the sensor layer. Modifying the channel results in larger sensor responses than modifying the gate, since no potential drops at the gate-electrolyte interface. Functionalizing the gate can still be attractive due to the larger variety in gate material and functionalization options. Sensing at steady-state is possible for capacitive layers without ion leakage.

For ion permeable capacitive layers, such as lipid bilayers, the sensing will occur within a frequency window determined by the ionic resistance through the capacitive layer and the gate-to-channel capacitance ratio. With the sensing being confined to a specific frequency window, dynamic measurements are required. Furthermore, in this case the small gate transistors typically considered poor performers are better suited for some of the sensing applications where low

resistance and high ionic permeability are to be expected. It should be noted, however, that small gate transistors are not always the best sensor choice, since the initial potential drop at the gate leaves less dynamic range for measurement of large changes in gate capacitance.

Acknowledgements

Conflict of interest

The authors declare no conflicts of interest.

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The role of relative capacitances in impedance sensing with organic electrochemical transistors

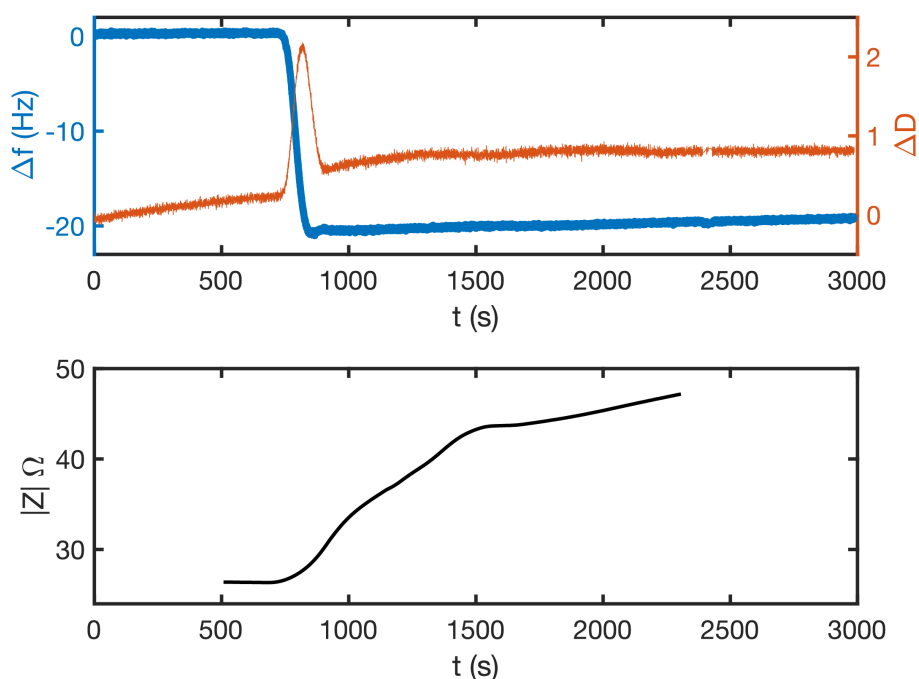*Josefin Nissa, Per Janson, Magnus Berggren,* Daniel T. Simon*

Figure S1. (top) QCM-D tracking of DOTAP vesicle fusion on Au sensor, 7th harmonic only, chosen as characteristic of the other harmonics. Blue trace (left y-axis) shows frequency shift and orange trace (right y-axis) dissipation vs time. Vesicles introduced 700 s into the measurement. (bottom) Absolute value of impedance versus time recorded at 200 Hz, 10 mV rms amplitude.
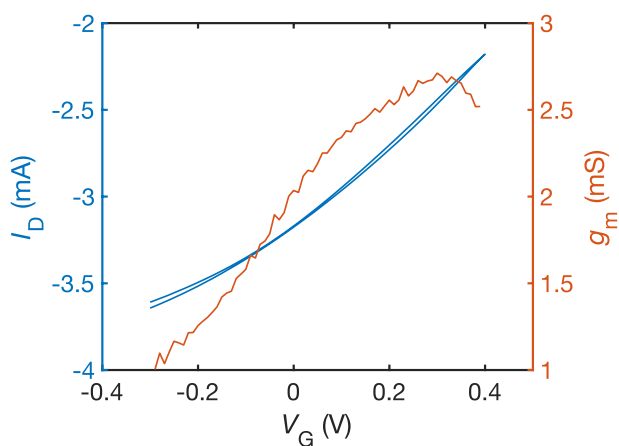

Figure S2. Transfer curve and transconductance for Au gate transistor used in DOTAP experiment. Recorded at V_d = -600 mV in PBS buffer before addition of DOTAP.
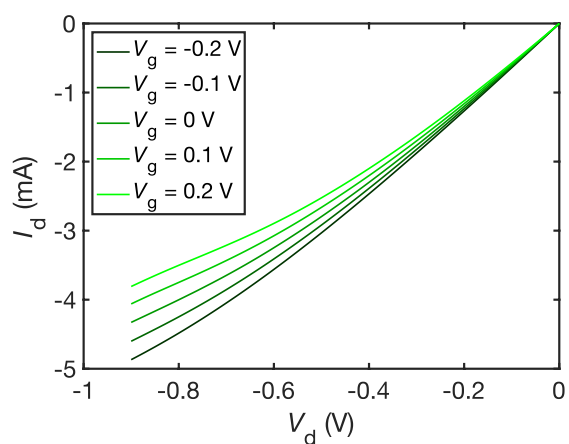

Figure S3. Output characteristics for gold gate OECT used in DOTAP experiment. Recorded in PBS buffer before addition of DOTAP.

Table S1. Suggestions for device geometries for various C_g/C_{ch}. The calculations are based on a 60 nm thick PEDOT:PSS channel and gold gate electrode. Gate double layer capacitance is assumed to be 25 μF/cm², and channel capacitance 160 μF/cm². W and L represent channel width and length, respectively. Note that there are many other possible gate and channel geometries producing the same C_g/C_{ch}.

C_g/C_{ch}	A_g/A_{ch}	A_g (mm²)	A_{ch} (mm²)	W (μm)	L (μm)
0.1	0.64	0.1	0.156	1250	125
1	6.4	0.1	0.0156	395	39.5
10	64	0.1	0.00156	125	12.5
100	640	1	0.00156	125	12.5