EZcomm

# EZcomm Technology Co., Ltd.

# 捷揚電通股份有限公司

## Product Specification

**Product Name: EZ2625**
NBIoT / GPS Module

**Version : 1.3**

**Doc No :**

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## DOCUMENT HISTORY

The next table gives an overview of the changes to the document

| DATE | VERSION | CHANGE | AUTHOR |
|---|---|---|---|
| 2019-01-03 | 1.0 | Preliminary | Vic Yang |
| 2019-01-07 | 1.1 | Update Table 1-4 | Vic Yang |
| 2019-07-12 | 1.2 | Add the Content of Chapter 9 | Vic Yang |
| 2019-07-22 | 1.3 | Update Table 5-10 | Vic Yang |
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## TERMS AND ABBREVIATION

| Abbreviation | Description |
|---|---|
| 3GPP | Third Generation Partnership Project |
| ADC | Analog-to-Digital Converter |
| BER | Bit Error Rate |
| BDS | BeiDou Navigation Satellite System |
| CEP | Circular Error of Probability |
| DCE | Data Communication Equipment |
| DL | Downlink |
| DTE | Data Terminal Equipment |
| eDRX | Extended Discontinuous Reception |
| EMC | Electromagnetic Compatibility |
| ESD | Electro-Static Discharge |
| E-UTRA | Evolved Universal Terrestrial Radio Access |
| H-FDD | Half Frequency Division Duplexing |
| GNSS | Global Navigation Satellite System |
| GPIO | General Purpose I/O |
| GPS | Global Positioning System |
| I2C | Inter-Integrated Circuit |
| NB-IoT | Narrow Band Internet of Things |
| LED | Light Emitting Diode |
| LGA | Land Grid Array |
| LTE | Long Term Evolution |
| M2M | Machine to Machine |
| MCS | Modulation and Coding Scheme |
| MO | Mobile Origination Cell |
| MT | Mobile Termination Cell |
| NC | Not Connect |
| PCB | Printed Circuit Board |
| PDN | Packet Data Network |
| PDU | Protocol Data Unit |
| PMU | Power Management Unit |
| PPP | Precise Point Positioning |
| PSM | Power Saving Mode |
| PTW | Paging Time Window |
| RF | Radio Frequency |

| | |
|---|---|
| RHCP | Right Hand Circular Polarization |
| RTC | Real Time Clock |
| RX | Receive Direction |
| SMS | Short Message Service |
| SPI | Serial Peripheral Interface |
| TAU | Tracking Area Update |
| TTFF | Time To First Fix |
| TVS | Transient Voltage Suppressor |
| TX | Transmit Direction |
| UART | Universal Asynchronous Receiver & Transmitter |
| UL | Uplink |
| USB | Universal Serial Bus |
| USIM | Universal Subscriber Identity Module |
| VSWR | Voltage Standing Wave Ratio |

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Figure index

# 1 OVERVIEW

This document describes the hardware interface of EZ2625 series modules to help users quickly understand the interface specification, electrical characteristics, mechanical dimensions and other related information of EZ2625 series modules.

## 1.1 INTRODUCTION

EZ2625 series is NB-IoT module compliant with 3GPP R13/R14 of CAT-NB1/NB2 standard and it includes GNSS and e-SIM designed for IoT/M2M application. It is the smallest LTE CAT-NB1/NB2 module in the market and meet the essential LTE connectivity with the network operator's infrastructure.

It features ultra-compact size, ultra-low power consumption, extended coverage and enhanced RF performances with the miniature LGA form factor (14.0 x 14.0 x 1.85mm, 52-pin). It provides the cost effective and size sensitive solution to help users to quick develop their devices for the strong growth in the NB-IoT market.

EZ2625 series modules include multiple sub-models and support E-UTRA operating bands B1/ B3/ B5/ B8/ B20/ B28 and GNSS (GPS/GLONASS/BDS/Galileo) technology. User can select a specific type based on wireless network and required functions.

**Table 1-1 : E-UTRA Operating Bands of EZ2625 Series**

| LTE Band | UL (MHz) | DL (MHz) | DUPLEX MODE |
|---|---|---|---|
| 1 | 1920 - 1980 | 2110 – 2170 | H-FDD |
| 3 | 1710 -1785 | 1805 - 1880 | H-FDD |
| 5 | 824 - 849 | 869 – 894 | H-FDD |
| 8 | 880 – 915 | 925 - 960 | H-FDD |
| 20 | 832 - 862 | 791 – 821 | H-FDD |
| 28 | 703 - 748 | 758 - 803 | H-FDD |

**Table 1-2 : GNSS Operating Bands of EZ2625 Series**

| GNSS Band | Frequency (MHz) |
|---|---|
| GPS L1 | 1575.42 +/- 1.023 |
| BeiDou B1 | 1561.098 +/- 2.046 |
| GLONASS G1 | 1602.5625 +/- 4 |
| Galileo E1 | 1575.42 +/- 1.023 |

**Table 1-3 : Product Selector of EZ2625 Series Modules**

| MODEL | PID | NB-IoT | Band | GNSS | e-SIM |
|---|---|---|---|---|---|
| EZ2625 | A01 | √ | B1/B3/B5/B8/B20/B28 | √ | √ |
| | G01 | √ | B1/B3/B5/B8/B20/B28 | √ | |
| | E01 | √ | B1/B3/B5/B8/B20/B28 | | √ |
| | L01 | √ | B1/B3/B5/B8/B20/B28 | | |

## 1.2 KEY FEATURES

**Table 1-4 : Key Features of EZ2625 Series**

| Item | Description | Specification |
|---|---|---|
| **Form Factor** | LGA | 52-PIN |
| **Physical Features** | Dimension | 14.0mm x 14.0mm x 1.85mm |
| | Weight | < 1g |
| **LTE Operating Frequency** | Band | B1/B3/B5/B8/B20/B28 |
| **GNSS Operating Frequency** | Band | GPS / BeiDou / GLONASS [1] / Galileo [1] |
| **Data Rate** | Single-Tone (NB1) | Max. DL: 26Kbps / UL: 16Kbps |
| | Multi-Tone (NB1) | Max. DL: 26Kbps / UL: 62Kbps |
| **Application Interface** | USIM | - Support external 3V/1.8V USIM card<br>- Supply VBAT_PA with 3.3 ~ 3.6V if 3V USIM is required |
| | UART | Main port UART1:<br>- 4-wires interface, supporting RTS/CTS flow control<br>- AT command and data transmission<br>- Default baud rate is 115200bps<br>Debug port UART0:<br>- 2-wires interface<br>- Debug and upgrade firmware<br>- Default baud rate is 115200bps |
| | USB | - USB 1.1 interface<br>- Capture debug log. Logging channel can be selected by AT command. |

| | | |
|---|---|---|
| | SPI | Support slave interface, 1/2-bit mode, clock up to 52MHz |
| | I2C | Support master mode, up to 3.4Mbps |
| | ADC | 10-bit ADC. The maximum input voltage is 1.4V. |
| | RESET | System reset control, active low |
| | PWRKEY | System power on/off control, active low |
| | Antenna | MAIN_ANT:<br>- Connect to LTE antenna terminal with 50Ω impedance control<br>GNSS_ANT:<br>- Connect to GNSS antenna terminal with 50Ω impedance control |
| **Data Service** | Internet Protocol | - IPv4/IPv6<br>- TCP/UDP/CoAP/MQTT/LWM2M<br>- HTTP/HTTPS |
| **Short Message** | SMS | MT, MO, Text and PDU |
| **Programming** | Firmware Upgrade | Debug port UART0 |
| **Power Supply** | VBAT | 2.1V ~ 3.6V, typical 3.3V |
| **Current Consumption** | Active | - B1: 130mA @ 23dBm<br>- B3: 120mA @ 23dBm<br>- B5: 110mA @ 23dBm<br>- B8: 130mA @ 23dBm<br>- B20: 110mA @ 23dBm<br>- B28: 130mA @ 23dBm |
| | IDLE | 5mA |
| | Light Sleep (eDRX) | 0.2mA |
| | Deep Sleep (PSM) | 3.5uA |
| | OFF | 2.5uA |
| **Environment** | Operating Temperature | -30 ~ 75℃ |
| | Extend Temperature | -40 ~ 85℃ |

1: By default, EZ2625 module is configured to receive GPS and Beidou signals in parallel. For other system configurations, it is under development.

## 1.3 APPLICATION

- Smart Grid
- Smart Metering
- Smart Parking

- Traffic Management and Monitoring
- Security and Asset Tracking
- Home and Industrial Automation
- Agricultural and Environmental Monitors

## 1.4 FUNCTIONAL BLOCK DIAGRAM

The functional block diagram and interfaces of EZ2625 series are illustrated in the figure below. The major functional units of EZ2625 series contain the following parts.

- Main chip: Baseband controller, Power Management Unit, RF transceiver and Memory
- RFFE: RF switch, transmitter filter, receiver filter, power amplifier and RF matching circuit
- Clock unit: 26MHz crystal oscillator and 32.768kHz crystal oscillator
- Dotted line: Functional blocks of GNSS and e-SIM

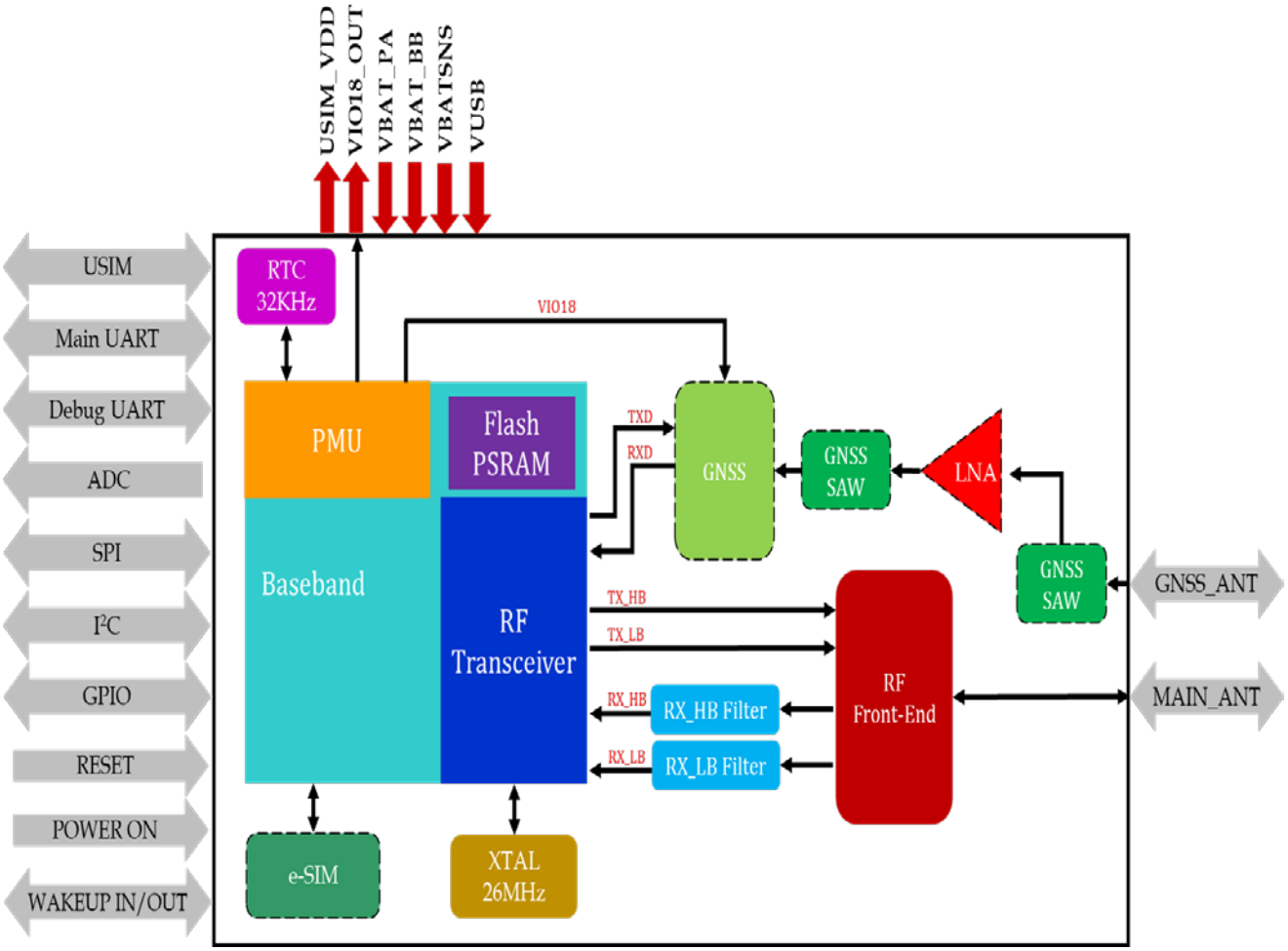



**Figure 1-1 : Functional Diagram of EZ2625 Series**

## 1.5 OPERATING MODES

EZ2625 series has various operating modes, which determine available functionality for different levels of power-saving. The table below summarizes the various operating modes.

**Table 1-5 : Overview of Operating Modes**

| Operating Mode | Function Description |
|---|---|
| ACTIVE | In ACTIVE mode, all functionality of module is available. Radio transmission and reception is performed whilst in this mode. Power consumption is related to data rate of uplink/ downlink, power control level and etc. |
| IDLE | In IDLE mode, the PMU keeps current voltage and all processors and peripherals are in the idle state. In this mode, module is registered to the network and paging reception. |
| FLIGHT | Send AT command "AT+CFUN=4" to enter the FLIGHT mode. In this mode, Radio transmission and reception is disable, but communication interface is accessible. |
| PSM | Send AT command to enter the PSM mode and it is exited by WAKEUP_IN or PWRKEY event. In this mode, all functionality is not unavailable except the RTC function. Meanwhile, RTC_GPIO0 will change state from low to high if WAKEUP_IN receive interrupt event. |
| OFF | Send AT command "AT+TPWROFF" or pull down PWRKEY to enter the OFF mode and it is exited by WAKEUP_IN or PWRKEY event. In this mode, PMU is shut down and communication interface is not accessible. |

## 1.6 POWER SAVING TECHNOLOGIES

Many IoT device are battery-operated and required to last for as long as possible on a single charge. To achieve this, NB-IoT introduces two new low-power enhancements: Power Saving Mode (PSM) and Extended Discontinuous Reception (eDRX) to further reduce power consumption and extend battery life

### *1.6.1 Power Saving Mode (PSM)*

The PSM process starts after a data link is terminated or after the periodic tracking area update (TAU) procedure completes. The device first goes into the idle mode and remains reachable via paging. After timer T3324 expires, the power saving mode is entered. PSM time is the difference between these timers (T3412-T3324). In this mode, the device remains registered with the network and there is no need to re-attach or re-establish PDN connections, but the device is not reachable in PSM Mode until until a mobile originated transaction (e.g. periodic TAU, uplink data transmission) requires it to initiate any procedure towards the network.

The power saving features PSM applicable for NB-IoT is illustrated in the figure below.

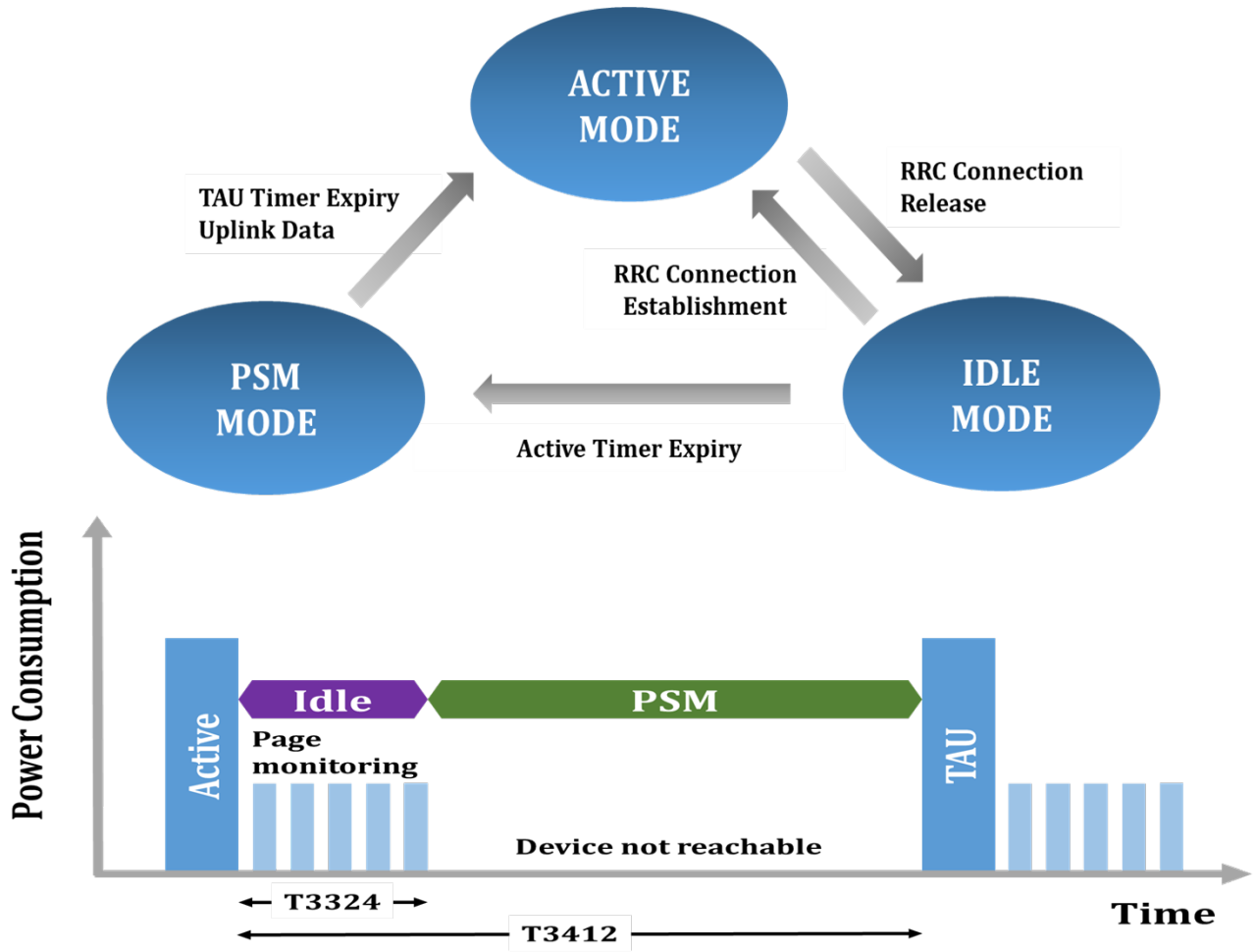



**Figure 1-2 : The Operation of PSM**

### *1.6.2 Extended Discontinuous Reception (eDRX)*

The eDRX is an another technology for reducing the power consumption. With the eDRX, the time interval is extended the modem goes into receive mode to receive paging messages and system status information. The eDRX timer determines how often this occurs. The eDRX cycle length duration can be configured by timer, ranging from 20.48 seconds to 2.92 hours. The paging time window (PTW) can be configured by a timer, ranging from 2.56s to 40.96s.

The power saving features eDRX applicable for NB-IoT is illustrated in the figure below.

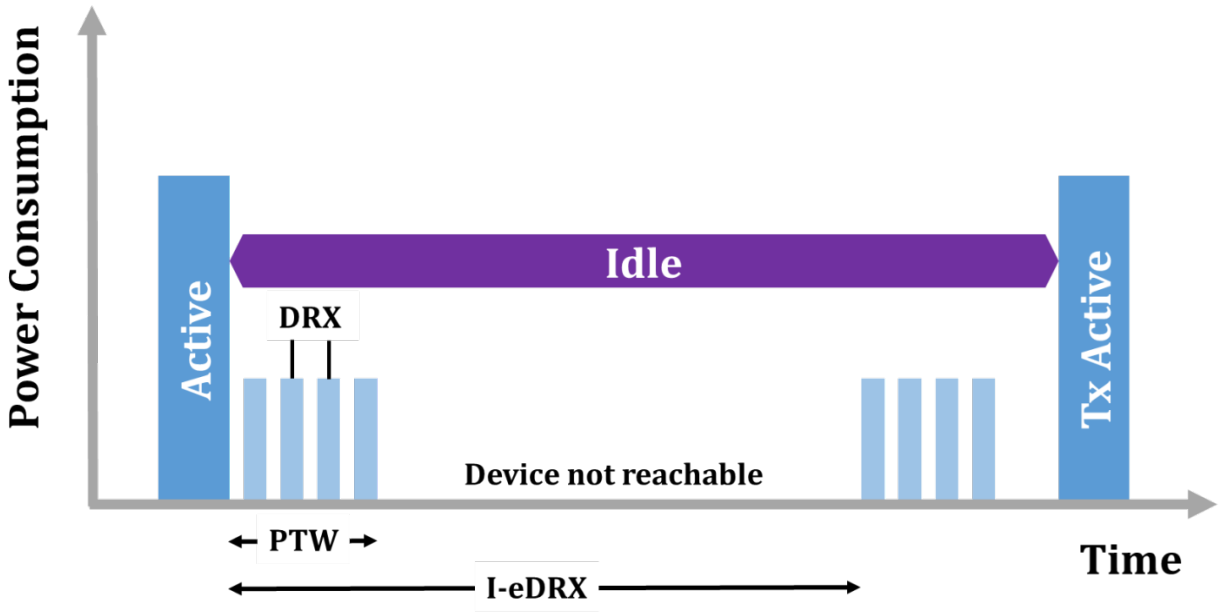



**Figure 1-3 : The Operation of eDRX**

# 2 PIN DEFINITION

## 2.1 PIN OUTLINE

EZ2625 series is a LGA package and equipped with 52 pins. The system interfaces are illustrated in the figure below.

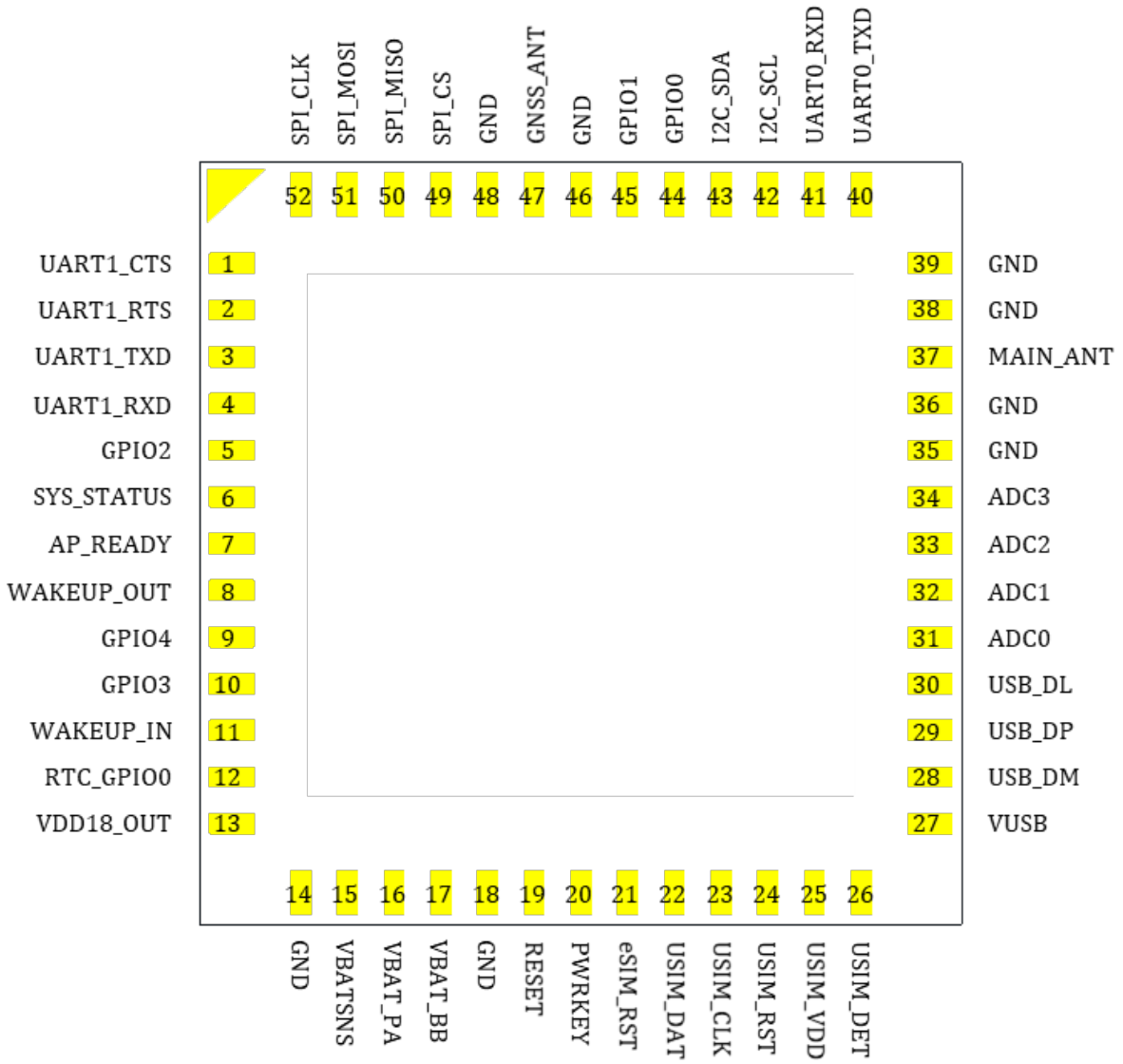



**Figure 2-1 : Pin Assignment (TOP VIEW)**

## 2.2 PIN DESCRIPTION

The system interface of EZ2625 series is through the LGA pad on the bottom of the PCB. The following table indicates the pin definition and description.

**Table 2-1 : Pin Definition and Description**

| Pin Name | Pin No. | Type | Description | Note |
|---|---|---|---|---|
| **Power Supply** | | | | |
| VBATSNS | 15 | PI | Battery sensing input | The maximum input voltage is 5.2V. The ratio of divider resistor is 4. |
| VBAT_PA | 16, | PI | Main power supply input. Voltage range is 2.1V-3.6V, typically 3.3V. | Supply VBAT_PA with 3.3V-3.6V if 3V USIM is required. |
| VBAT_BB | 17 | PI | Main power supply input. Voltage range is 2.1V-3.6V, typically 3.3V. | |
| VDD18_OUT | 13 | PO | 1.8V power supply output for external circuit, such as level shift circuit. | Leave it open if not used |
| GND | 14,18,35, 36,38,39, 46,48 | GND | Ground connection | Must be connected to ground |
| **UART Interface** | | | | |
| UART1_CTS | 1 | DI | UART1 clear to send | Used for AT command and data transmission. 1.8V power domain. Recommend to reserve test point. |
| UART1_RTS | 2 | DO | UART1 request to send | |
| UART1_TXD | 3 | DO | UART1 transmit data | |
| UART1_RXD | 4 | DI | UART1 receive data | |
| UART0_TXD | 40 | DO | UART0 transmit data | Used for debug and upgrade firmware. 1.8V power domain. Recommend to reserve test point. |
| UART0_RXD | 41 | DI | UART0 receive data | |
| **USIM Interface** | | | | |
| eSIM_RST | 21 | DO | eSIM reset signal | - EZ2625-A01: Connect with USIM_RST<br>- EZ2625-E01: Connect with USIM_RST<br>- EZ2625-G01: Keep it open<br>- EZ2625-L01: Keep it open |
| USIM_DAT | 22 | DIO | USIM data signal | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |

| | | | | |
|---|---|---|---|---|
| USIM_CLK | 23 | DO | USIM clock signal | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |
| USIM_RST | 24 | DO | USIM reset signal | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Connect with eSIM_RST<br>- EZ2625-E01: Connect with eSIM_RST |
| USIM_VDD | 25 | PO | USIM power supply output. Output voltage is dependent on SIM card type. | Connect with a TVS diode for ESD protection.<br>- EZ2625-A01: Connect with 0.1uF decoupling capacitor<br>- EZ2625-E01: Connect with 0.1uF decoupling capacitor |
| USIM_DET | 26 | DI | USIM detect signal | If used, pull up to VDD18_OUT with 10Kohm.<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |
| **USB Interface** | | | | |
| VUSB | 27 | PI | 3.3V USB power supply input | 3.3V power domain. Used for debug. |
| USB_DM | 28 | DIO | Positive line of USB differential signal. | 90ohm differential impedance is required. |
| USB_DP | 29 | DIO | Negative line of USB differential signal | 90ohm differential impedance is required. |
| USB_DL | 30 | DI | USB download mode selection. Do not pull down before power on. | GND: USB download mode<br>1.8V: No USB download mode.<br>Leave it open if not used. |
| **SPI Interface (Support Slave Mode)** | | | | |
| SPI_CS | 49 | DI | SPI chip select signal | 1.8V power domain. Leave it open if not used. |
| SPI_MISO | 50 | DO | SPI master in and slave out | 1.8V power domain. Leave it open if not used. |
| SPI_MOSI | 51 | DI | SPI master out and slave in | 1.8V power domain. Leave it open if not used. |
| SPI_CLK | 52 | DI | SPI clock input | 1.8V power domain. Leave it open if not used. |
| **I2C Interface** | | | | |
| I2C_SCL | 42 | DIO | I2C serial clock signal | 1.8V power domain. Pull up to 1.8V with 2.2Kohm if used. Leave it open if not used. |
| I2C_SDA | 43 | DIO | I2C serial data signal | 1.8V power domain. Pull up to 1.8V with 2.2Kohm if used. Leave it open if not used. |
| **ADC Interface** | | | | |
| ADC0 | 31 | AI | Analog-to-digital converter input | 1.8V power domain. 10-bit ADC. The maximum input |

| | | | | |
|---|---|---|---|---|
| | | | | voltage is 1.4V. Leave it open if not used. |
| ADC1 | 32 | AI | Analog-to-digital converter input | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |
| ADC2 | 33 | AI | Analog-to-digital converter input | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |
| ADC3 | 34 | AI | Analog-to-digital converter input | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |
| **RF Interface** | | | | |
| MAIN_ANT | 37 | AIO | LTE antenna port | 50Ω impedance control is required. Connect with a TVS diode for ESD protection |
| GNSS_ANT | 47 | AI | GNSS antenna port | 50Ω impedance control is required. Connect with a TVS diode for ESD protection.<br>- EZ2625-E01: Keep it open<br>- EZ2625-L01: Keep it open |
| **System Control** | | | | |
| RESET | 19 | DI | System reset control, active low. | VBAT power domain. Internal pull high with 40Kohm. |
| PWRKEY | 20 | DI | System power on/off control, active low. | VBAT power domain. Internal pull high with 40Kohm. |
| WAKEUP_IN | 11 | DI | Dedicate external interrupt input in RTC | VBAT power domain. It is the wake up source for exiting PSM. Pull up to VBAT with 10Kohm if used. |
| RTC_GPIO0 | 12 | DO | External boost control in RTC | VBAT power domain. In PSM, it will change state from low to high if WAKEUP_IN receive interrupt event. |
| **GPIO Interface** | | | | |
| GPIO2 | 5 | DIO | General purpose input/output | 1.8V power domain. Leave it open if not used. |
| SYS_STATUS | 6 | DO | The indication of network status | 1.8V power domain. Leave it open if not used. |
| AP_READY | 7 | DO | The indication of operating status.<br>High level: Power on and F/W ready<br>Low level: Power off | 1.8V power domain. Leave it open if not used. |
| WAKEUP_OUT | 8 | DO | Module wake up the host | 1.8V power domain. Leave it open if not used. |
| GPIO4 | 9 | DIO | General purpose input/output | 1.8V power domain. Leave it open if not used. |

| | | | | |
|---|---|---|---|---|
| GPIO3 | 10 | DIO | General purpose input/output | 1.8V power domain. Leave it open if not used. |
| GPIO0 | 44 | DIO | General purpose input/output | 1.8V power domain. Leave it open if not used. |
| GPIO1 | 45 | DIO | General purpose input/output | 1.8V power domain. Leave it open if not used. |

**Table 2-2 : I/O Definition**

| Type | Description |
|---|---|
| AIO | Analog input and output |
| AI | Analog input |
| AO | Analog output |
| DIO | Digital input and output |
| DI | Digital input |
| DO | Digital output |
| PI | Power input |
| PO | Power output |
| GND | Ground |

# 3 ELECTRICAL SPECIFICATION

## 3.1 ABSOLUTE MAXIMUM RATING

**Table 3-1 : Absolute Maximum Ratings**

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Voltage to VBAT_PA/VBAT_BB | -0.3 | +3.63 | V |
| Voltage to VBATSNS | -0.3 | +5.5 | V |
| Voltage to VUSB | -0.3 | +3.63 | V |
| Voltage to USIM_VDD | -0.3 | +3.63 | V |
| Voltage to Digital Pins (UART/SPI/I2C/GPIO) | -0.3 | +1.98 | V |
| Voltage to USIM Pins | -0.3 | +3.63 | V |
| Voltage to Control Pins (RESET/PWRKEY/WAKEUP_IN/ RTC_GPIO0) | -0.3 | +3.63 | V |

## 3.2 ENVIRONMENTAL REQUIREMENT

**Table 3-2 : Environment Requirement**

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| Normal Operating Temperature Range | -30 | +75 | ℃ |
| Extended Operating Temperature Range | -40 | +85 | ℃ |
| Storage Temperature | -40 | +90 | ℃ |
| Operating Humidity | 10 | 85 | % |
| Storage Humidity | 5 | 90 | % |

- Normal Operating Temperature Range: The functionality of module is met the 3GPP specification across the specified temperature range.
- Extended Operating Temperature Range: The functionality of module is normal across the specified temperature range. The deviation from 3GPP specification may occur.

## 3.3 ESD PROTECTION

**Table 3-3 : Maximum ESD Rating**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| All Pins (Contact Discharge) | | | ±2 | kV |
| All Pins (Air Discharge) | | | ±4 | kV |

- The module is sensitive to ESD. Require special precautions when handling.

## 3.4 RECOMMENDED OPERATION RATING

### *3.4.1 Power Supply*

**Table 3-4 : DC Characteristics of Power Supply**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| VBAT_PA/VBAT_BB | 2.1 | 3.3 | 3.6 | V |
| VBATSNS | 0 | - | 5.2 | V |
| VDD18_OUT | 1.7 | 1.8 | 1.9 | V |
| VUSB | 3.2 | 3.3 | 3.4 | V |
| USIM_VDD (1.8V) | 1.7 | 1.8 | 1.9 | V |
| USIM_VDD (3.0V) | 2.9 | 3.0. | 3.1 | V |

### *3.4.2 UART Interface*

**Table 3-5 : DC Characteristics of UART Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DVDDIO | Power Domain | | 1.8 | | V |
| VOH | High Level Output | 0.85*DVDDIO | - | - | V |
| VOL | Low Level Output | - | - | 0.15*DVDDIO | V |
| VIH | High Level Input | 0.75*DVDDIO | - | DVDDIO | V |
| VIL | Low Level Input | 0 | - | 0.25*DVDDIO | V |
| IL | Leakage Current | -5 | | +5 | μA |

### 3.4.3 USIM Interface

**Table 3-6 : DC Characteristics of USIM Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| USIM_VDD | Power Domain | | 1.8/3.0 | | V |
| VOH | High Level Output | 0.85* USIM_VDD | - | - | V |
| VOL | Low Level Output | - | - | 0.15* USIM_VDD | V |
| VIH | High Level Input | 0.75* USIM_VDD | - | USIM_VDD | V |
| VIL | Low Level Input | 0 | - | 0.25* USIM_VDD | V |
| IL | Leakage Current | -5 | | +5 | μA |

### 3.4.4 USB Interface

**Table 3-7 : DC Characteristics of USB Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VUSB | Power Domain | | 3.3 | | V |
| VOH | High Level Output | 0.85* VUSB | - | 1.1* VUSB | V |
| VOL | Low Level Output | 0 | - | 0.1* VUSB | V |
| VDI | Differential Input Sensitivity | 0.2 | - | - | V |
| VCM | Differential Common Mode Range | 0.8 | - | 2.5 | V |

### 3.4.5 SPI Interface

**Table 3-8 : DC Characteristics of SPI Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DVDDIO | Power Domain | | 1.8 | | V |
| VOH | High Level Output | 0.85*DVDDIO | - | - | V |
| VOL | Low Level Output | - | - | 0.15*DVDDIO | V |
| VIH | High Level Input | 0.75*DVDDIO | - | DVDDIO | V |
| VIL | Low Level Input | 0 | - | 0.25*DVDDIO | V |
| IL | Leakage Current | -5 | | +5 | μA |

### 3.4.6 I2C Interface

**Table 3-9 : DC Characteristics of I2C Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DVDDIO | Power Domain | | 1.8 | | V |
| VOH | High Level Output | 0.85*DVDDIO | - | - | V |
| VOL | Low Level Output | - | - | 0.15*DVDDIO | V |
| VIH | High Level Input | 0.75*DVDDIO | - | DVDDIO | V |
| VIL | Low Level Input | 0 | - | 0.25*DVDDIO | V |
| IL | Leakage Current | -5 | | +5 | μA |

### 3.4.7 System Control Interface

**Table 3-10 : DC Characteristics of System Control Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VBAT | Power Domain | 2.1 | 3.3 | 3.6 | V |
| VOH | High Level Output | 0.85*VBAT | - | - | V |
| VOL | Low Level Output | - | - | 0.15*VBAT | V |
| VIH | High Level Input | 0.75*DVDDIO | - | VBAT | V |
| VIL | Low Level Input | 0 | - | 0.25*VBAT | V |
| IL | Leakage Current | -5 | | +5 | μA |

### 3.4.8 GPIO Interface

**Table 3-11 : DC Characteristics of GPIO Interface**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DVDDIO | Power Domain | | 1.8 | | V |
| VOH | High Level Output | 0.85*DVDDIO | - | - | V |
| VOL | Low Level Output | - | - | 0.15*DVDDIO | V |
| VIH | High Level Input | 0.75*DVDDIO | - | DVDDIO | V |
| VIL | Low Level Input | 0 | - | 0.25*DVDDIO | V |
| IL | Leakage Current | -5 | | +5 | μA |

## 3.5 CURRENT CONSUMPTION

The supply current for various modes with operation at 25℃ and VBAT = 3.3V.

**Table 3-12 : Current Consumption @ 3.3V**

| Operating Mode | Description | | Typ. | Unit |
|---|---|---|---|---|
| OFF | Leakage current | | 2.5 | μA |
| PSM | PSM supply current | | 3.5 | μA |
| eDRX | PTW=10.24s, eDRX=81.92s, DRX=2.56s | | 146 | μA |
| | PTW=10.24s, eDRX=163.84s, DRX=1.28s | | 83 | μA |
| | PTW=20.48s, eDRX=163.84s, DRX=2.56s | | 120 | μA |
| | PTW=40.96s, eDRX=327.68s, DRX=2.56s | | 116 | μA |
| Idle | Idle Mode | | 0.8 | mA |
| Active | B1 | Transmit at 23dBm | 140 | mA |
| | | Transmit at 10dBm | 40 | |
| | | Transmit at 0dBm | 25 | |
| | B3 | Transmit at 23dBm | 115 | mA |
| | | Transmit at 10dBm | 40 | |
| | | Transmit at 0dBm | 25 | |
| | B5 | Transmit at 23dBm | 115 | mA |
| | | Transmit at 10dBm | 40 | |
| | | Transmit at 0dBm | 30 | |
| | B8 | Transmit at 23dBm | 140 | mA |
| | | Transmit at 10dBm | 40 | |
| | | Transmit at 0dBm | 30 | |
| | B20 | Transmit at 23dBm | 115 | mA |
| | | Transmit at 10dBm | 40 | |
| | | Transmit at 0dBm | 30 | |
| | B28 | Transmit at 23dBm | 115 | mA |
| | | Transmit at 10dBm | 35 | |
| | | Transmit at 0dBm | 25 | |
| | B1/B3/B5/B8 B20/B28 | Receive | 18 | mA |

# 4 RF SPECIFICATION

## 4.1 TRANSMITTER OUTPUT POWER

**Table 4-1 : Transmitter Output Power**

| Band | Max. | Min. |
|---|---|---|
| B1 | 23dBm±2dB | < -40dBm |
| B3 | 23dBm±2dB | < -40dBm |
| B5 | 23dBm±2dB | < -40dBm |
| B8 | 23dBm±2dB | < -40dBm |
| B20 | 23dBm±2dB | < -40dBm |
| B28 | 23dBm±2dB | < -40dBm |

**Table 4-2 : Maximum Power Reduction (MPR) for Power Class 3**

| Tones | Allocation | Modulation | MPR (dB) |
|---|---|---|---|
| 3 | 0 - 2 | QPSK | ≤ 0.5 |
| 3 | 3 – 5 | QPSK | 0 |
| 3 | 6 – 7 | QPSK | 0 |
| 3 | 9 - 11 | QPSK | ≤ 0.5 |
| 6 | 0 - 5 | QPSK | ≤ 1.0 |
| 6 | 6 - 11 | QPSK | ≤ 1.0 |
| 12 | 0 - 11 | QPSK | ≤ 2.0 |

## 4.2 RECEIVER SENSITIVITY

**Table 4-3 : Receiver Sensitivity**

| Band | Condition | Typ. |
|---|---|---|
| | MCS-1, 95% Throughput with Repetitions | -131dBm±1dB |
| B3 | | -131dBm±1dB |
| B5 | | -131dBm±1dB |

| | | |
|---|---|---|
| B8 | | -131dBm±1dB |
| B20 | | -131dBm±1dB |
| B28 | | -131dBm±1dB |

## 4.3 GNSS SPECIFICATION

**Table 4-4 : Electrical Characteristics of GNSS**

| Parameter | GPS | Beidou | GLONASS |
|---|---|---|---|
| Acquisition Sensitivity | -147dBm | -145dBm | -145dBm |
| Tracking Sensitivity | -160dBm | -160dBm | -159dBm |
| TTFF (Cold Start) | < 30sec | | |
| TTFF (Hot Start) | < 1sec | | |
| PPP | < 2.0m CEP | | |
| D-GNSS | < 1.0m CEP | | |
| Speed Accuracy | 0.1m/s | | |

## 4.4 ANTENNA REQUIREMENT

The antenna is the most critical component, and depending on the design and application of the terminal device. There are different antenna types. The following antenna requirements, external antenna is used as reference for LTE antenna, patch antenna is used as reference for GNSS antenna.

**Table 4-5 : LTE Antenna Requirement**

| Parameter | | Requirement | Unit |
|---|---|---|---|
| Frequency Range | Low Band | 703 ~ 960 | MHz |
| | High Band | 1710 ~ 2200 | |
| VSWR | | < 3 | |
| Antenna Efficiency | | 50 | % |
| Polarization | | Linear | |
| Radiation Pattern | | Omni-directional | |
| Input Impedance | | 50 | Ω |

**Table 4-6 : GNSS Antenna Requirement**

| Parameter | GPS L1 | Beidou B1 | GLONASS G1 | Unit |
|---|---|---|---|---|
| Frequency Range | 1575.42 +/- 1.023 | 1561.098 +/- 2.046 | 1602.5625 +/- 4 | MHz |
| VSWR | < 2 | | | |
| Axial Ratio | < 3 | | | dB |
| Peak Gain | > 3 | | | dBi |
| Antenna Efficiency | > 70 | | | % |
| Polarization | RHCP | | | |
| Radiation Pattern | Omni-directional | | | |
| Input Impedance | 50 | | | Ω |

# 5 DESIGN RECOMMENDATION

## 5.1 APPLICATION CIRCUIT OF BATTERY OPERATION

EZ2625 series module is suitable for the operation of different battery types, such as Li-ion battery, Li-MnO2 battery, Alkaline Battery and so on. To meet the operation of different battery types, an external power circuit, like bulk or boost converter is needed to output a specific voltage level for powering the module.

### *5.1.1 Li-ion Battery for EZ2625*

When using Li-ion battery as power source (VBAT_IN), an external buck converter circuit is required. The reference design of external buck converter circuit is shown in the figure below. In addition, a TVS diode close to battery connector, power switch or USB connector is recommended for ESD protection.

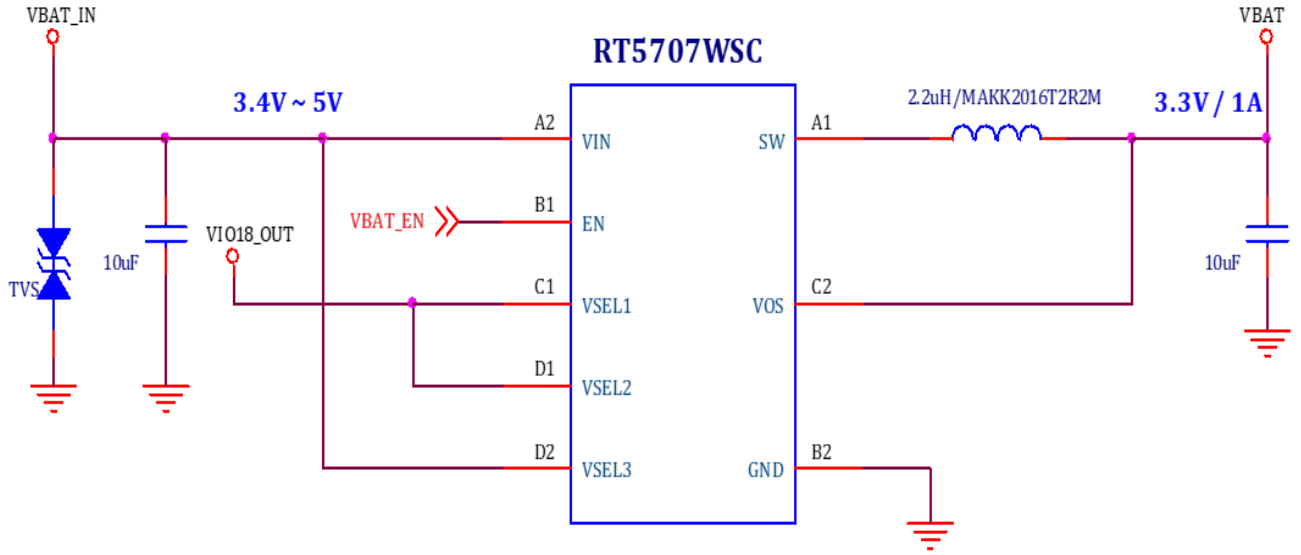



**Figure 5-1 : Reference Design of External Buck Converter**

### *5.1.2 Li-MnO2 or 2S Alkaline Battery for EZ2625*

When using Li-MnO2 or 2S Alkaline battery as power source (VBAT_IN), an external boost converter circuit is required or not depending on the USIM types.

- Using 1.8V USIM: No need to add an external boost converter circuit
- Using 3V USIM: Need to add an external boost converter circuit. The reference design is shown in the figure below. In addition, a TVS diode close to battery connector, power switch or USB connector is recommended for ESD protection.

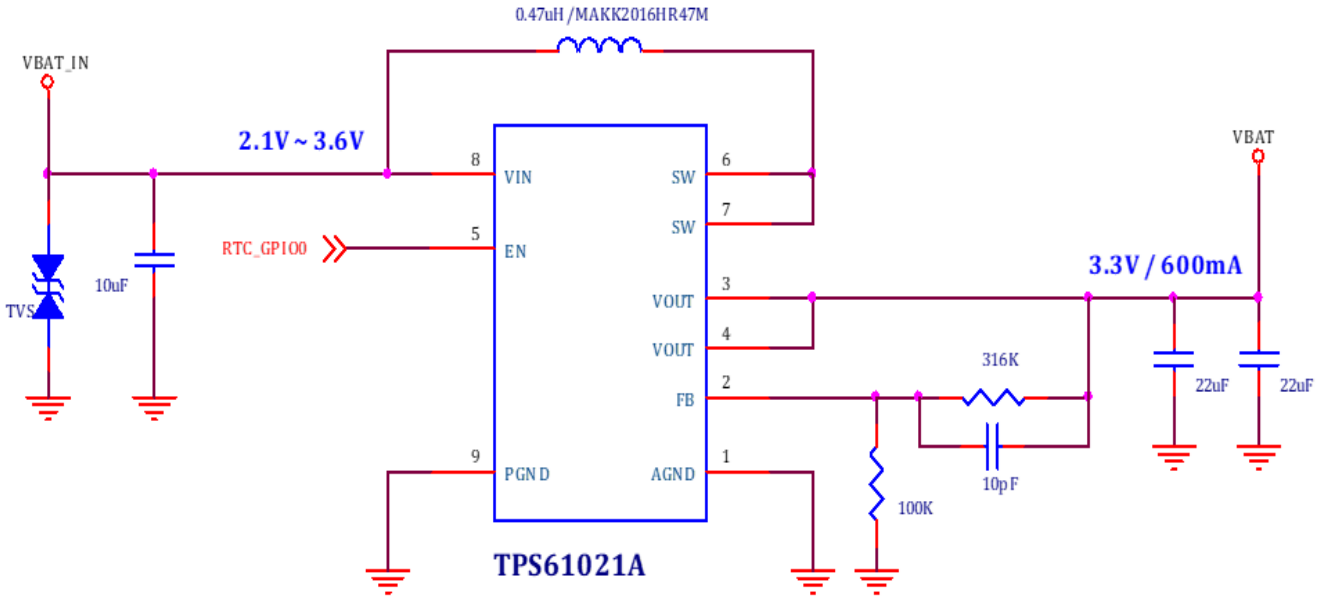



**Figure 5-2 : Reference Design of External Boost Converter**

## 5.2 POWER SUPPLY

EZ2625 series module is powered via VBAT_PA and VBAT_BB pins. The voltage ranges from 2.1 ~ 3.6V with a typical 3.3V operation and is required at least 0.5A current capability. In addition, the module has a LDO power output named as VDD18_OUT. The output voltage is 1.8V.

**Table 5-1 : Power Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| VBATSNS | 15 | Battery sensing input. The maximum input voltage is 5.2V |
| VBAT_PA | 16 | Voltage range is 2.1V-3.6V, typically 3.3V. Supply VBAT_PA with 3.3V-3.6V if 3V USIM is required. |
| VBAT_BB | 17 | Voltage range is 2.1V-3.6V, typically 3.3V. |
| VDD18_OUT | 13 | 1.8V power supply output for external circuit. Leave it open if not used. |
| GND | 14,18,35,36,38, 39,46,48 | Ground connection |

To avoid the voltage drop caused by peak current and lower the radio interference from a given circuit, it is recommended to have the following suggestions.

- A 100uF Tantalum capacitor with low ESR is recommended.
- Add 33pF、0.1uF、10uF decoupling capacitors as close as possible to VBAT_PA and VBAT_BB pins from small capacitance to large capacitance.
- Add a TVS diode for ESD protection.

- Keep VBAT trace as wider as possible.

### *5.2.1 Power Supply by Using Li-ion Battery*

The reference design of power supply circuit is shown in the figure below. Refer to the Figure 5-1 for the connections between VBAT_PA / VBAT_BB / VBATSNS and VBAT / VBAT_IN.

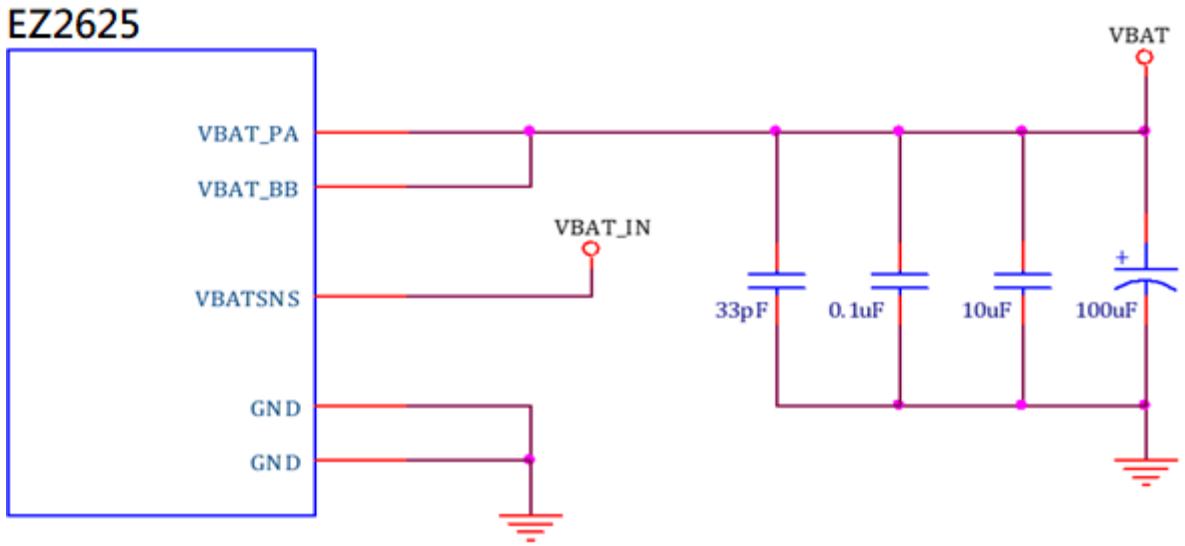



**Figure 5-3 : Power Supply with Li-ion battery and 1.8V/3V USIM**

### *5.2.2 Power Supply by Using Li-MnO2 or 2S Alkaline Battery (1.8V USIM)*

Connect VBAT_PA, VBAT_BB and VBATSNS pins with the positive terminal of battery directly when using 1.8V USIM. The reference design of power supply circuit is shown in the figure below.

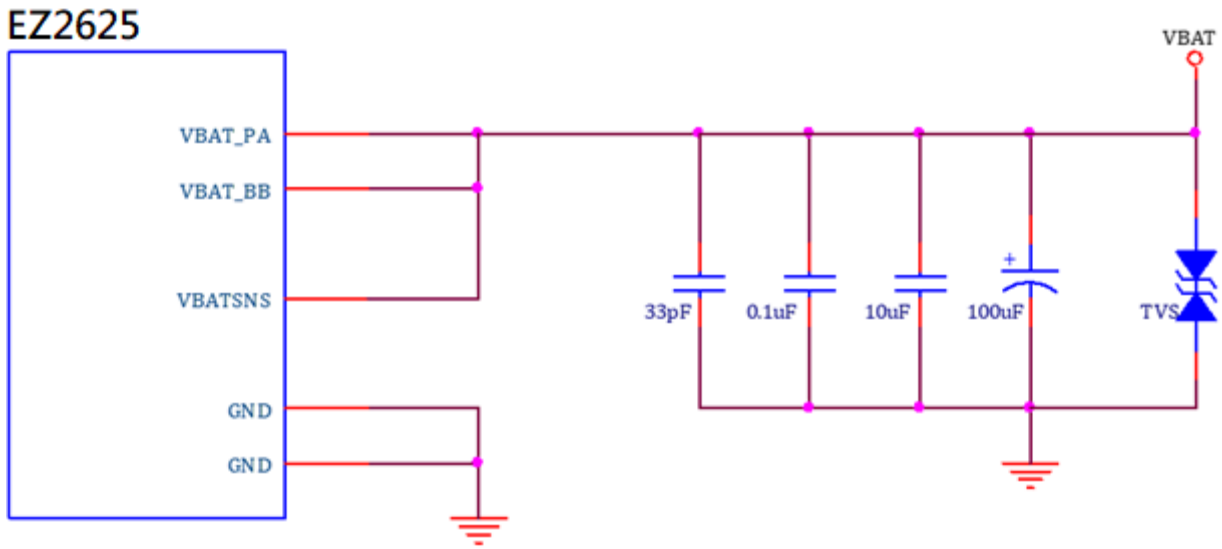



**Figure 5-4 : Power Supply with Li-MnO2/2S Alkaline Battery and 1 .8V USIM**

### *5.2.3 Power Supply by Using Li-MnO2 or 2S Alkaline Battery (3V USIM)*

Supply VBAT_PP with 3.3V-3.6V when using 3V USIM. The reference design of power supply circuit is shown in the figure below. Refer to the Figure 5-2 for the connections between VBAT_PA / VBAT_BB / VBATSNS and VBAT / VBAT_IN.

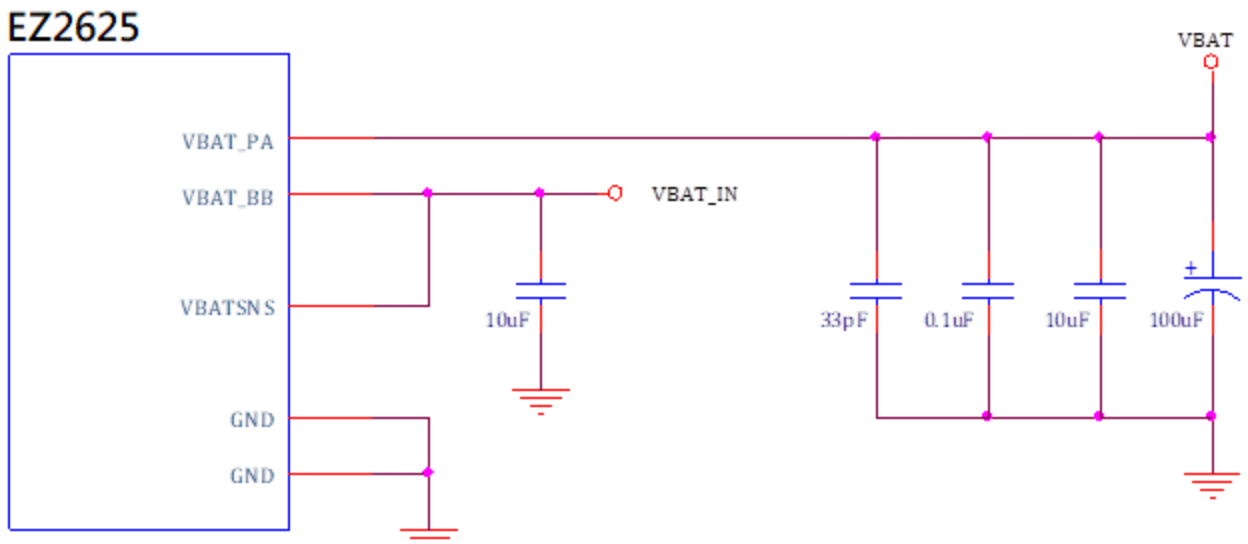



**Figure 5-5 : Power Supply with Li-MnO2/2S Alkaline Battery and 3V USIM**

## 5.3 UART INTERFACE

EZ2625 series module features two UART interfaces for communication. UART1 is main port used for sending AT command and data transmission. UART0 is debug port used for collecting debugging and upgrade firmware. Support baud rates from 9600 to 921600bps.

**Table 5-2 : UART Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| UART1_CTS | 1 | 1.8V power domain.<br>Used for AT command and data transmission.<br>Default baud rate is 115200bps |
| UART1_RTS | 2 | |
| UART1_TXD | 3 | |
| UART1_RXD | 4 | |
| UART0_TXD | 40 | 1.8V power domain.<br>Used for debug and upgrade firmware.<br>Default baud rate is 115200bps |
| UART0_RXD | 41 | |

The connections between the module (DCE, Data Communication Equipment) and application processor (DTE, Data Terminal Equipment) are illustrated in the figures below. It is recommended to have the following suggestions.

- Note that the UART logic level in circuit design.
- Note that the UART connections between EZ2625 and application processor.
- Add 0Ω resistors and test points for the consideration of signal integrity.
- Recommend to reserve test point.

### *5.3.1 Application of 2-Wire UART Main Port*

- If 1.8V application processor is used, the circuit is illustrated in the figure below.

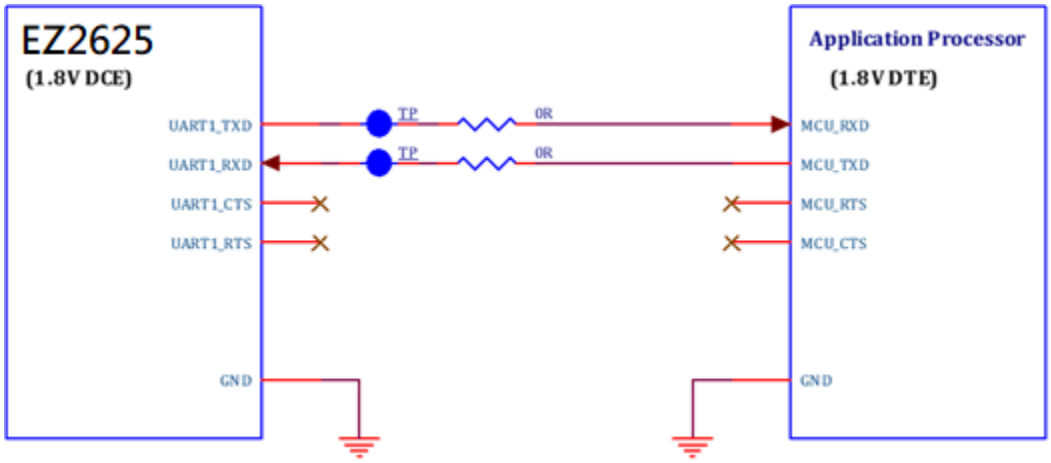



**Figure 5-6 : Application Circuit with 2-Wire UART and 1.8V DTE**

- If 3.3V application processor is used, the level shifter circuit is required for voltage-level matching. A bidirectional voltage-level translator (TXB0102DCUR) is recommended. The circuit is illustrated in the figure below.

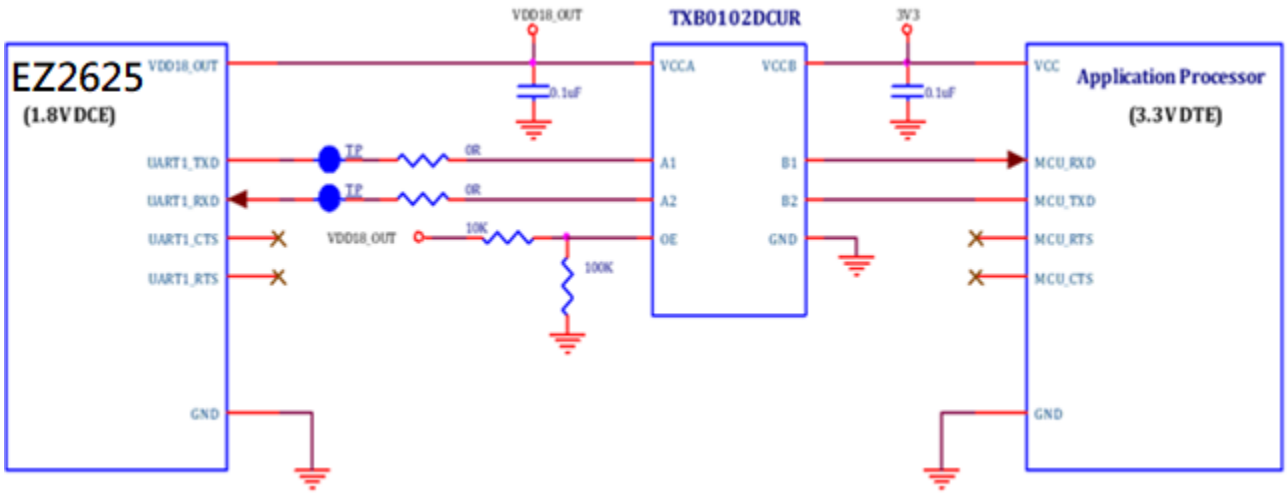



**Figure 5-7 : Application Circuit with 2-Wire UART and 3.3V DTE**

### 5.3.2 Application of 4-Wire UART Main Port

- If 1.8V application processor is used, the circuit is illustrated in the figure below.

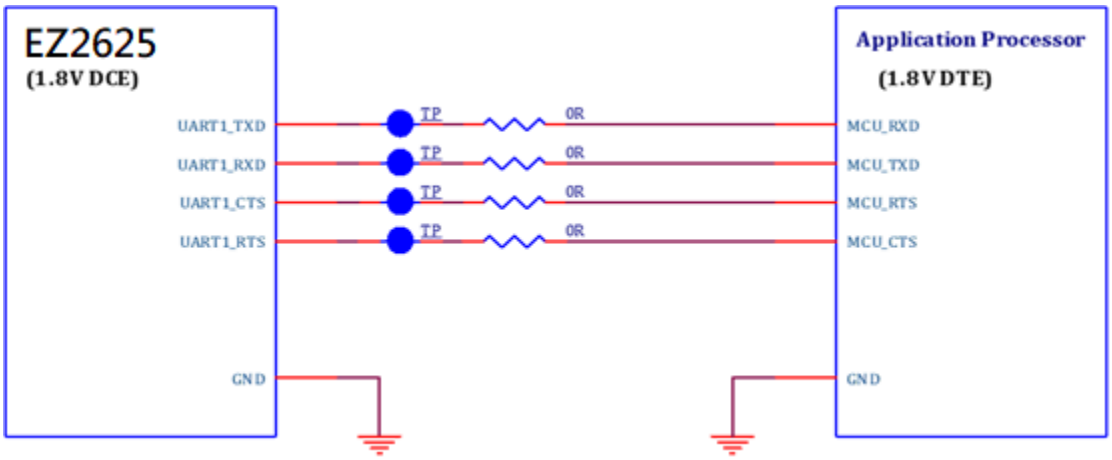



**Figure 5-8 : Application Circuit with 4-Wire UART and 1.8V DTE**

- If 3.3V application processor is used, the level shifter circuit is required for voltage-level matching. A bidirectional voltage-level translator (TXB0104PWR) is recommended. The circuit is illustrated in the figure below.

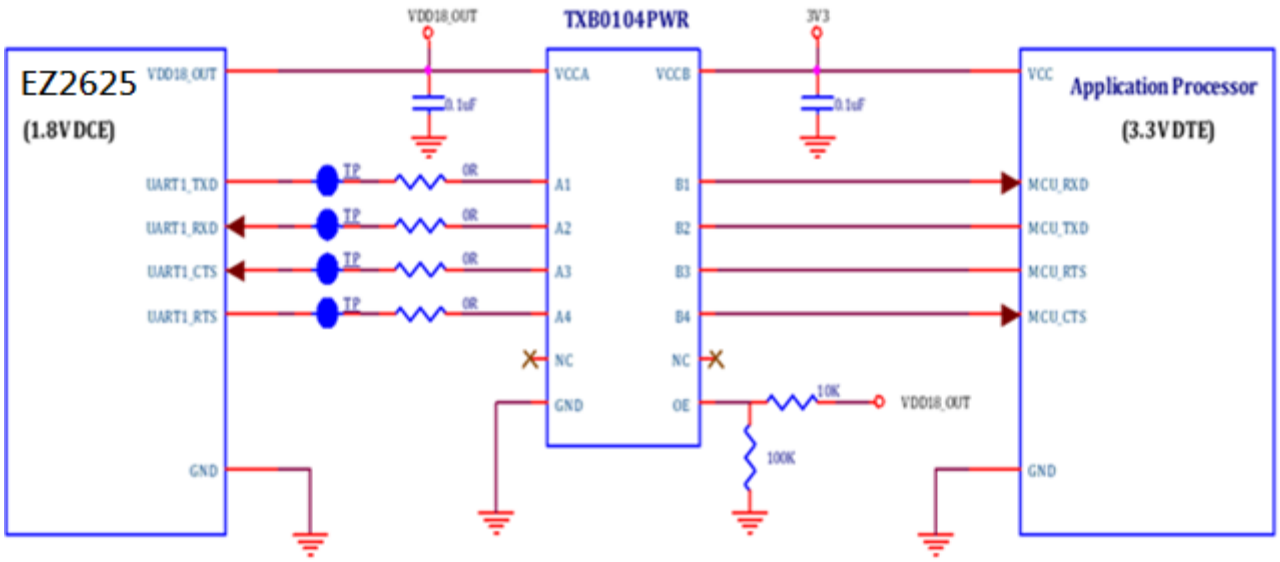



**Figure 5-9 : Application Circuit with 4-Wire UART and 3.3V DTE**

### 5.3.3 Application of UART Debug Port

UART debug port (UART0) is used for debugging and firmware upgrade. It is recommended to reserve test points or pin header for application.

## 5.4 USIM INTERFACE

EZ2625-A01 and EZ2625-E01 feature one e-SIM chip inside the module. EZ2625-G01 and EZ2625-L01 feature one USIM card interface compatible with the ISO/IEC 7816-3 standard. The USIM interface is powered by USIM_VDD. It is 3.0V or 1.8V typically.

**Table 5-3 : USIM Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| eSIM_RST | 21 | - EZ2625-A01: Connect with USIM_RST<br>- EZ2625-E01: Connect with USIM_RST<br>- EZ2625-G01: Keep it open<br>- EZ2625-L01: Keep it open |
| USIM_DAT | 22 | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |
| USIM_CLK | 23 | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |
| USIM_RST | 24 | Connect with a TVS diode for ESD protection<br>- EZ2625-A01: Connect with eSIM_RST<br>- EZ2625-E01: Connect with eSIM_RST |
| USIM_VDD | 25 | 1.8V or 3V power domain, depending on VBAT_PA. Connect with a TVS diode for ESD protection.<br>- EZ2625-A01: Connect with 0.1uF decoupling capacitor<br>- EZ2625-E01: Connect with 0.1uF decoupling capacitor |
| USIM_DET | 26 | If used, pull up to VDD18_OUT with 10Kohm.<br>- EZ2625-A01: Keep it open<br>- EZ2625-E01: Keep it open |

For EZ2625-A01 and EZ2625-E01, it is required to have the following suggestions.
- eSIM_RST and USIM_RST have to be connected.
- Add a 0.1uF decoupling capacitor as close as possible to USIM_VDD.

For EZ2625-G01 and EZ2625-L01, it is recommended to have the following suggestions.
- Place USIM card holder close to the module and keep signal trace length less than 50mm.
- Keep the signal traces of USIM socket as far away from any RF trace and VBAT
- Keep 3W spacing rule and use ground or guard traces between USIM_CLK and USIM_DAT to minimize cross talk.
- Add TVS diodes for ESD protection and place it as close as possible to USIM socket.
- Add 22Ω resistors in series connection between the module and USIM socket for signal integrity.
- Add 22pF capacitors and place it as close as to USIM socket for reducing EMI.

- Add a 20KΩ pull-up resistor between USIM_DAT and USIM_VDD to enhance USIM stability.
- If USIM_DET is used, it is required to pull up to VDD18_OUT with a 10KΩ resistor.

### *5.4.1 Application of Internal e-SIM Chip*

- If EZ2625-A01 or EZ2625-E01 is used, the application circuit is illustrated in the figure below.

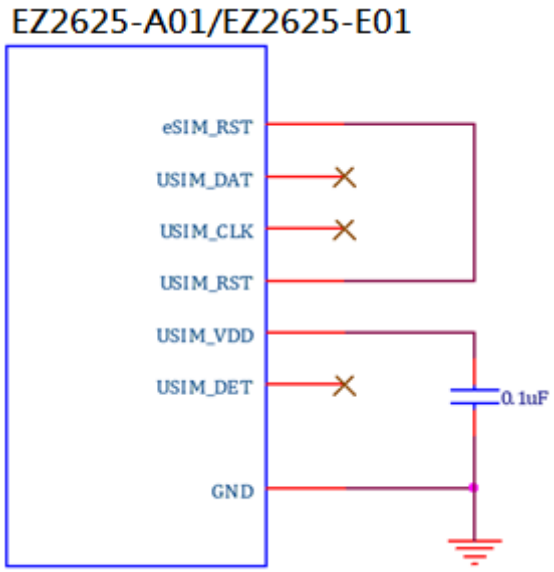



**Figure 5-10 : Application Circuit of Internal e-SIM Chip**

### *5.4.2 Application of External USIM Socket*

- If EZ2625-G01 or EZ2625-L01 is used, the application circuit is illustrated in the figure below.

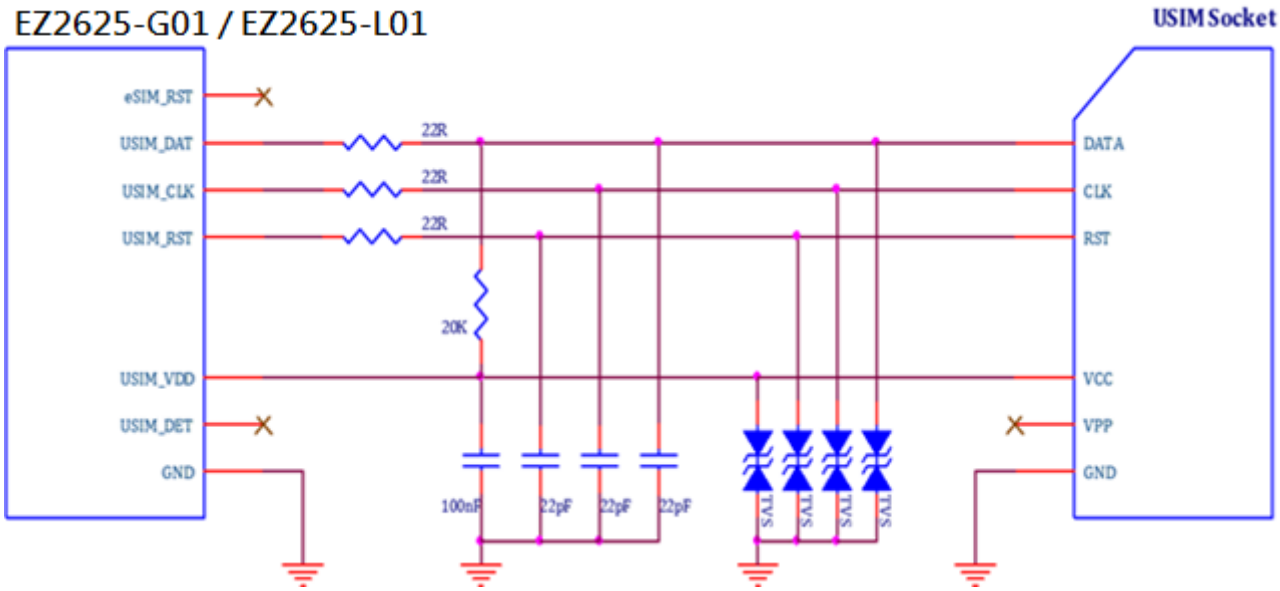



**Figure 5-11 : Application Circuit of External USIM Socket**

### *5.4.3 SIM Card Holder*

It is recommended to have the 6-pin SIM socket for design application. A Nano-SIM card holder, 693043020611 produced by Wurth Electronics is given for reference.

**Table 5-4 : Pin Definition of Nano-SIM Card Holder**

| Pin Name | Pin No. | Comment |
|---|---|---|
| VCC | C1 | Supply voltage. Connect to USIM_VDD. |
| RST | C2 | Reset signal. Connect to USIM_RST. |
| CLK | C3 | Clock signal. Connect to USIM_RCLK |
| GND | C4 | Connect to ground |
| VPP | C5 | Keep it open |
| I/O | C6 | Data signal. Connect to USIM_DAT |

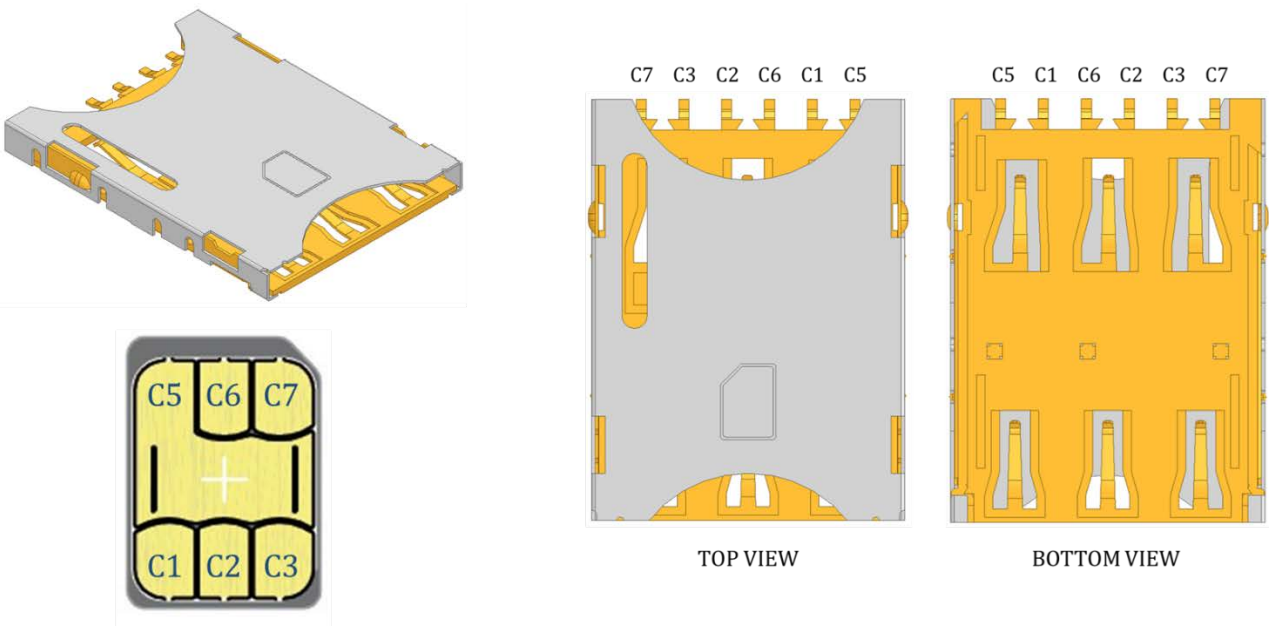



**Figure 5-12 : An Example of Nano-SIM Card Holder**

## 5.5 USB INTERFACE

EZ2625 series module features one USB interface compliant with USB1.1 specification. It is mainly used to capture debug log. There will be 2 virtual port, debug and modem port after installing USB driver. Contact Connegence support team for more details.

**Table 5-5 : USB Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| VUSB | 27 | 3.3V USB power supply input. |
| USB_DM | 28 | USB data line D-.<br>90ohm differential impedance is required. |
| USB_DP | 29 | USB data line D+.<br>90ohm differential impedance is required. |
| USB_DL | 30 | USB download mode selection. Leave it open if not used. |

The application circuit is illustrated in the figures below. It is recommended to have the following suggestions.

- Add TVS diodes for ESD protection and place it as close as possible to USB connector. The maximum junction capacitance of TVS must be less than 2pF for ESD protection.
- Add 0Ω resistors in series connection with D+ and D- for the consideration of signal integrity.
- Route D+ and D- as 90 ohm differential pair.
- Provide a good return path (ground) for current. Do not route over a gap in the reference plane.
- Route D+ and D- on the top as short as reasonably possible and length mismatch must not exceed 50 mil.
- Keep USB trace as far away from any susceptible trace, such as clock trace, high speed trace and noisy power traces.
- If not used, it is strongly recommend to reserve test point or pin header.

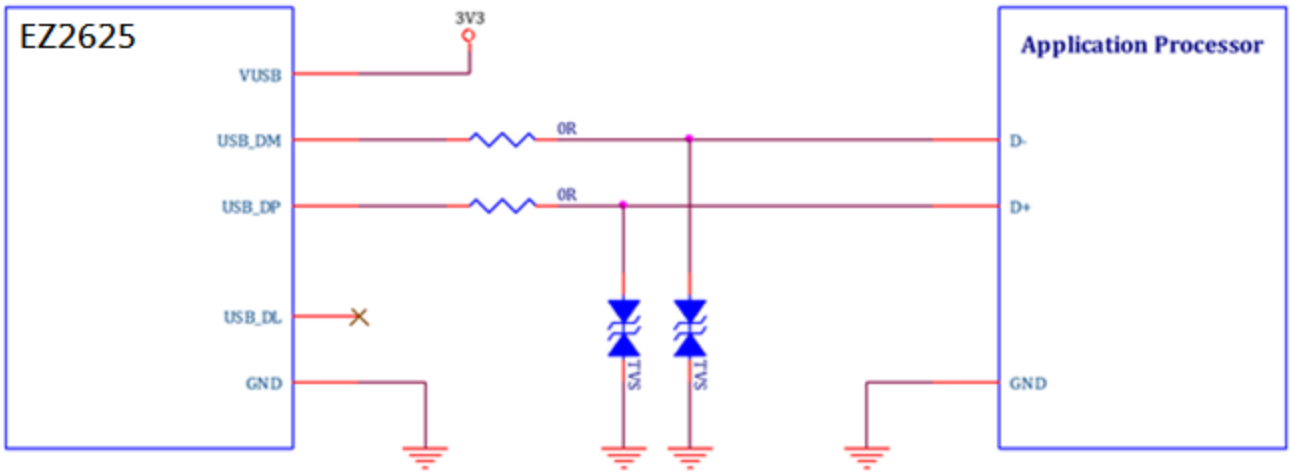



**Figure 5-13 : Application Circuit of USB Interface**

## 5.6 SPI INTERFACE

EZ2625 series module feature one SPI slave controller to receive and transmit device data using single and dual SPI protocol. The SPI controller can communicate at up to 52Mbps.

**Table 5-6 : SPI Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| SPI_CS | 49 | 1.8V power domain. Leave it open if not used. |
| SPI_MISO | 50 | 1.8V power domain. Leave it open if not used. |
| SPI_MOSI | 51 | 1.8V power domain. Leave it open if not used. |
| SPI_CLK | 52 | 1.8V power domain. Leave it open if not used. |

The application circuit is illustrated in the figure below. It is recommended to have the following suggestions.

- Note that the SPI logic level in circuit design.
- Keep 3W spacing rule between SPI_CLK and other signal to minimize cross talk.
- Avoid SPI_CLK crossing a split ground plane.
- Route SPI_CLK, SPI_MOSI, SPI_MISO with controlled impedance and identical length.
- Minimize the use of vias to reduce PCB trace impedance changes.

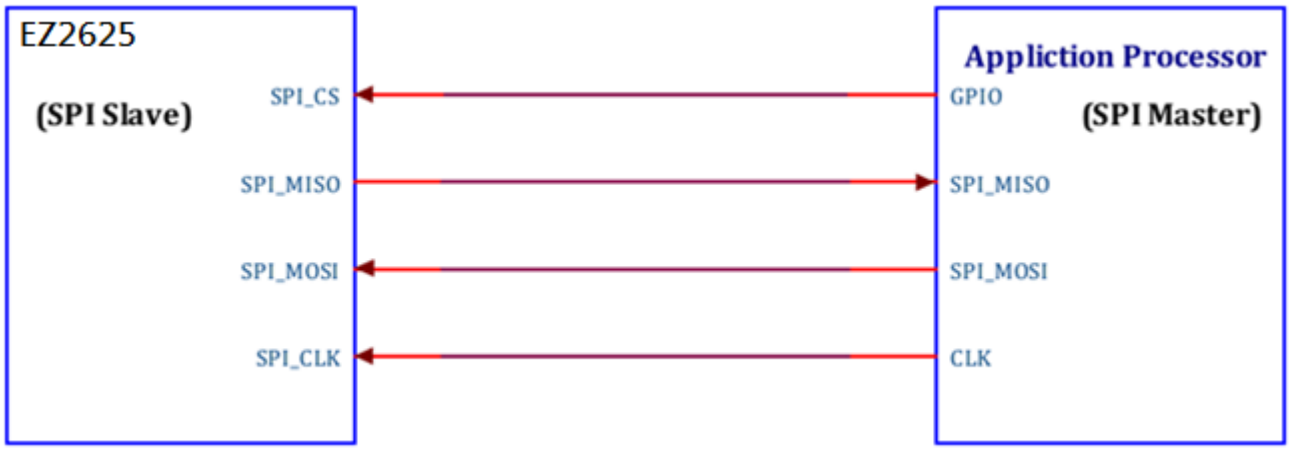



**Figure 5-14 : Application Circuit of SPI Interface**

## 5.7 I2C INTERFACE

EZ2625 series module feature one I2C master controller. There are three types of speed modes, including standard mode (100kbps), fast mode (400kbps) and high-speed mode (3.4Mbps).

**Table 5-7 : I2C Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| I2C_SCL | 42 | 1.8V power domain. Pull up to 1.8V with 2.2Kohm if used. Leave it open if not used. |
| I2C_SDA | 43 | 1.8V power domain. Pull up to 1.8V with 2.2Kohm if used. Leave it open if not used. |

The application circuit is illustrated in the figure below. It is recommended to have the following suggestions.

- Note that the I2C logic level in circuit design.
- Add a 2.2KΩ pull-up resistor to enhance I2C stability.
- Keep 3W spacing rule between I2C_SCL and other signal to minimize cross talk.
- Avoid I2C_SCL crossing a split ground plane.
- Route I2C_SDA and I2C_SCL with controlled impedance and identical length.

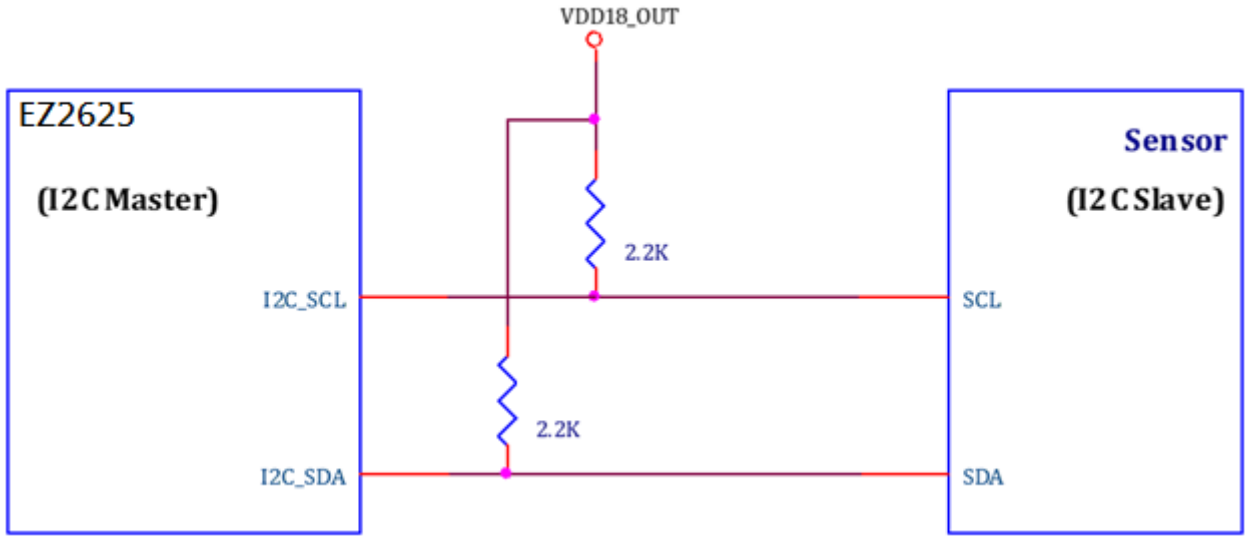



**Figure 5-15 : Application Circuit of I2C Interface**

## 5.8 ADC INTERFACE

EZ2625 series module features four channels of 10-bit ADC with maximum input voltage 1.4V for auxiliary analog function monitoring.

**Table 5-8 : ADC Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| ADC0 | 31 | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |
| ADC1 | 32 | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |

| | | |
|---|---|---|
| ADC2 | 33 | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |
| ADC3 | 34 | 1.8V power domain. 10-bit ADC. The maximum input voltage is 1.4V. Leave it open if not used. |

## 5.9 SYSTEM CONTROL

### *5.9.1 Power On / Power off*

EZ2625 series module is powered on/off via PWRKEY pin. It is equipped with an internal active pull-up resistor; an external pull-up resistor is not required.

**Table 5-9 : Power on/off Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| PWRKEY | 20 | VBAT power domain. Active low. Internal pull high with 40Kohm<br>- Power on: PWRKEY is keep low for 2 sec.<br>- Power off: PWRKEY is keep low for 8 sec (default). |

The application circuits are illustrated in the figure below. One is controlled by transistor circuit and another is controlled by a tact switch. It is recommended to have the following suggestions.

- Note that the logic level in circuit design.
- Add 0.1uF decoupling capacitor and a TVS diode for ESD protection

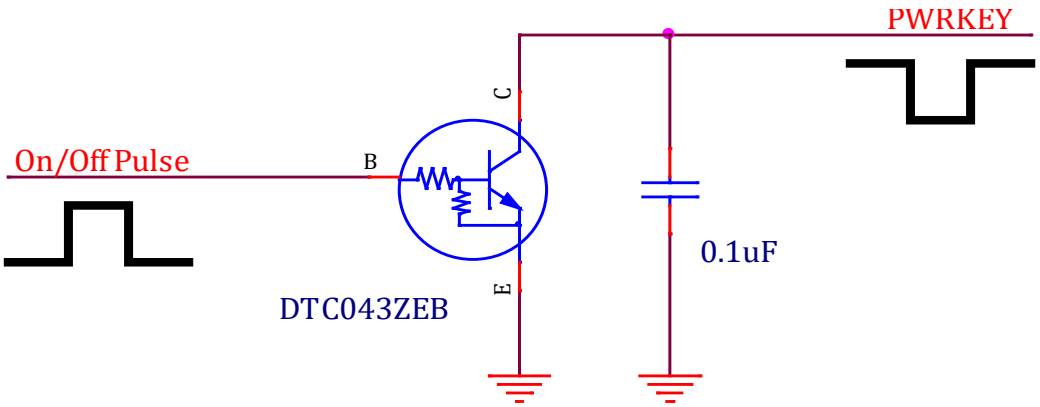



**Figure 5-16 : Power On/Off Circuit with Transistor**

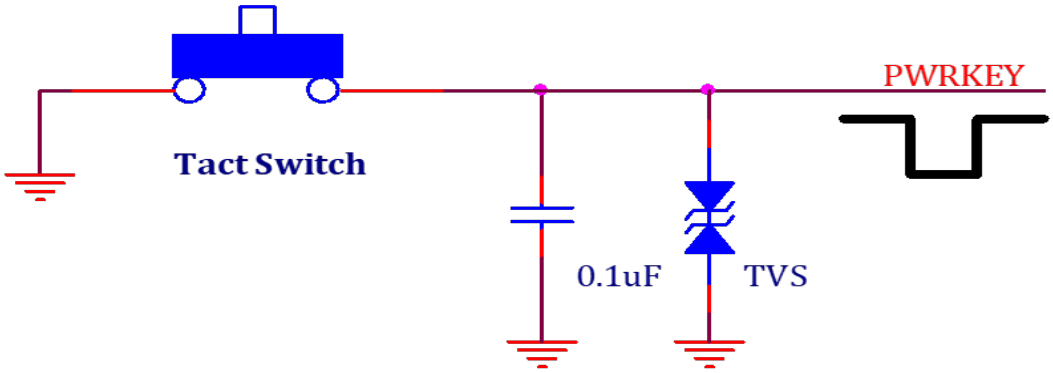



**Figure 5-17 : Power On/Off Circuit with Tact Switch**

The power on/off timing sequence is illustrated in the figure below.

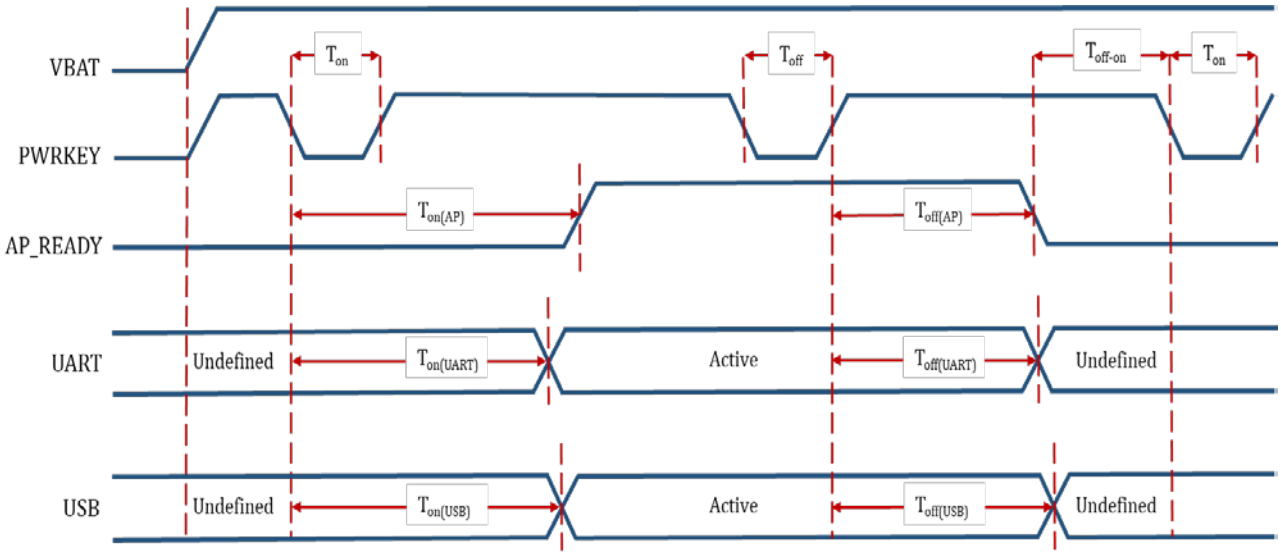



**Figure 5-18 : Power on/off Timing Sequence**

**Table 5-10 : Timing Sequence Parameters**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{on}$ | The time of power on the module | 240 | 800 | - | ms |
| $T_{on(AP)}$ | The time from power on to AP ready | - | 800 | - | ms |
| $T_{on(UART)}$ | The time from power on to UART interface ready | - | - | 1 | s |
| $T_{on(USB)}$ | The time from power on to USB interface ready | - | - | 1 | s |
| $T_{off}$ | The time of power off the module | 6 | 7 | 8 | s |
| $T_{off(AP)}$ | The time from power off to AP ready | - | - | 500 | ms |
| $T_{off(UART)}$ | The time from power off to UART | - | - | 1 | s |

| | | | | | |
|---|---|---|---|---|---|
| | interface ready | | | | |
| $T_{off(USB)}$ | The time from power off to USB interface ready | - | - | 1 | s |
| $T_{off-on}$ | The buffer time from power off to power on | 3 | - | - | s |

### *5.9.2 RESET*

EZ2625 series module can be reset by holding the RSTB pin low. The RSTB pin has an internal active pull-up resistor; an external pull-up resistor is not required. Note that the RSTB pin is ineffective in the power off mode.

**Table 5-11 : Reset Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| RESET | 19 | VBAT power domain. Active low. Internal pull high with 40Kohm. Reset time > 100ms |

The application circuits are illustrated in the figure below. One is controlled by transistor circuit and another is controlled by a tact switch. It is recommended to have the following suggestions.

- Note that the logic level in circuit design.
- Add 0.1uF decoupling capacitor and a TVS diode for ESD protection

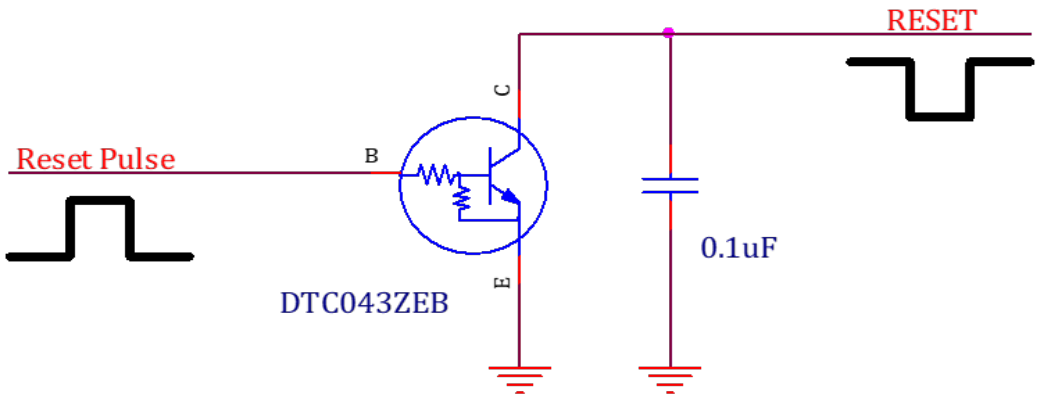



**Figure 5-19 : Reset Circuit with Transistor**

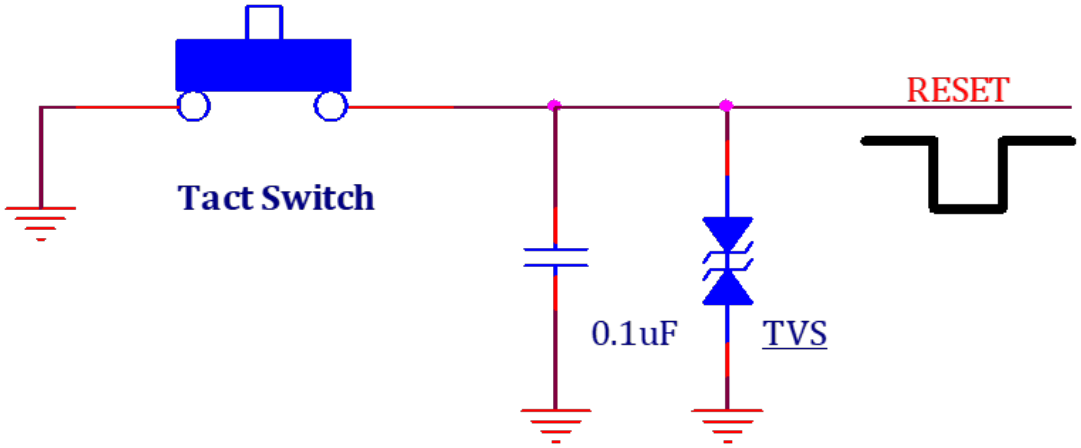



**Figure 5-20 : Reset Circuit with Tact Switch**

### *5.9.3 WAKEUP_IN*

EZ2625 series module can be waken up by external MCU through WAKEUP_IN pin. After the module enters the PSM mode, it can only wake up the module through PWRKEY or WAKEUP_IN event.

**Table 5-12 : WAKEUP_IN Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| WAKEUP_IN | 11 | VBAT power domain. Active low. It is the wake up source for exiting PSM. Pull up to VBAT with 10Kohm if used. |

The application circuit is illustrated in the figure below. Note that the logic level is used in circuit design.

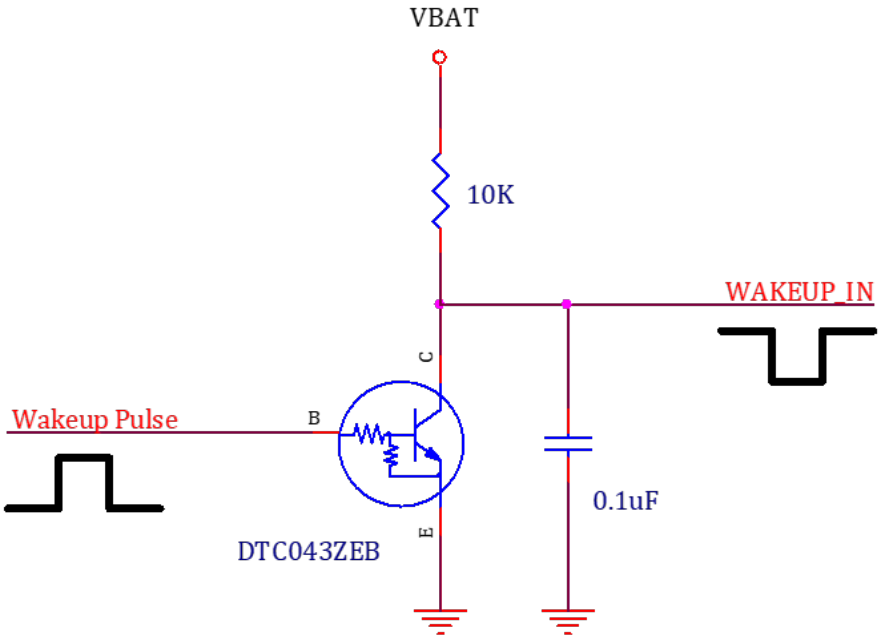



**Figure 5-21 : Application Circuit of WAKEUP_IN**

## 5.10 GPIO INTERFACE

### *5.10.1 WAKEUP_OUT*

EZ2625 series module has a WAKEUP_OUT pin to wake up the external MCU.

**Table 5-13 : WAKEUP_OUT Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| WAKEUP_OUT | 8 | 1.8V power domain. Leave it open if not used. |

### *5.10.2 SYS_STATUS*

EZ2625 series module has a SYS_STATUS pin to indicate the network status. The different blinking modes of the LED is indicated the different network status.

**Table 5-14 : SYS_STATUS Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| SYS_STATUS | 6 | 1.8V power domain. The indication of network status. Leave it open if not used.<br>LED blinking mode:<br>- Power OFF/PSM Mode: OFF |

| | | |
|---|---|---|
| | | - Search Network: 1Hz, 50% duty cycle.<br>- Register Network: 0.3Hz, 10% duty cycle.<br>- Data Transmit: 10Hz, 50% duty cycle. |

The application circuit is illustrated in the figure below. Note that it is not recommended to apply the LED indication circuit if low power consumption is concerned.

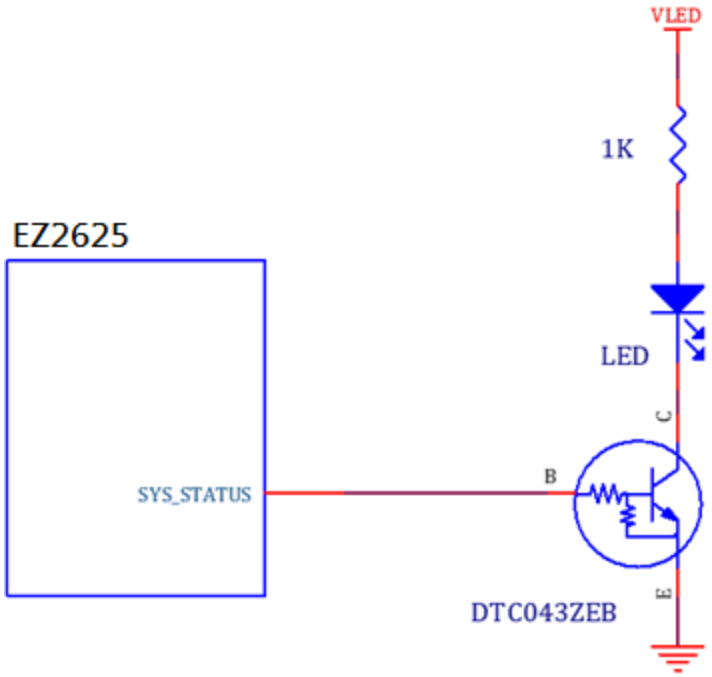



**Figure 5-22 : Application Circuit of SYS_STATUS**

### *5.10.3 GPIO*

EZ2625 series module has 5 GPIO pins for design application.

**Table 5-15 : GPIO Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| GPIO0 | 44 | 1.8V power domain. Leave it open if not used. |
| GPIO1 | 45 | |
| GPIO2 | 5 | |
| GPIO3 | 10 | |
| GPIO4 | 9 | |

## 5.11 RF INTERFACE

### *5.11.1 Antenna Interface*

EZ2625 series module has 2 RF interfaces for connecting the external or internal integrated antennas. One is MAIN_ANT pin connected to LTE antenna and another is GNSS_ANT connected to GNSS antenna. The MAIN_ANT and GNSS_ANT pins have a nominal characteristic impedance 50Ω and must be connected to the physical antenna through 50Ω transmission line.

**Table 5-16 : Antenna RF Interface**

| Pin Name | Pin No. | Comment |
|---|---|---|
| MAIN_ANT | 37 | 50Ω impedance control is required. Connect with a TVS diode for ESD protection |
| GNSS_ANT | 47 | 50Ω impedance control is required. Connect with a TVS diode for ESD protection.<br>- EZ2625-E01: Keep it open<br>- EZ2625-L01: Keep it open |

### *5.11.2 Antenna Design Guide*

The antenna is the most critical component and easily be influenced by surroundings, such as system ground plane, nearby components, mechanical parts, human or animal body. The application circuit is illustrated in the figure below. It is recommended to have the following suggestions.

- The RF signals should be routed using trace with a characteristic impedance of 50Ω. The 50Ω characteristic impedance can be calculated with a simulation tool, such as APPCAD.
- The RF trace between RF and antenna port should be as short and straight as possible.
- Place π-network mating circuit as close as possible to the antenna terminal.
- There should be a solid ground below RF trace. Do not route any signals under the RF trace.
- Keep RF trace as far away from any susceptible trace, such as clock trace, high speed trace and noisy power traces.
- Do not use right angles in the RF trace, it is better to use 45°bend or radius to change direction.
- In a good board design, drop as many ground vias as possible in the RF circuitry section.
- Add a ESD protection diode with ultra-low capacitance.

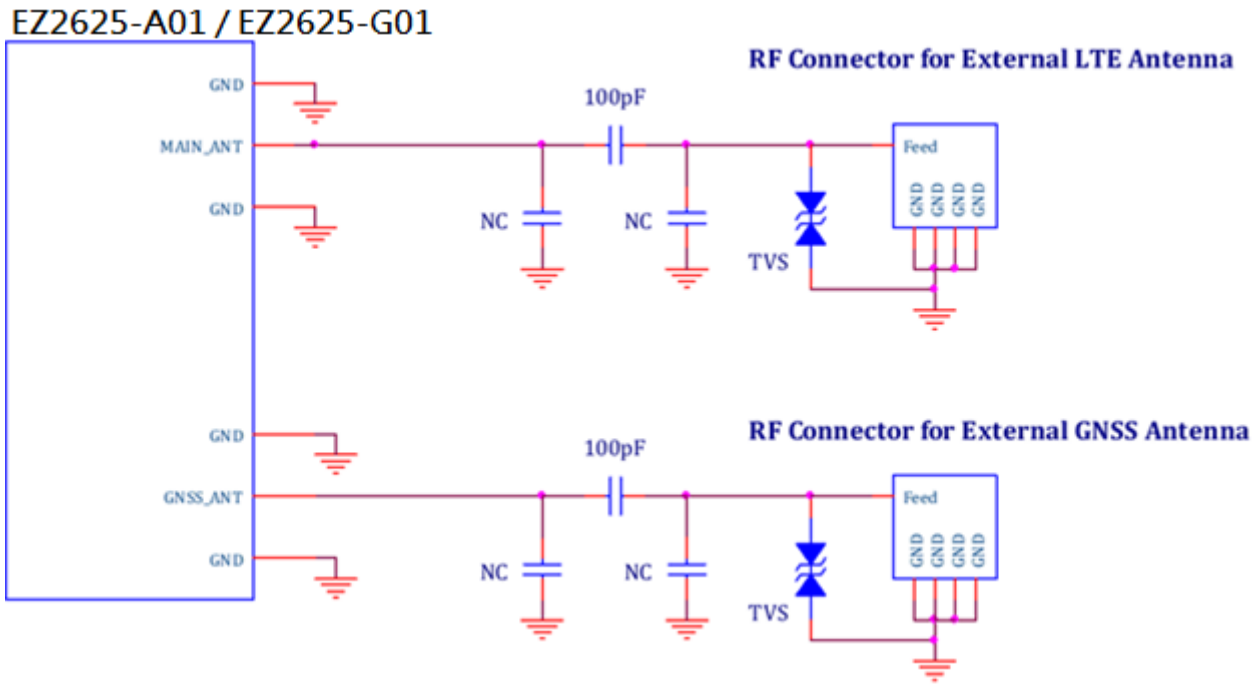



**Figure 5-23 : Application Circuit of Antenna RF Interface**

### *5.11.3 RF Transmission Line Design Guide*

Any RF transmission line must be designed with a characteristic impedance of 50Ω, such as the RF traces from MAIN_ANT pin to antenna connector or to internal integrated antenna. The 50Ω characteristic impedance can be calculated with a simulation tool, such as APPCAD from Agilent or Si9000 from Polar Instruments. An example of 4-layer PCB stack-up is illustrated in the figure below for design reference.

To achieve a 50Ω characteristic impedance, the width of RF transmission line must be chosen depending on:

- The dielectric thickness between the TOP layer implementing RF transmission line and L2 layer implementing reference ground plane. (e.g. H1=9mil in the Figure 5-24)
- The dielectric constant of dielectric material. (e.g. Er1=4.3 in the Figure 5-24)
- The dielectric constant of coating material. (e.g. CEr=4.0 in the Figure 5-24)
- The dielectric thickness of coating material. (e.g. C1=C2=C3=1mil in the Figure 5-24)
- The ground strip separation. (e.g. D1=20mil in the Figure 5-24)
- The copper thickness of the RF transmission line. (e.g. T1=1.4mil in the Figure 5-24)

| LAYER NO. | STRUCTURE | MATERIAL | THICKNESS (MIL) |
|---|---|---|---|
| | | SR | 1 |
| TOP | | COPPER | 1.4 |
| | | PREPREG | 9 |
| L2 | | COPPER | 1.4 |
| | | CORE | 35 |
| L3 | | COPPER | 1.4 |
| | | PREPREG | 9 |
| BOTTOM | | COPPER | 1.4 |
| | | SR | 1 |
| FINISHED THICKNESS | | | 60.6 |

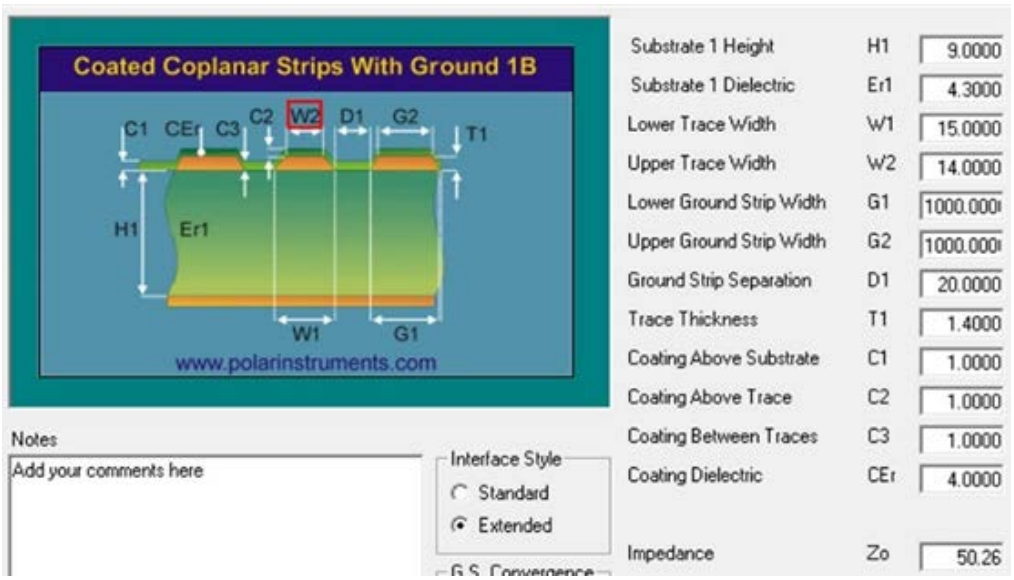



**Figure 5-24 : Example of 50Ω Transmission Line Design for 4-Layer PCB Stack-up**

# 6 MECHANICAL SPECIFICATIONS

## 6.1 PHYSICAL DIMENSIONS

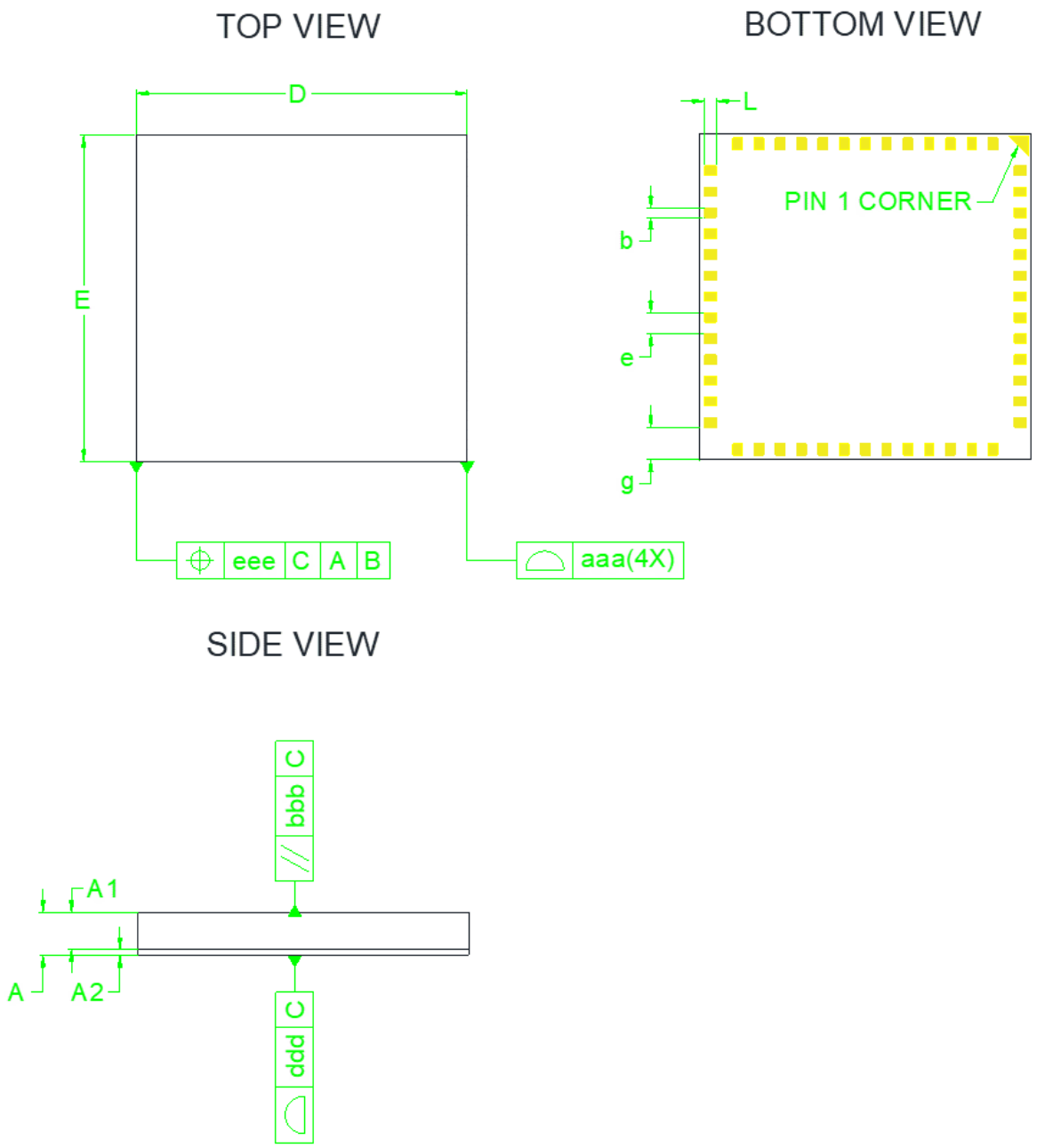



**Figure 6-1 : Module Mechanical Outline**

**Table 6-1 : Dimension of Mechanical Outline**

| Symbol | Dimension (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 1.80 | 1.85 | 1.90 |
| A1 | | 1.60 | |
| A2 | | 0.25 | |
| b | 0.35 | 0.40 | 0.45 |
| D | 13.90 | 14.00 | 14.10 |
| E | 13.90 | 14.00 | 14.10 |
| e | | 0.90 | |
| L | 0.45 | 0.50 | 0.55 |
| g | | 1.40 | |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ddd | | 0.10 | |
| eee | | 0.10 | |

## 6.2 MARKING INFORMATION


**Figure 6-2 : EZ2625 Markings**

**Table 6-2 : EZ2625 Markings**

| Marking | Description |
|---|---|
| EZ2625 | Model name |
| EZ2625-HLB-01 | Hardware version |
| 1850NT | Date code and manufacturer code |
| A01<br>G01<br>E01<br>L01 | Product identification |

# 7 REFERENCE PCB DESIGN

## 7.1 PCB LAND PATTERN DESIGN

**Unit: mm**

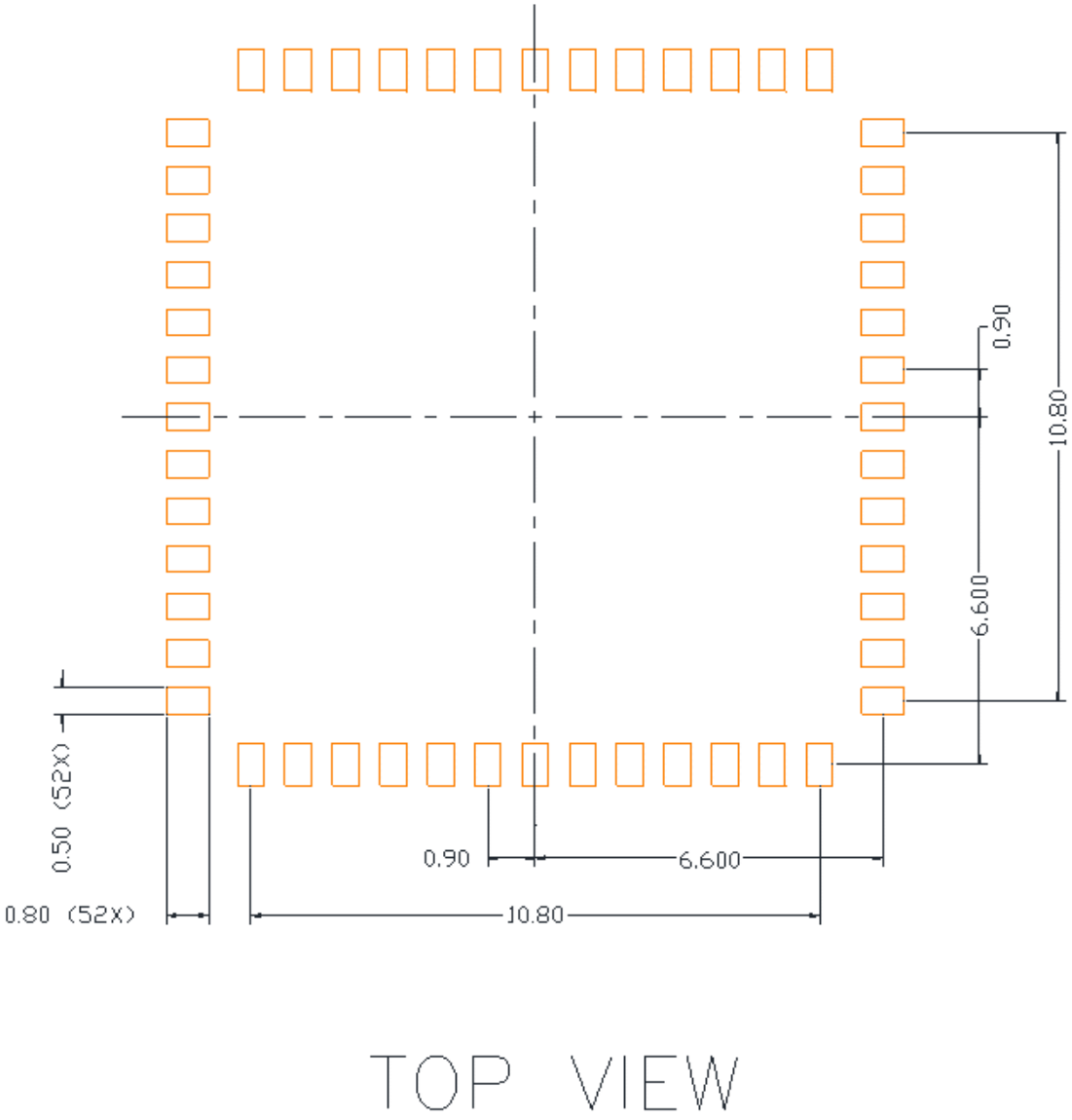



**Figure 7-1 : Recommended PCB Land Design**

## 7.2 SOLDER MASK DESIGN

**Unit: mm**

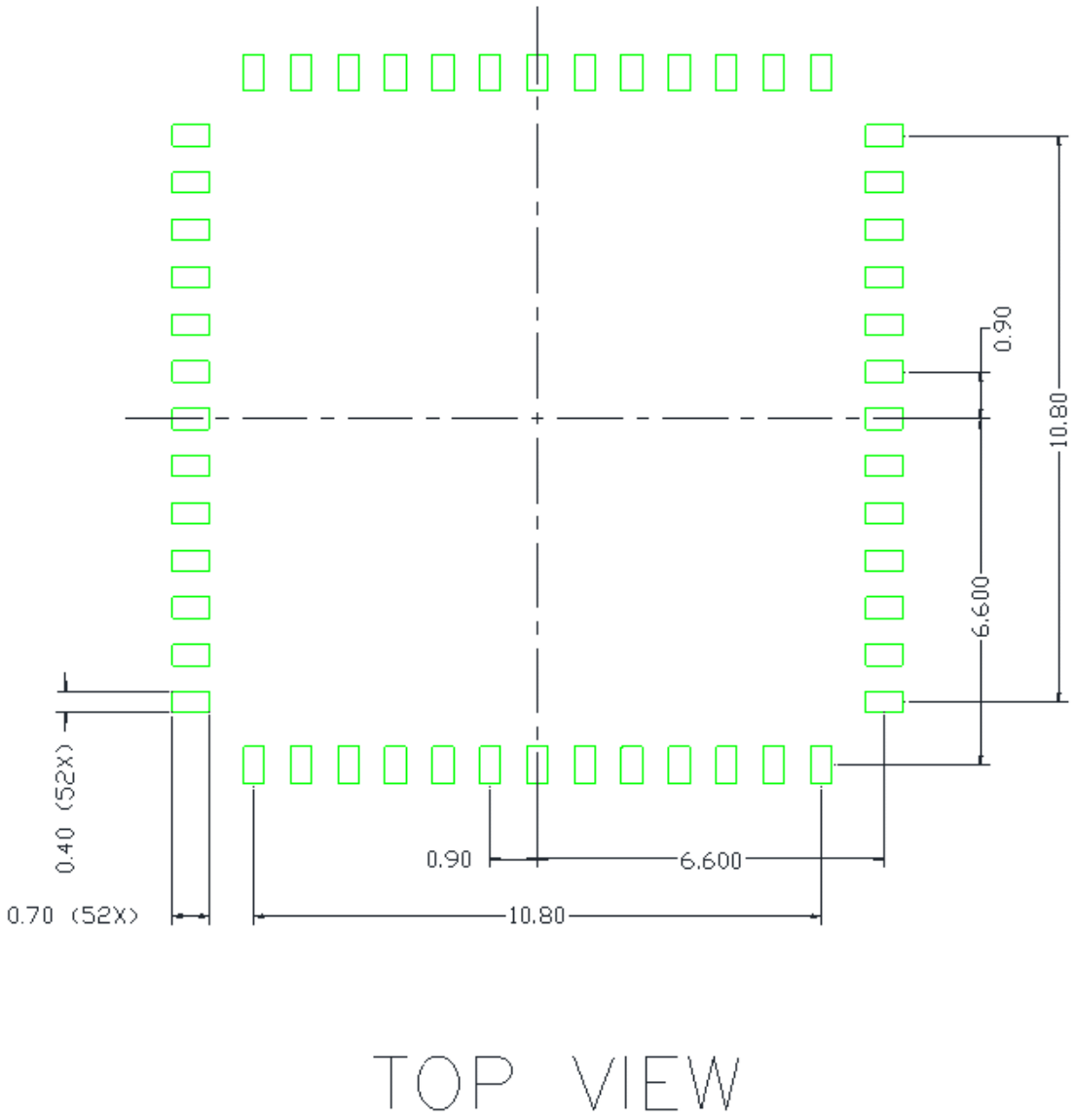



**Figure 7-2 : Recommended Solder Mask Design**

# 8 RECOMMENDED REFLOW PROFILE

## 8.1 REFLOW PROFILE

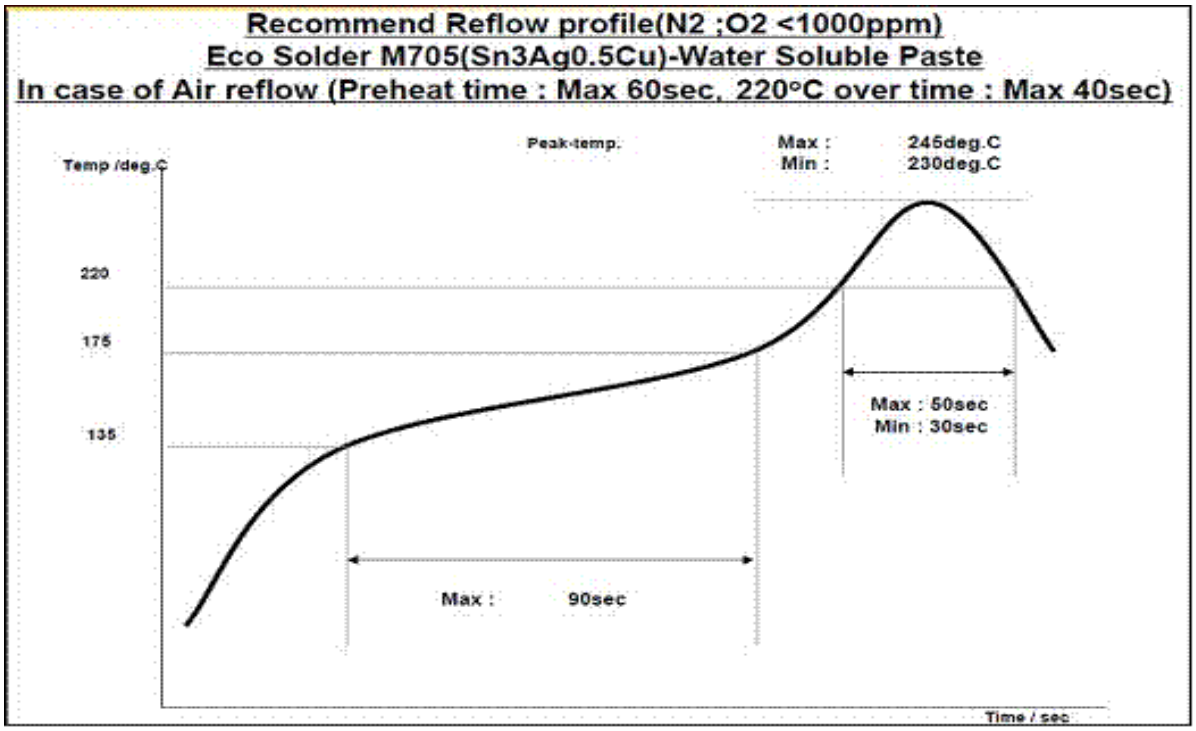



**Figure 8-1 : Reflow Profile**

**Table 8-1 : Temperature Value for Reflow Profile**

| Parameter | Value |
|---|---|
| Preheat Ramp-up Rate | 125°C to 217°C < 1°C /sec |
| Time at T > 217°C | 60 sec to 90 sec |
| Peak Temperature | 245°C |
| Cooling Ramp-down Rate | < 1°C / sec |
| Time From 25°C to peak | 240 to 360 sec |

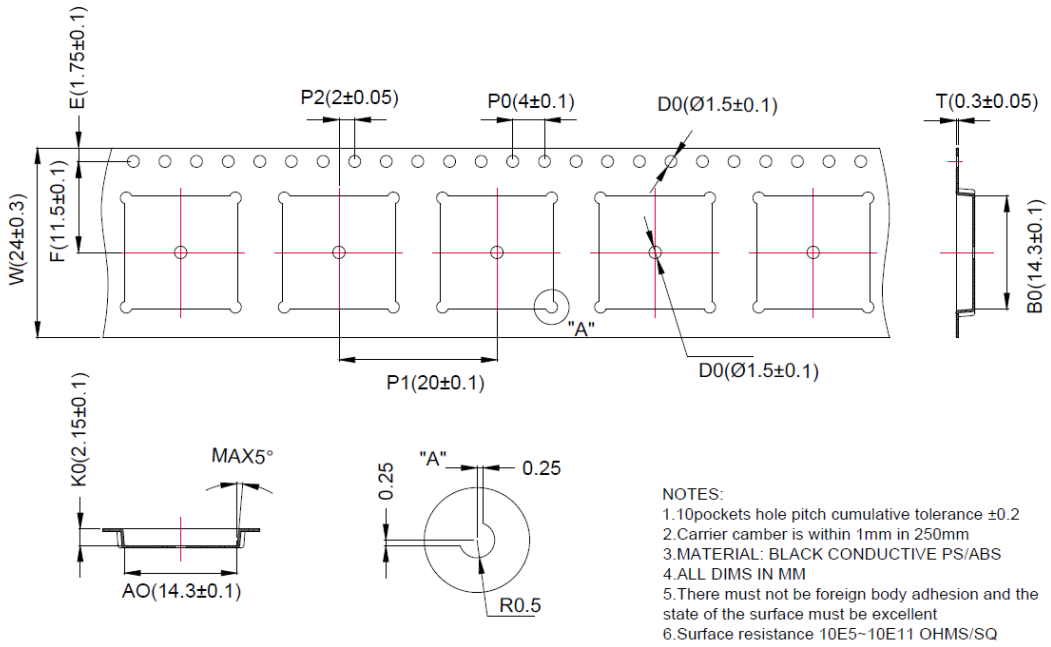
Note 1: The peak temperature of reflow profile should be less than 250°C.
Note 2: If the PCB is required double-sided soldering, it is strongly suggested that the module is mounted at the second side of PCB after completing soldering profile for the first side of PCB.

## 8.2 REWORK GUIDELINE

Reference guideline was listed below for de-mount process from PCB.

- PCBA should be baked for 24 hours at 125°C.
- De-mount EZ2625 module from PCB with hot air gun. Heat air should be less than 380 °C, 30 seconds.

# 9 TAPE AND REEL INFORMATION



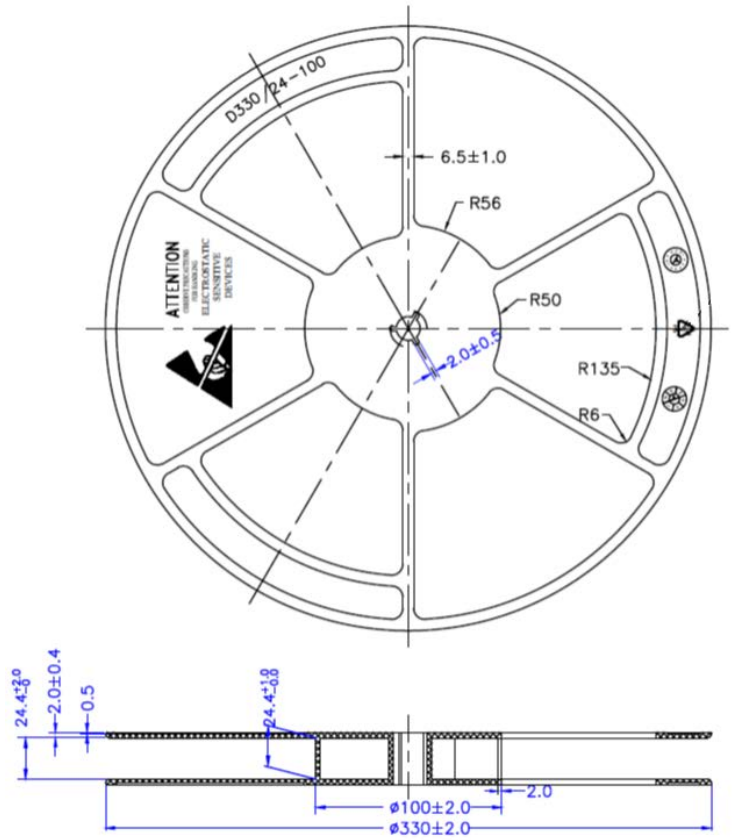




**Figure 9-1 : Tape and Reel Dimension**

# 10 HANDLING MOISTURE SENSITIVITY

## 10.1 MOISTURE SENSITIVITY LEVEL

Follow the latest IPC/JEDEC J-STD-020 standard revision for moisture sensitivity qualification. EZ2625 series is classified as MSL3.

**Table 10-1 : Moisture Sensitivity Level**

| Moisture Sensitivity Level | Condition | Floor Life |
|---|---|---|
| 1 | ≦30℃ and 85%RH | Unlimited |
| 2 | ≦30℃ and 60%RH | 1 year |
| 3 | ≦30℃ and 60%RH | 168 hours |
| 4 | ≦30℃ and 60%RH | 72 hours |
| 5 | ≦30℃ and 60%RH | 48 hours |
| 6 | ≦30℃ and 60%RH | 6 hours |

## 10.2 STORAGE CONDITION

EZ2625 series, as delivered in tape-and-reel carrier, must be stored in a vacuum-sealed bag. Shelf life is 12 months. This is required an ambient temperature less than 40 $^{O}$C and relative humidity less than 90%.

## 10.3 OUT-OF-BANG DURATION

EZ2625 series can be exposed for 168 hours to an environment with a maximum temperature of 30$^{O}$C and a maximum relative humidity of 60%.

## 10.4 BAKING REQUIREMENT

After bag is opened, module that will be subjected to reflow solder or other high temperature process must be

- Mounted within: 168 hours of factory condition ≦30$^{O}$C/60%RH,
- Stored at ≦ 30$^{O}$C/10%RH.

Module require bake before mounting, if Humidity Indicator Card reads ＞10% when read at 23±5$^{O}$C. If baking is required, following baking condition should be used.

- 24 hours at 125 ±5$^{O}$C .