# 8.3 Multivalued Logic & Signal Resolution

## Multivalued Logic and Signal Resolution

- Verilog uses ***4-valued*** logic system by default.
- Four values for signals in a 4-valued logic : *X*, 0, 1, and *Z*

| | |
|---|---|
| **X** | **Unknown state**.<br>May occur if the initial value of a signal is unknown, or if a signal is simultaneously driven to two conflicting values, such as 0 and 1. |
| **0** | 0 |
| **1** | 1 |
| **Z** | **High impedance**.<br>Used for modeling ***tristate buffers*** and ***busses***. |

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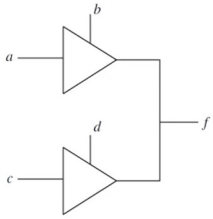
## Example

- Tristate buffers with active-high output enable:




(a) Tristate module with **always** statements:

```
module t_buff_exmpl (a, b, c, d, f);
   input a;
   input b;
   input c;
   input d;
   output f;
   reg f;

   always @(a or b)
   begin : buff1
      if (b == 1'b1)
         f = a ;
      else
         f = 1'bz ;
   end
```

* Violation of the guideline:
  Set an output in two **always** blocks. However, match the requirement of the circuit.

```
   always @(c or d)
   begin : buff2
      if (d == 1'b1)
         f = c ;
      else
         f = 1'bz ;
   end

endmodule
```

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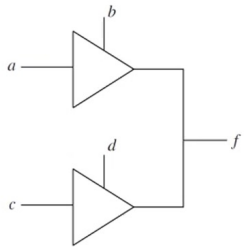



(b) Tristate module with **assign** statements:

```
module t_buff_exmpl2 (a, b, c, d, f);
   input a;
   input b;
   input c;
   input d;
   output f;

   assign f = b ? a : 1'bz ;
   assign f = d ? c : 1'bz ;

endmodule
```

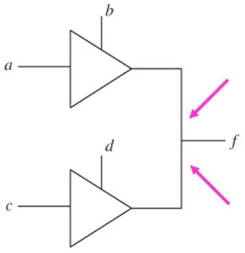
* Violation of the guideline:
  Set a single output in two **assign** statements.
  However, match the requirement of the circuit.



# Operation of Tristate Bus

Operation of a tristate bus with 4-valued logic:

| | X | 0 | 1 | Z |
|---|---|---|---|---|
| X | X | X | X | X |
| 0 | X | 0 | X | 0 |
| 1 | X | X | 1 | 1 |
| Z | X | 0 | 1 | Z |




- X resolved w/ any value returns X.
- Z resolved w/ any value returns that value.
- 0 resolved w/ 1 returns X.

Ex

| | X | 0 | 1 | Z |
|---|---|---|---|---|
| X | X | X | X | X |
| 0 | X | 0 | X | 0 |
| 1 | X | X | 1 | 1 |
| Z | X | 0 | 1 | Z |

# Example

- Resolved value of a signal for each pair of input values:
  - individual wires: s(0), s(1), s(2)
  - Result of the resolution: R

| Time | s(0) | s(1) | s(2) | R |
|---|---|---|---|---|
| 0 | Z | Z | Z | Z |
| 2 | 0 | Z | Z | 0 |
| 4 | 0 | 1 | Z | X |
| 6 | Z | 1 | Z | 1 |
| 8 | Z | 1 | 1 | 1 |
| 10 | Z | 1 | 0 | X |



# AND/OR Functions for 4-Valued Logic

- AND and OR functions for the 4-valued logic:

| AND | X | 0 | 1 | Z |
|---|---|---|---|---|
| X | X | 0 | X | X |
| 0 | 0 | 0 | 0 | 0 |
| 1 | X | 0 | 1 | X |
| Z | X | 0 | X | X |

| OR | X | 0 | 1 | Z |
|---|---|---|---|---|
| X | X | X | 1 | X |
| 0 | X | 0 | 1 | X |
| 1 | 1 | 1 | 1 | 1 |
| Z | X | X | 1 | X |