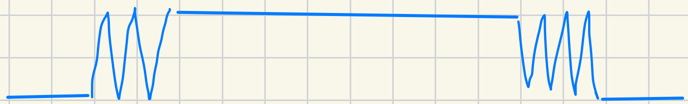
4.7 Synchronization and Debouncing

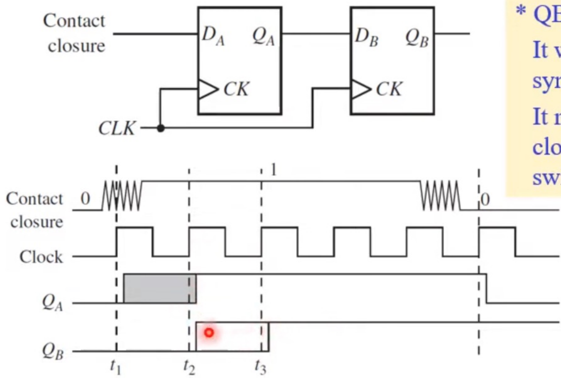
- Issues in systems w/ external inputs:
  - synchronization: outputs from a keypad or pushbutton switches are not sync to the system clock signal.
  - switch bounce: when a mechanical switch is closed or opened, the switch contact will bounce, causing noise in the switch output

Contact 

  - After closing the switch, must wait for the bounce to settle before reading the key.

Debouncing and Synchronizing Circuit

- Debouncing and synchronizing ckt: p.230, Fig 4-22
  - ***Flip-flops*** are very useful devices when contacts must be synchronized and debounced.

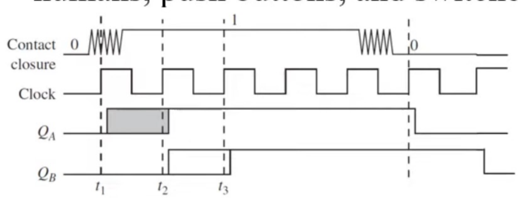


* QB: the ***debounced signal***
It will always be clean and synchronized w/ the clock.
It may be delayed up to 2 clock cycles after the switch is pressed.

* Assumption:
The clock period is greater than the bounce time.

Single Pulser

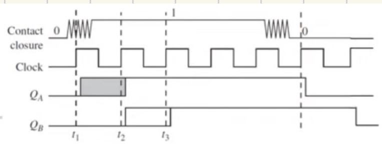
- It is difficult for humans to produce a signal that lasts only for a clock pulse.
- Single pulser:
  - a ckt that generates a ***single pulse*** for a human action of pressing a button or switch.
  - can be used in many applications involving humans, push buttons, and switches.



→ 4 or 5 cycles

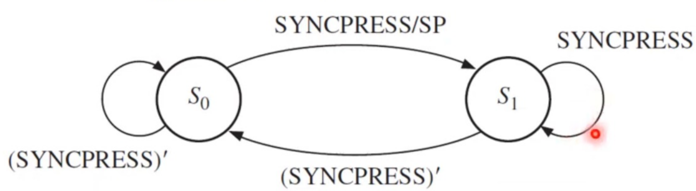
Problem Description

- Problem description:
  - Design a ckt that delivers a ***synchronized*** pulse that is a ***single*** clock cycle long when a button is pressed.
  - The ckt must sense the pressing of a button and assert an output signal for one clock cycle. Then the output stays inactive until the button is released.



State Diagram

- State diagram: 2 states

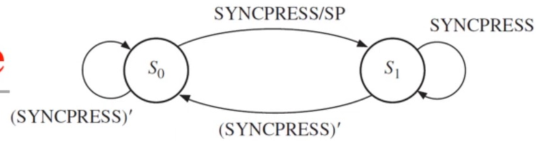


* ***SYNCPRESS***: synchronized key press ← Q_B

* ***SP***: single pulse

  - can be implemented using one flip-flop:
    D = SYNCPRESS
  - Equation for single pulse: $SP = S_0 \cdot SYNCPRESS$

State Table



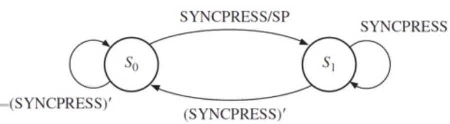
- State table: 2 states ⇒ 1 D flip-flop

Present state	Nest state		Output (SP)	
	SYNCPRESS = 0	1	SYNCPRESS = 0	1
(S_0) 0	0	1	0	1
(S_1) 1	0	1	0	0

– Memory input equation: ***D = SYNCPRESS***

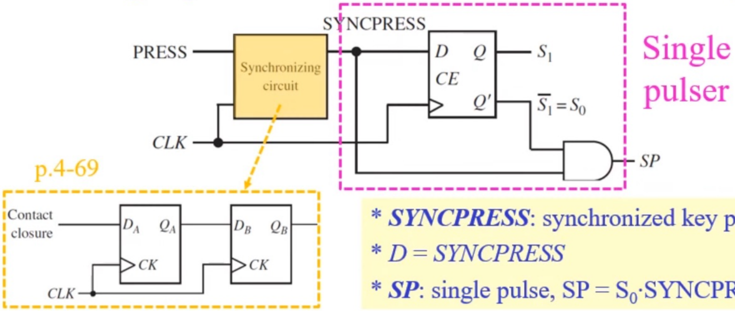
– Output equation: $\boldsymbol{SP = S_0 \cdot SYNCPRESS}$

Block Diagram



$SP = S_0 \cdot SYNCPRESS$

- Single pulser and synchronizer circuit: Fig 4-24



* ***SYNCPRESS***: synchronized key press
* *D = SYNCPRESS*
* ***SP***: single pulse, SP = $S_0 \cdot$SYNCPRESS

– ***Synchronizing ckt***: including 2 flip-flops (p.230, Fig 4-22)