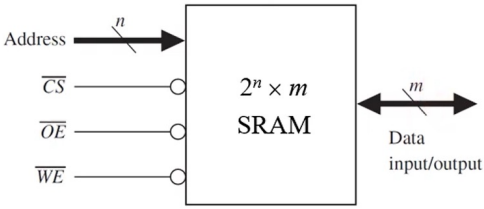
8.6 SRAM Model

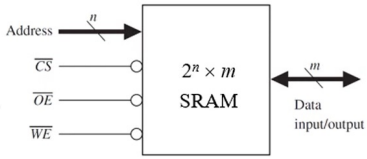
Block Diagram of SRAM

- Block diagram of a static RAM:



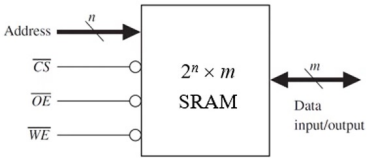
  - n address lines, m data lines, and 3 control lines.
  - Memory can store 2^n words, each m bits wide.
  - Data lines are ***bidirectional***.

    ⇒ Reduce the required # of pins and the package size of the memory chip.



- Function of the control lines:
  - **$\overline{CS}$**: ***Chip select***, active-low
    - When asserted low, selects the memory chip so that memory read and write ops are possible.
  - **$\overline{OE}$**: ***Output enable***, active-low
    - When asserted low, enables the memory output onto an external bus.
  - **$\overline{WE}$**: ***Write enable***, active-low
    - When asserted low, allows data to be written to the RAM.

  * A signal is asserted when it is in its active state.



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Verilog Model of RAM

- A simple memory model for a 256×8 RAM with ***async read*** and ***sync write***: