

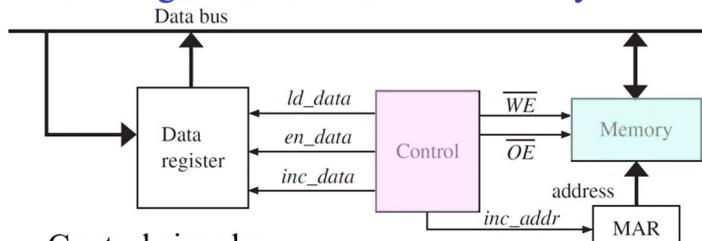
Model for SRAM Read/Write System

- Example: Design a RAM read-write system that reads the content of 32 memory locations from a RAM, increases each data value and stores it back to RAM.
 - **Data register:** holds the word that is read from memory
 - **Memory address register (MAR):** holds the memory addr that is being accessed.
 - **Data bus** is used as a *bidirectional tristate bus* (read/write data).

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Block Diagram

- Block diagram of RAM read-write system:



- Control signals:

- **ld_data** load data register from Data Bus
- **en_data** enable data register output onto Data Bus
- **inc_data** increment Data Register
- **inc_addr** increment MAR
- **WE** Write Enable for SRAM
- **OE** Output Enable for SRAM

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SM Chart

■ SM chart for RAM system:

- Reads a word from the RAM, loads it into the *data register*, increments the data register, stores the result back in the RAM, and then increments the *memory address register*.
- This process continues until the memory addr equals 32.

* a RAM w/ *async read* and *sync write*

\overline{CS}	\overline{OE}	\overline{WE}	Mode	I/O pins
H	x	x	Not selected	High-Z
L	H	H	Output disabled	High-Z
L	L	H	Read	Data out
L	x	L	Write	Data in

