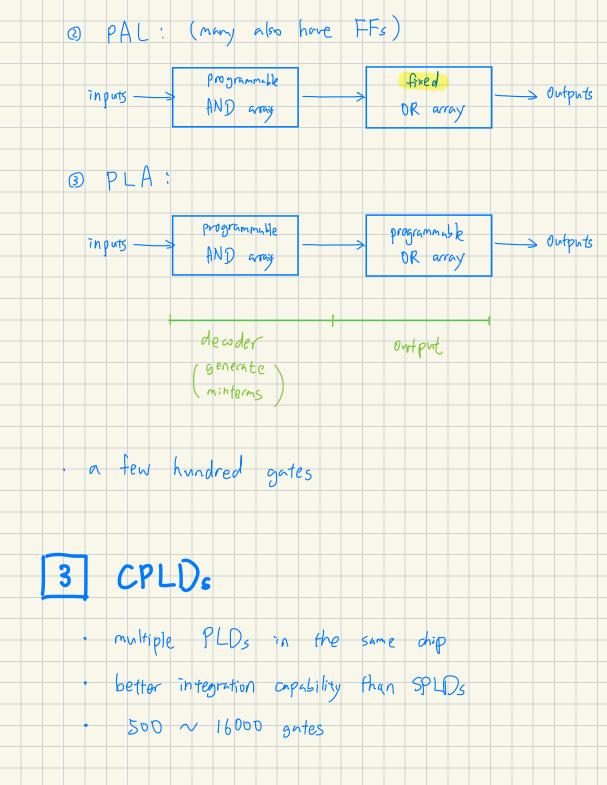
3.	Brief	Overvie.	, of	Png	ranmable	
	Logic	Devices	(P	LDs)		
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	Classiti	cution	ot	PLD.	5	
		program	mmasle	logic		
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Rom	M	GA A	SPLD		CPLD	FP6A
PROM	1	PLA		PAL	GAL	
Programmable	SPLD)5			1. Lattice	
D in	PROM!	fixed		pr	ogrammal k	-> Outputs
		AND army			OR array	



4 FPGAs uses SRAM to hold configuration info. larger & more complex blocks containing SRAM & muxes > 5 million gules