2.9 Delays in Verilog

1 Inertial Delay and Transport Delay

inertial delay	transport delay
models gates and other devices that do not propagate short pulses from input to output (pulse rejection)	models wiring delay

// explicit continuous assignment
wire D;
assign #5 D = A && B;
// implicit continuous assignment
wire #5 D = A && B;
// net declaration
wire #5 D;
assign D = A && B;
	// cannot be done w/ continuous assignment
	assign a = #10 b; (X)
	reg a;
	a = #10 b; (O)

inter-assignment delay delay evaluation	intra-assignment delay delay assignment

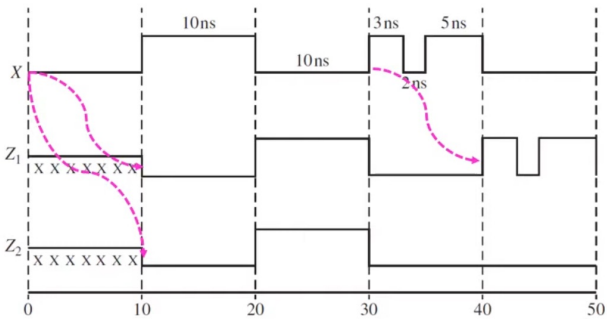
Ex :

Example: Initial and Transport Delays

```
always @ (X)
begin
   Z1 <=#10 (X); // transport delay
end
assign #10 Z2 = X; // inertial delay
```

* ***Delay assignment***: The expression on the right hand side is evaluated but not assigned to Z_1 until the delay has elapsed.

* ***Delay evaluation***: The delay elapses first and then the expression is evaluated and assigned to Z_2.



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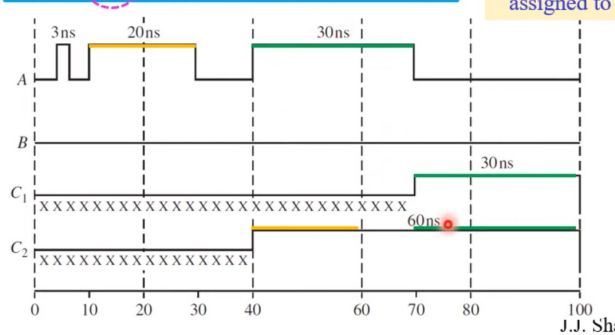
2 Net Delays

Example: Net Delays (p.86)

```
wire C1;
wire #10 C2;  //net delay on wire C2
assign #30 C1 = A || B;  //inertial delay
assign #20 C2 = A || B;  //inertial delay
```

* Added to net delay before being assigned to wire C2



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