

## 3.4 FPGAs

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### What are FPGAs?

- ICs that contain an array of identical logic blocks with programmable interconnections.
- 3 major programmable elements in an FPGA:
  - ① logic blocks (muxes, LUTs, AND-OR, NAND-NAND arrays)
  - ② interconnects
  - ③ I/O blocks

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### Pros & Cons Comparing to MPGAs

- Pros:
  1. shorter manufacturing time & design iteration
  2. cheaper than MPGAs at low volume

- Cons :

1. less dense
2. programmability requires a lot of resources
3. interconnection delays are unpredictable

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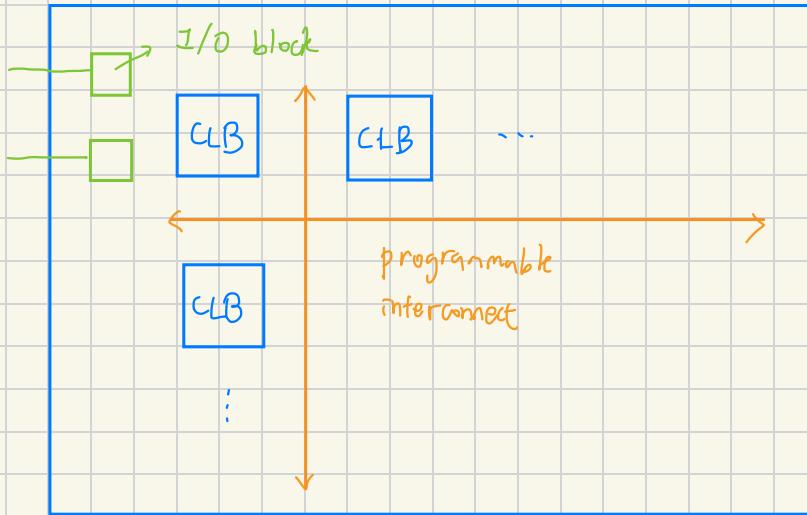
## Contents in this Section

- Organization
- Programmable Technologies
- Programmable Logic Block Architectures
- Programmable Interconnects
- Programmable I/O Blocks
- Dedicated Specialized Components
- Applications
- Design Flow

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## Organization of a Typical FPGA

- Layout of an FPGA



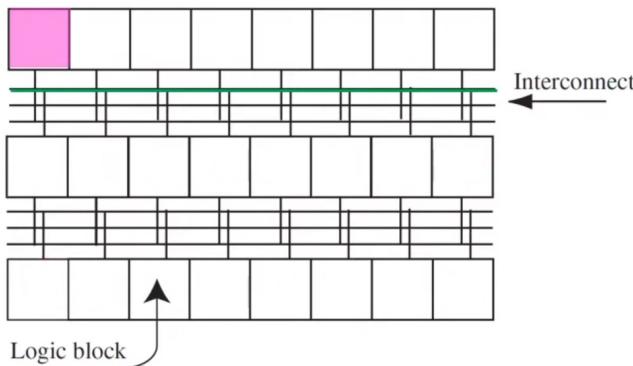
- architectures (topologies)

1. matrix -based (symmetric array) architecture
  - most Xilinx FPGAs
  - large granularity : capable of implementing 4 variable functions or more
  - smaller chips :  $8 \times 8$  arrays  
bigger chips :  $100 \times 100$  or bigger arrays
  - two -dimensional channel routing  
(Horizontal and vertical)

## 2. Row-based architecture

- Microchip FPGAs
- Inspired by traditional gate arrays
- traditional MPGAs use a similar structure
- one-dimensional channeled routing  
(Routing resources are located as channels b/w rows of logic resources)

### ■ Row-based:



\* Routing: **one-dimensional channeled** routing

## 3. hierarchical - based architecture

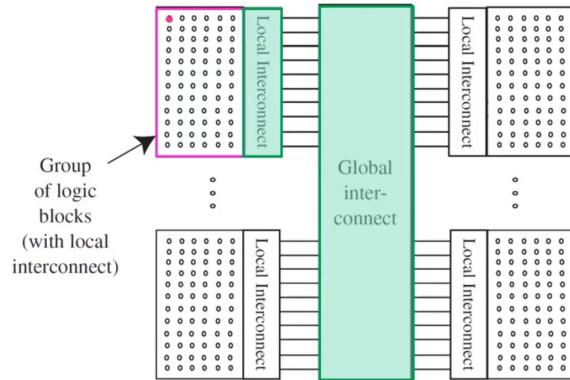
- Altera APEX20 and Altera II
- blocks of logic cells are grouped together by a local interconnect,

and several such groups are interconnected by global interconnect.



\* Routing: **local interconnect & global interconnect**

■ Hierarchical PLD:



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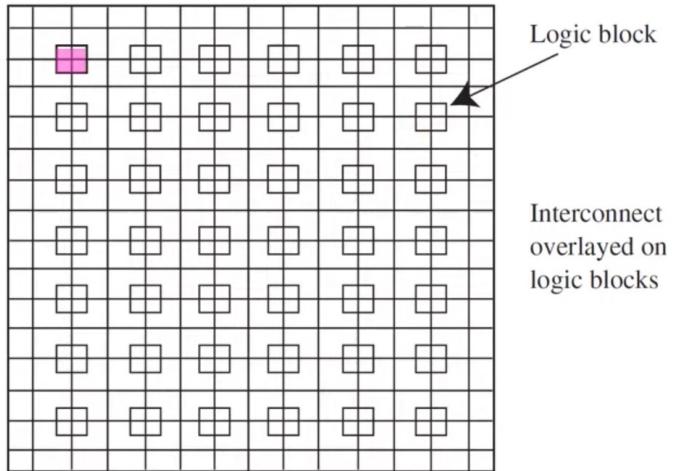
#### 4. sea. of gates architecture

(sea of tiles, sea of cells)

a few gates

- Plessey - mid 1990's (sea-of-gates),  
Microsemi Fusion (sea of tiles)
- a large number of gates w/ an  
interconnect superimposed

## ■ Sea-of-gates:



## 5 Programming Technologies

### • SRAM Programming Technology

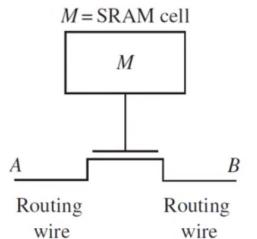
- LBSs, I/O blocks, interconnects can be made programmable using configuration bits stored in SRAM.  
can be easily implemented using  
LUTs

- another device (e.g. EEPROM) is needed to store the configuration bits.

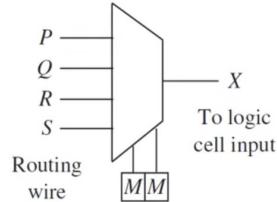
# Routing w/ Static RAM Programming

- Key idea:

- use pass transistors to create switches and then control them using the SRAM content.



Pass transistor connecting two points



Multiplexer controlled by two memory cells

\* An SRAM cell usually takes six transistors.

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→ expensive

- EPROM / EEPROM / flash programming technology
  - erasable (UV)      ↗ electrically - erasable
  - EPROM / EEPROM are used to control programmable connections.
  - Comparison w/ SRAM:
    - slower
    - more processing steps
- 反熔絲
- Antifuse programming technology

- programming : changes from high resistance (open circuit) to low resistance (closed circuit) when a high voltage is applied.
- one-time programmable (irreversible)
- Comparison w/ SRAM & (E)EPROM
  - smaller area
  - faster connections

## Comparison of Programming Technologies

- Characteristics of the major FPGA programming technologies:

Programming Technology	Volatile/Nonvolatile	Reprogrammable	Area Overhead	Resistance	Capacitance
SRAM	Volatile	In-circuit	Large	Medium-high	High
EPROM	Nonvolatile	Out-of-ckt	Small	High	High
EEPROM/Flash	Nonvolatile	In-ckt	Medium to high	High	High
Antifuse	Nonvolatile	Not	Small	Small	Small

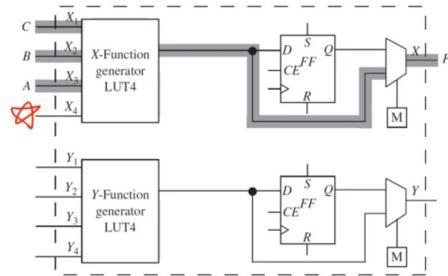
# 6 Programmable Logic Block Architectures

- different names of logic blocks:
  - Xilinx : Configurable Logic Blocks (CLBs)
  - Altera : Logic Elements (LEs)
    - Logic Array Block (LAB) : a collection of  $8 \sim 10$  LEs
  - Microsemi : VersaTile
- various basic components of logic blocks:
  - LUT - based  $\xrightarrow{\text{4/6-function generator}}$ 
    - LUT 4 / LUT 6 + FF
    - common for Xilinx and Altera

<Ans.>

$$\begin{aligned}F_1 &= A'B'C + A'BC' + AB \\&= \sum m(1, 2, 6, 7)\end{aligned}$$

■ Paths for  $F_1$ :



■ The LUT contents:

— 0, 1, 1, 0, 0, 0, 1, 1 | 0, 1, 1, 0, 0, 0, 1, 1  
  0   1   2   3   4   5   6   7   8   9   10   11   12   13   14   15

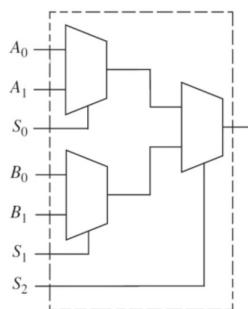
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— muxes & logic gates

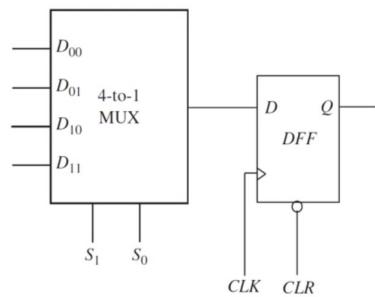
— MicroSemi

## Example: Logic Blocks Based on MUXs and Gates

- A logic block w/ three 2-to-1 MUXes:



- A logic block w/ a 4-to-1 MUX and a flip-flop:



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**<Ans.>**

$$F_1 = A'B'C + A'BC' + AB$$

$$= \sum m (1, 2, 6, 7)$$

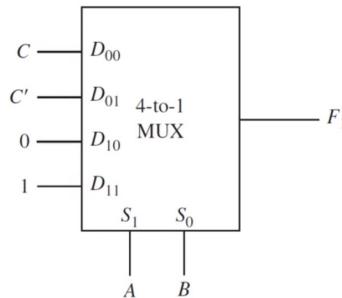
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

**C**

**C'**

**0**

**1**



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- transistor pairs ( e.g. CrossPoint PPGAs)
- PLD blocks ( e.g. early Altera)
- NAND gates ( e.g. Plessey)

## Summary: Architecture, Technology, & Logic Block Types of Commercial FPGAs

Company	Device Names	General Architecture	Logic Block Type	Programming Technology
Microsemi	IGLOO	Sea of Tiles	LUT	Flash
	ProASIC/ ProASIC3/ ProASICplus	Sea of Tiles	Multiplexers & Basic Gates	Flash, SRAM
	SX/SXA/ex/MX	Sea of Modules	Multiplexers & Basic Gates	Antifuse
	Axcelerator	Sea of Modules	Multiplexers & Basic Gates	SRAM
Xilinx	Fusion	Sea of Tiles	Multiplexers & Basic Gates	Flash, SRAM
	Kintex	Symmetrical Array	LUT	SRAM
	Virtex	Symmetrical Array	LUT	SRAM
Atmel	Spartan	Symmetrical Array	LUT	SRAM
	AT40KAL	Cell-Based	Multiplexers & Basic Gates	SRAM
QuickLogic	Eclipse II PolarPro	Flexible Clock Cell-Based	LUT LUT	SRAM SRAM
Altera	Cyclone II	Two-Dimensional Row and Column Based	LUT	SRAM
	Stratix II	Two-Dimensional Row and Column Based	LUT	SRAM
	APEX II	Row and Column, But Hierarchical Interconnect	LUT	SRAM

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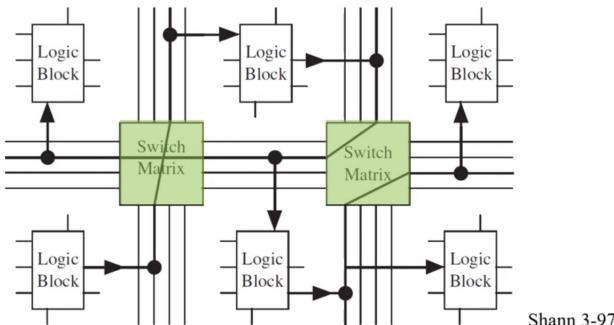
# Programmable Interconnect

- Interconnects in Symmetric Array FPGAs
  - general-purpose interconnect

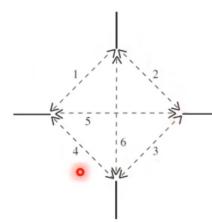
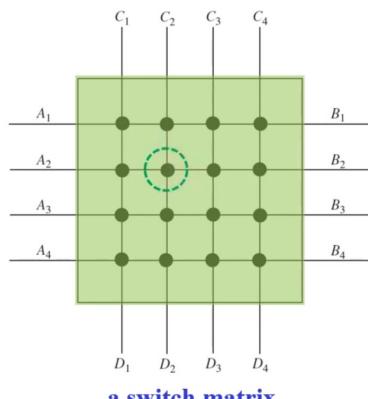
## General-Purpose Interconnect

- General-purpose:

- Use **switch matrices** that provide interconnections b/t routing wires connected to the switch matrix.



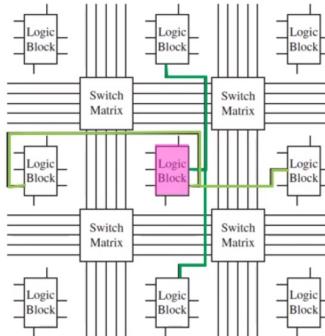
- Internals of a **switch matrix**:



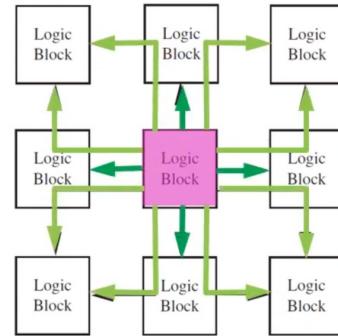
**a 6-way switch**

- direct interconnects
  - special connections b/w the 4 ~8 nearest neighbor blocks
  - do not go through the routing matrix  
⇒ fast

### ■ Nearest 4 and 8 neighboring blocks:



(a) Direct interconnects to four near neighbors



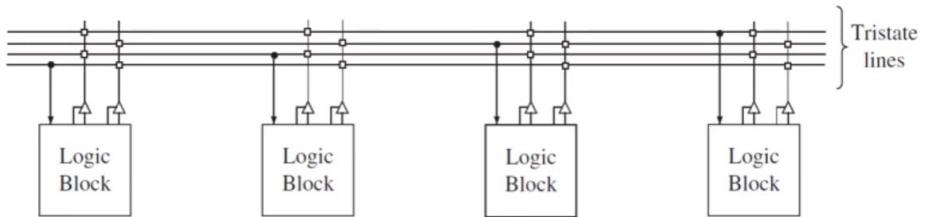
(b) Special connections to 8 neighbors

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- global lines
  - routing lines that span the entire width/height of device
  - provide for purposes such as high

fan out & low-skew clock distribution

- A limited  $\approx 4$  of such global lines are provided by many FPGAs in horizontal & vertical directions.



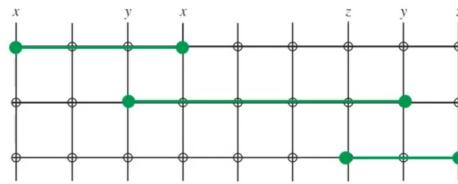
- Interconnects in row-based FPGAs
  - has rows of logic blocks and channels of switches to enable connections b/w the logic blocks.
  - two categories:
    1. non-segmented routing (high area overhead)
    2. segmented routing

## Example: Non-segmented vs. Segmented

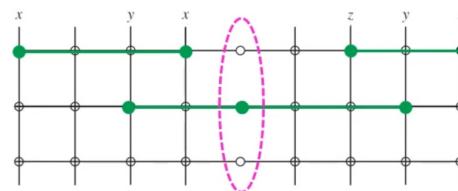
Example nets



Non-segmented channel routing of example nets



Segmented channel routing of example nets



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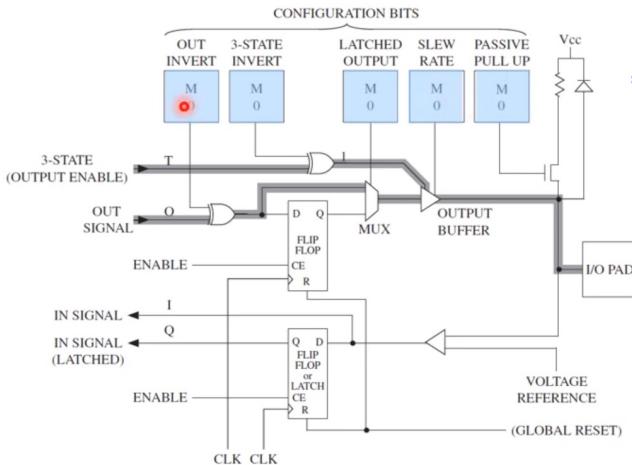
## Programmable I/O Blocks

- I/O blocks on modern FPGAs.
  - allow use of pins as:
    - input / output
    - direct (combinational) / latched
    - tristate true / inverted
    - a variety of I/O standards

# Programmable I/O Blocks

■ E.g.: Xilinx

allow use of the pin as *input* and/or *output*, in *direct (comb)* or *latched* forms, in *tristate true* or *inverted* forms, and with a variety of *I/O standards*



\* M: configuration memory cell

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## Dedicated Specialized Components

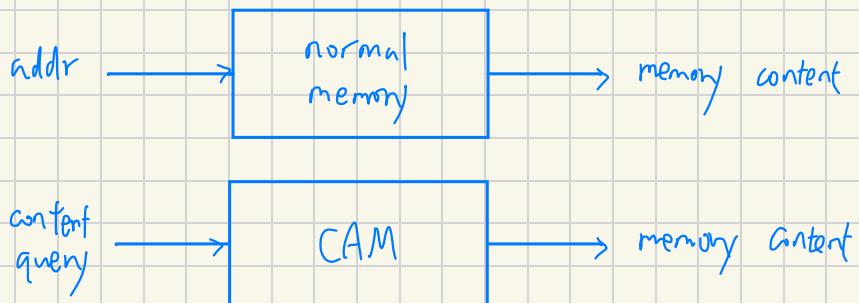
- dedicated memory blocks (RAM)
  - a key feature of modern FPGAs
  - capacity : 16 K ~ 10 M bits
  - Variable-width RAM: width (# bits/word) of the embedded RAM can often be adjusted.

Ex. aspect ratios of 32 K-bit RAM

#bits/word Width	#words Depth	Addr Bus	Data Bus	* # of addr lines and data lines get adjusted according to the aspect ratio. 3-108
1	32 K	15 bits	1 bit	
2	16 K	14 bits	2 bits	
4	8 K	13 bits	4 bits	
8	4 K	12 bits	8 bits	
16	2 K	11 bits	16 bits	

- dedicated arithmetic units / muxes
  - When logic is implemented using FPGA logic blocks, it generally takes more area and power and is slower than custom implementations.
- DSP processors
  - dedicated multipliers : help DSP applications
  - carry chains : facilitate addition
  - DSP building blocks : hardware for FFTs, Finite Impulse Response (FIR) filters, infinite impulse response (IIR) filters, encryption / decryption, codecs, security

- embedded processors
- analog - to - digital (A/D) converters
- content addressable memory (CAM)
  - CAM is a special type of memory in which the content, not the address, is used to search the memory.



## 10 Applications of FPGAs

- rapid prototyping
- final product in medium-speed systems  
(enhancements can be provided by software updates.)
- (dynamically) reconfigurable clkts & systems
- glue logic : interface b/w modules & components

- hardware accelerators / coprocessors



## Design Flow for FPGAs

1. HDL code
2. simulate & debug
3. synthesize the design targeting your device.
4. run the mapping / partition program.
5. run an automatic PnR program
6. run a bit pattern generation program
7. download the bit pattern into the internal configuration cells in the FPGA and test the operation of the FPGA