8.4 Built-in Primitives

1 Introduction

- built-in primitives: provide gate and switch level modeling facility.
  - predefined logic gate primitives: 14
  - predefined switch primitives: 12
- advantages of modeling at gate or switch level
  - synthesis tools can easily map it to the desired circuitry since gates provide a very close 1-1 mapping b/w ckt & model.
  - There are primitives such as the bidirectional transfer gate that cannot be otherwise modeled using dataflow or behavioral level.

Built-in Primitives in Verilog

* Output port(s) first followed by input(s).

Gate-level Primitive	Type
and, nand, nor, or, xnor, xor	n-input gates (1 output)
buf, not	n-output gates (1 input)
bufif0, bufif1, notif0, notif1	Three-state gates

Switch-level Primitive	Type
pulldown, pullup	Pull gates; resistor
cmos, nmos, pmos, rcmos, rnmos, rpmos	MOS switches
rtran, rtranif0, rtranif1, tran, transif0, tranif1	Bidirectional switches

Example: Array of Tristate Buffers

- Model an array of four inverting tristate buffers using built-in primitive:

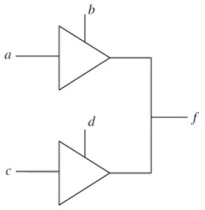
```
module tri_driver (in, out, tri_en);
  input [3:0] in;
  output [3:0] out;
  input tri_en;

  bufif0 buf_array[3:0] (out, in, tri_en); // array of tristate buffers

endmodule
```

* ***Output*** first followed by ***inputs***, ***control*** last.

  - buf_array[3:0] is used as instance name and is indexed.
  - Statement could be replaced using instance names that are not indexed:

```
bufif0  buf_array3 (out[3], in[3], tri_en);
bufif0 buf_array2 (out[2], in[2], tri_en);
bufif0 buf_array1 (out[1], in[1], tri_en);
bufif0 buf_array0 (out[0], in[0], tri_en);
```

Example




```
module tri_buffer (a,b,c,d,f);
   input a,b,c,d;
   output f;

   bufif1 buf_one (f,a,b);
   bufif1 buf_two (f,c,d);

endmodule
```

* ***Output*** first followed by ***inputs***, ***control*** last.

- delay specification for built-in primitives
  - built-in primitives can have an optional delay specification
  - delay specification can contain up to 3 delay values, depending on the gate.
    - 1st delay: transition to rise delay (transition to 1)
    - 2nd delay: transition to fall delay (transition to 0)

- 3rd delay : transition to high impedance delay (turn off delay)

Examples: Primitives w/ Delays

- Examples: primitives with delays:
  - **and** # (10) a1 (out, in1, in2);
    // only one delay so rise delay = 10
  - **and** # (10,12) a2 (out, in1, in2);
    // rise delay = 10 and fall delay = 12
  - **bufif0** # (10,12,11) b3 (out, in, ctrl);
    // rise, fall, and turn-off delays