# 8.7 Model for SRAM R/W System

Model for SRAM Read/Write System

- Example: Design a RAM read-write system that reads the content of 32 memory locations from a RAM, increases each data value and stores it back to RAM.
  - **Data register**: holds the word that is read from memory
  - **Memory address register (MAR)**: holds the memory addr that is being accessed.
  - **Data bus** is used as a *bidirectional tristate bus* (read/write data).

8-61

Block Diagram

- Block diagram of RAM read-write system:
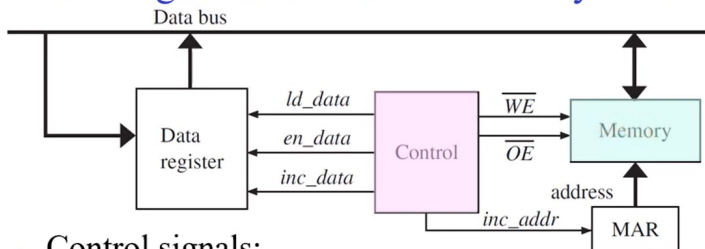
  - Control signals:
    - › **ld_data**   load data register from Data Bus
    - › **en_data**   enable data register output onto Data Bus
    - › **inc_data**   increment Data Register
    - › **inc_addr**   increment MAR
    - › **$\overline{WE}$**   Write Enable for SRAM
    - › **$\overline{OE}$**   Output Enable for SRAM

8-62

SM Chart

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pins
H	×	×	Not selected	High-Z
L	H	H	Output disabled	High-Z
L	L	H	Read	Data out
L	×	L	Write	Data in

- SM chart for RAM system:

  — Reads a word from the RAM, loads it into the *data register*, increments the data register, stores the result back in the RAM, and then increments the *memory address register*.

  — This process continues until the memory addr equals 32.

S_0 =0 S_2

$\overline{OE}$
ld_data

$\overline{WE}$
en_data
inc_addr

S_1

S_3

inc_data

addr = 32   N

Y

done

8-63