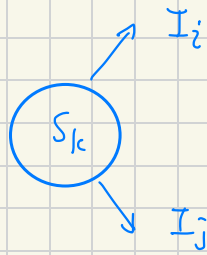


4.5 State Graphs for Control Circuits

1 Notations and Conditions Used on Control State Graphs

- Label control state graphs using variable names instead of 0's and 1's.
- Label of arc on a Mealy state graph $X_i X_j / Z_p Z_q$
 - inputs $X_i, X_j : 1$
other inputs : don't care's
 - outputs $Z_p, Z_q : 1$
other outputs : 0
 - Then traverse the arc to go to the next state.
- completely specified proper state graph :
 - the next state is uniquely defined for every input combination.



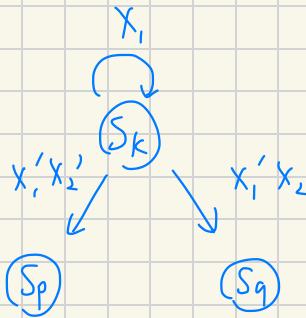
- constraints on the input labels for every state S_k :

(Each I_x is a boolean condition formed from the machine's input variables,
e.g. $I_i = A'B$ or AB')

1. If I_i and I_j are any pair of input labels on arcs exiting state S_k , then $I_i I_j = 0$ if $i \neq j$.
 \Rightarrow At most one input label can be 1 at any given time.
2. If n arcs exit state S_k and the n arcs have labels I_1, I_2, \dots, I_n , respectively, then, $I_1 + I_2 + \dots + I_n = 1$

⇒ At least one input label will be 1 at any given time.

Ex. A Partial State Graph



• For S_k :

$$\begin{cases} I_1 = X_1 \\ I_2 = X_1'X_2' \\ I_3 = X_1'X_2 \end{cases}$$

• Condition 1:

$$I_1 I_2 = (X_1)(X_1'X_2') = 0$$

$$I_1 I_3 = (X_1)(X_1'X_2) = 0$$

$$I_2 I_3 = (X_1'X_2')(X_1'X_2) = 0$$

• Condition 2:

$$\begin{aligned} I_1 + I_2 + I_3 &= X_1 + X_1'X_2' + X_1'X_2 \\ &= 1 \end{aligned}$$

⇒ Conditions 1 & 2 are satisfied, this graph is a completely specified state graph

• incompletely specified state graph

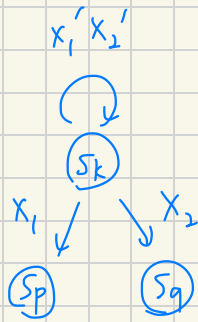
– It must always satisfy condition 2.

$$I_1 + I_2 + \dots + I_n = 1$$

- It must condition 1 for all combinations of values of input variables that can occur for each state S_k .

$$I_i I_j = 0 \text{ if } i \neq j$$

Ex. A partial state graph



- For S_k :

$$\begin{cases} I_1 = x_1'x_2' \\ I_2 = x_1 \\ I_3 = x_2 \end{cases}$$

- Condition 1:

$$\begin{aligned} I_1 + I_2 + I_3 \\ &= x_1'x_2' + x_1 + x_2 \\ &= 1 \end{aligned}$$

- Condition 2:

$$\begin{aligned} I_1 I_2 &= (x_1'x_2') x_1 = 0 \\ I_2 I_3 &= (x_1'x_2) x_2 = 0 \\ I_1 I_3 &= (x_1')(x_2) = ? \end{aligned}$$

$\Rightarrow x_1 = x_2 = 1$ cannot occur in state S_k .