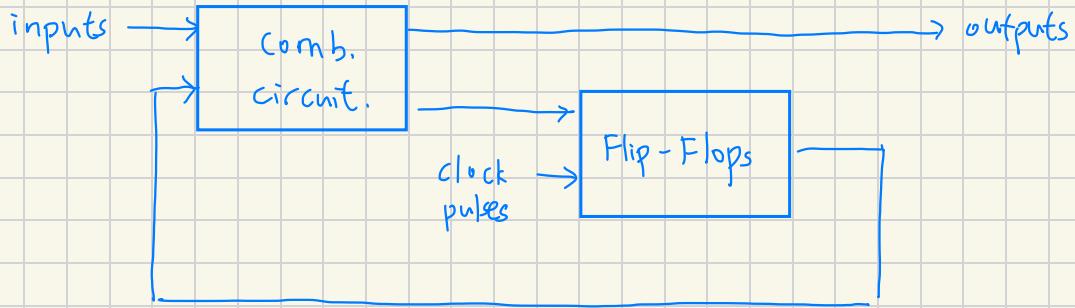


1.10 Sequential Circuit Design

1 Analysis of a Digital Circuit

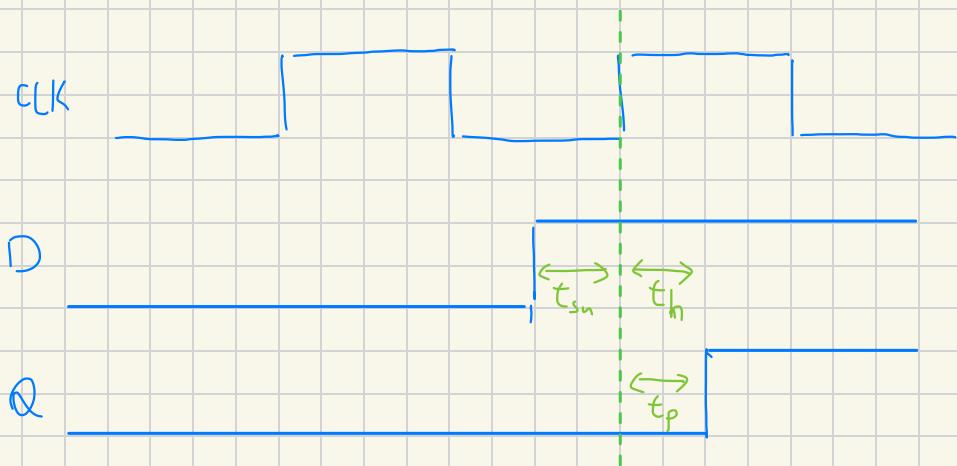


- analyze the function of the circuit
- analyze the performance / timing of the circuit
 - ① For comb. ckt : input - to - output delay
 - ② For seq. ckt. : the timing conditions for proper operation (e.g. max frequency)

2 Timing Parameters of Flip-Flops



- propagation delay
- setup time
- hold time

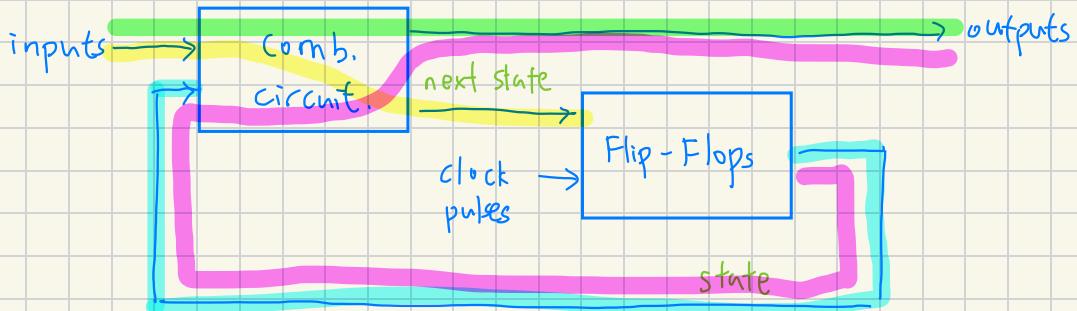


3 Timing Conditions for Proper Operation

- Clock period must be long enough.
⇒ propagation delays, setup and hold times create complications in timings
- Static Timing Analysis (STA) :
 - validating the timing performance of a design by checking all possible paths for timing violations under worst case conditions.

4

Timing Paths



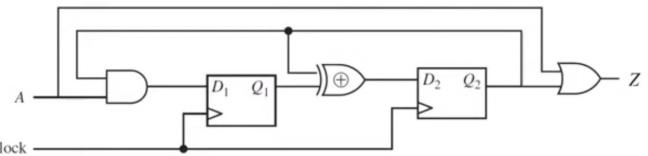
- 4 types of timing paths in a synchronous digital system.

4
timing
paths

- (i) input to FF
- (ii) input to output (no FF)
- (iii) FF to FF
- (iv) FF to output

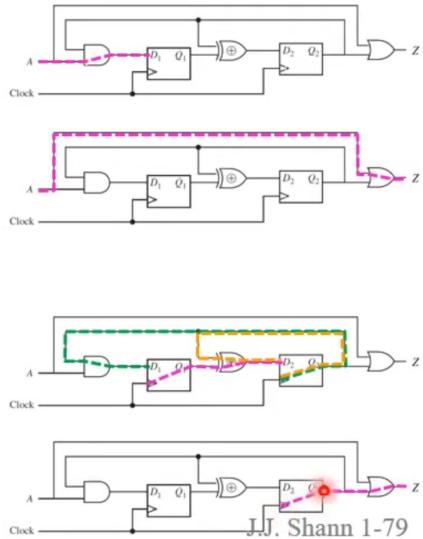
Ex.

<Ans.>



■ Static timing paths:

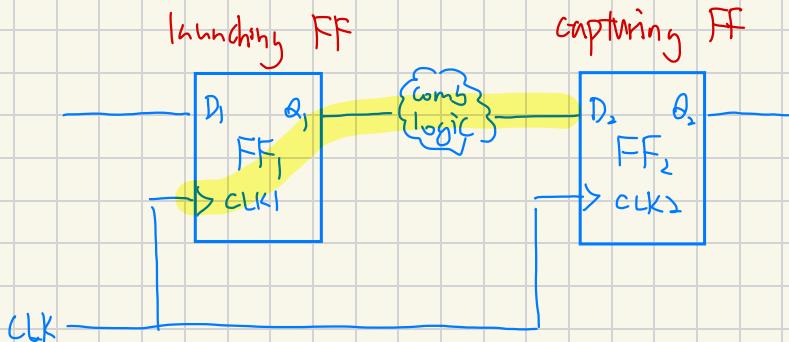
- Input to flip-flop:
 1. From A to D_1 via AND
- Input to output:
 2. From A to Z via OR
- Flip-flop to flip-flop:
 3. From D_1 to D_2 via XOR
 4. From D_2 to D_1 via AND
 5. From D_2 to D_2 via XOR
- Flip-flop to output:
 6. From D_2 to Z via OR



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5 Timing Rules for FF to FF Paths

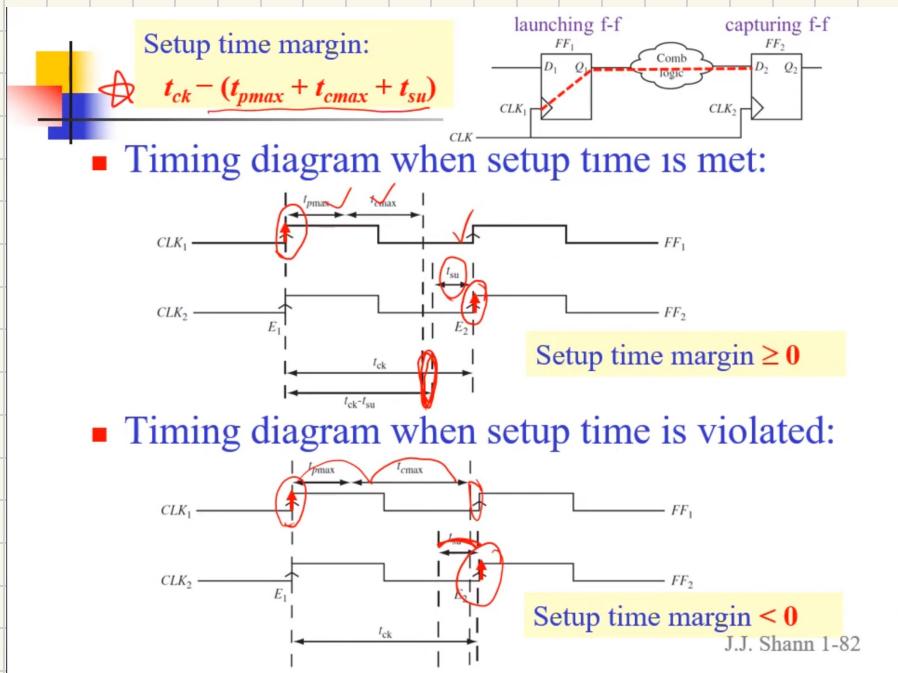
- Timing rules for FF to FF path:



Rule #1: setup time rule: clock period should be long enough to satisfy the capturing FF setup time.

- $t_{ck} \geq t_{pmax} + t_{cmax} + t_{su}$
- reduce the clock freq. to correct the setup time violation

- Setup time margin: $t_{ck} - (t_{pmax} + t_{cmax} + t_{su})$



Rule #2: hold time rule: minimum circuit delays should be long enough to satisfy FF hold time.

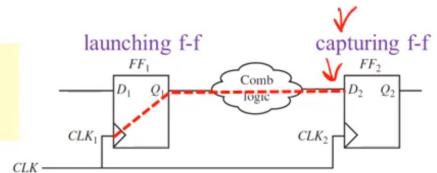
increase the min comb. ckt. delay
 ↗ to satisfy the capturing FF hold time

$$\underbrace{t_{pmin}}_{\text{min. prop. delay of the launching FF}} + \underbrace{t_{cmin}}_{\text{min. prop. delay of the comb. ckt.}} \geq t_h$$

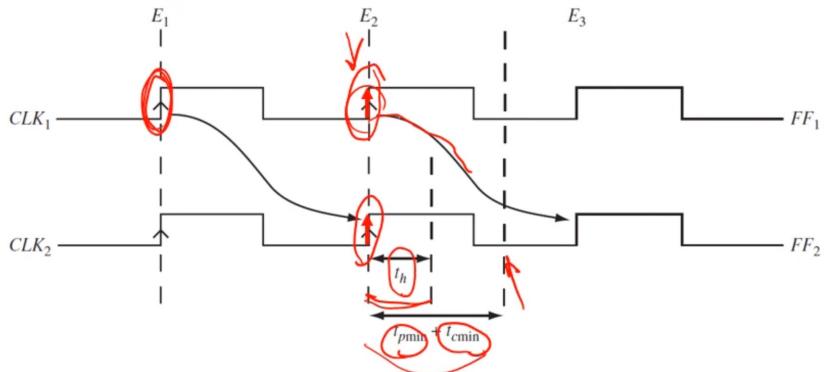
hold time of the capturing FF

Hold time rule for f-f to f-f path:

$$\underline{t_{pmin} + t_{cmin} \geq t_h}$$

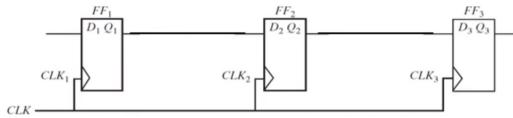


- Timing diagrams illustrating hold time in flip-flop path:

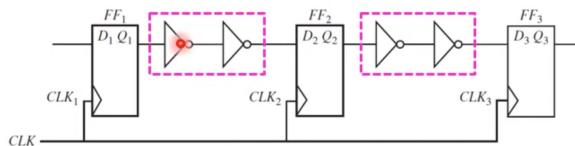


Example: Shift Register

- Designing shift registers by chaining together flip-flops:



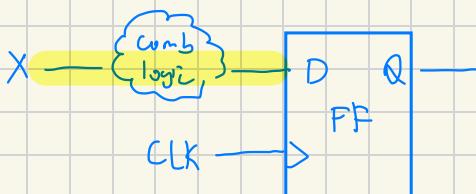
- Combinational ckt delay is zero.
⇒ It is very difficult to meet hold-time constraints
- For meeting hold-time constraints:



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6

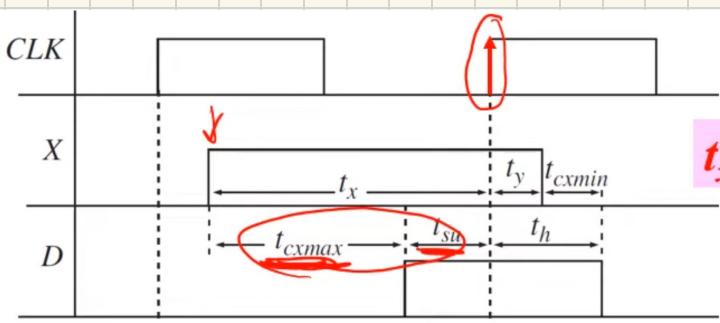
Timing Rules for Input to FF Path



Rule #3: setup time rule

$$\underline{t_x} \geq t_{cmix} + t_{su}$$

X changes at
time t_x before
the active edge
of the clock

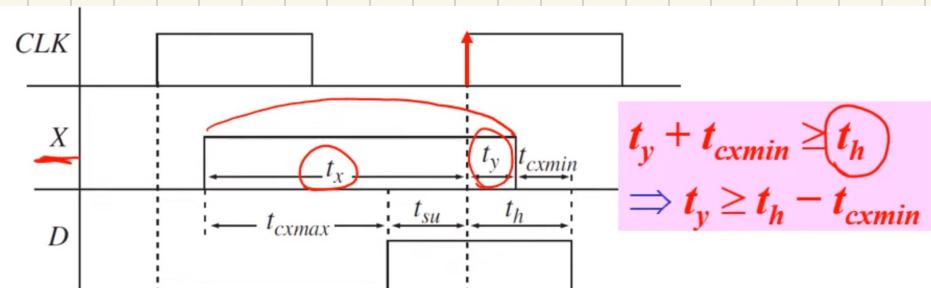


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Rule #4: hold time rule

$$\underline{t_y} + t_{cxmin} \geq t_h$$

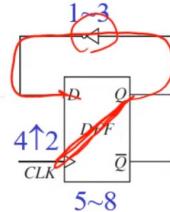
X changes at
time t_y after
the active edge
of the clock



Ex. Simple Frequency Divider

<Ans>

Inverter: $t_{invmin} = 1 \text{ ns}$, $t_{invmax} = 3 \text{ ns}$
 Flip-flop: $t_{pmin} = 5 \text{ ns}$, $t_{pmax} = 8 \text{ ns}$,
 $t_{su} = 4 \text{ ns}$, $t_h = 2 \text{ ns}$



* No external input

- The minimum clock period t_{ckmin} :

$$\text{Rule#1 } t_{ckmin} = t_{pmax} + t_{cmax} + t_{su} \\ = 8 + 3 + 4 = 15 \text{ ns}$$

- The maximum clock frequency f_{max} :

$$f_{max} = 1/t_{ckmin} = 66.67 \text{ MHz}$$

- Hold time requirement:

 - for filp-flip to flip-flop path: Rule 2

$$\text{Rule#2 } t_{pmin} + t_{cmin} \geq t_h \Rightarrow 5 + 1 \geq 2 \quad (\checkmark)$$

 - for input to flip-flop path: Rule 4

no external input

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Ex.

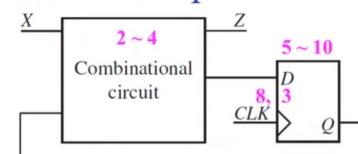
<Ans>

Delay of the combinational circuit: 2~4 ns

Flip-flop: $t_p : 5 \sim 10 \text{ ns}$; $t_{su} = 8 \text{ ns}$; $t_h = 3 \text{ ns}$

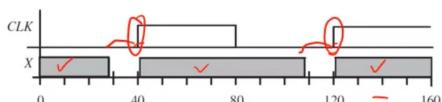
- Setup time requirement for f-f to f-f path:

$$\text{Rule#1 } t_{ck} \geq t_{pmax} + t_{cmax} + t_{su} \\ t_{ck} \geq 10 + 4 + 8 = 22 \text{ ns}$$



- Hold time requirement for f-f to f-f path:

$$\text{Rule#2 } t_{pmin} + t_{cmin} \geq t_h \\ 5 + 2 = 7 \geq 3 \quad (\checkmark)$$



- Safe regions for changes in input X:

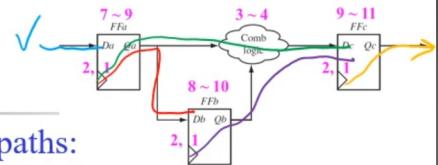
$$\text{– Rule 3: } t_x \geq t_{cxmax} + t_{su} \Rightarrow t_x \geq 4 + 8 = 12$$

$$\text{– Rule 4: } t_y \geq t_h - t_{cxmin} \Rightarrow t_y \geq 3 - 2 = 1$$

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Ex.

<Ans.>



■ Max delays for all timing paths:

- Delay for path from flip-flop A to B:
 $t_{\text{clk-to-Q(A)}} + t_{\text{su(B)}} = 9 + 2 = 11 \text{ ns}$
 - Delay for path from flip-flop A to C:
 $t_{\text{clk-to-Q(A)}} + t_{\text{comb}} + t_{\text{su(C)}} = 9 + 4 + 2 = 15 \text{ ns}$
 - Delay for path from flip-flop B to C:
 $t_{\text{clk-to-Q(B)}} + t_{\text{comb}} + t_{\text{su(C)}} = 10 + 4 + 2 = 16 \text{ ns}$
 - Delay for path from input to flip-flop A:
 $t_{\text{su(A)}} = 2 \text{ ns}$
 - Delay for path from flip-flop C to output:
 $t_{\text{clk-to-Q(C)}} = 11 \text{ ns}$
- ### ■ Min clock period: $\Rightarrow 16 \text{ ns}$
- ### ■ Max clock frequency:
- $1/16 \text{ ns} = 62.5 \text{ MHz}$

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7

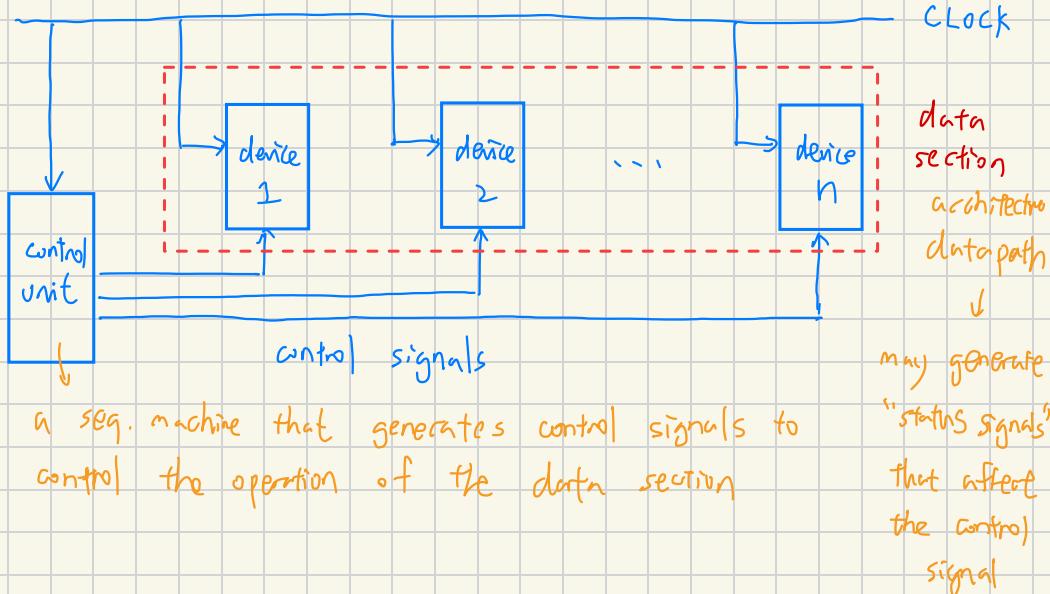
Timing Conditions for Sync. Seq Ckts w/ Clock Skew

• Sync Design v.s Async Design

Despite their higher power consumption, designers favor

	design & debug	reliability	power consumption at design	sync design
sync design	easier	better	more (clock distribution network)	↑
async design	harder	worse	less	

Synchronous Digital System



a seq. machine that generates control signals to control the operation of the data section

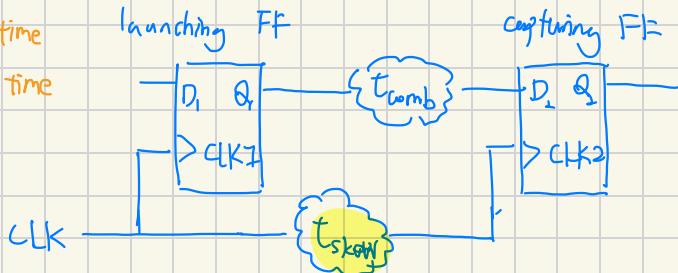
many generate
"status signals"
that affect
the control
signal

Clock skew

- the absolute time difference in clock signal arrival b/w 2 points in the clock network.

- positive clock skew

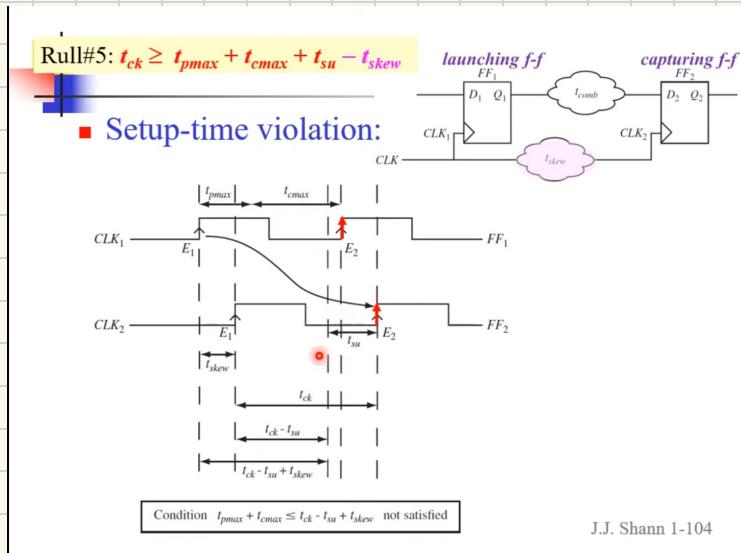
good for setup time
bad for hold time



- ① wire delay
- ② combinational ckt.

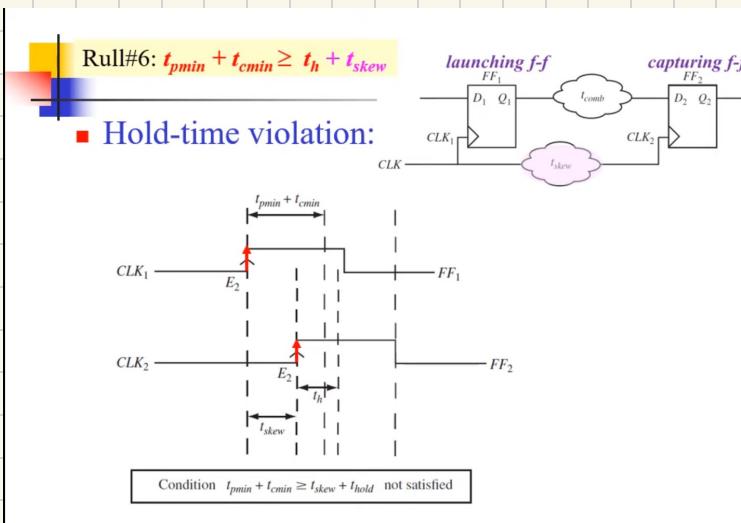
Rule #5: modification of rule #1

$$t_{ck} \geq t_{pmax} + t_{cmax} + t_{su} - t_{skew}$$



Rule #6: modification of rule #2

$$t_{pmin} + t_{cmin} \geq t_h + t_{skew}$$



Ex.

<Ans.>

(a) Max clock frequency:

i. with clock skew

$$\begin{aligned}t_{clk} &= t_{pmax} + t_{cmax} + t_{su} - t_{skew} \\&= 9 \text{ ns} + 6 \text{ ns} + 5 \text{ ns} - 3 \text{ ns} \\&= 17 \text{ ns}\end{aligned}$$

$$f_{max} = 1/17 \text{ ns} = 58.82 \text{ MHz}$$

ii. without clock skew (p.39)

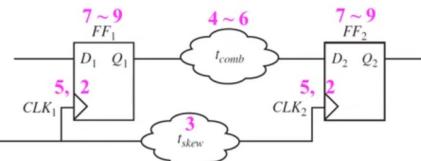
$$\begin{aligned}t_{clk} &= t_{pmax} + t_{cmax} + t_{su} \\&= 9 \text{ ns} + 6 \text{ ns} + 5 \text{ ns} \\&= 20 \text{ ns}\end{aligned}$$

$$f_{max} = 1/20 \text{ ns} = 50 \text{ MHz}$$

(b) The biggest skew:

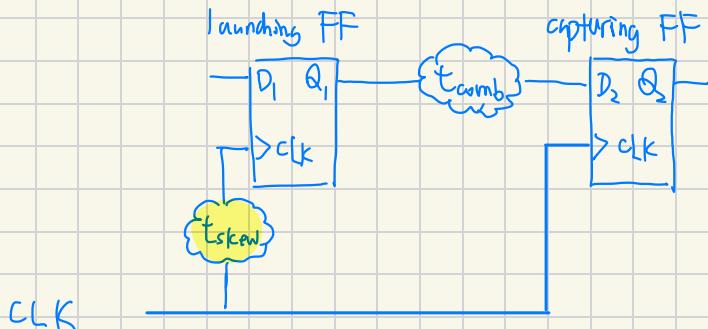
$$\begin{aligned}t_{pmin} + t_{cmin} &\geq t_h + t_{skew} \Rightarrow 7 \text{ ns} + 4 \text{ ns} \geq 2 \text{ ns} + t_{skew} \\&\Rightarrow t_{skew} \leq 9 \text{ ns}\end{aligned}$$

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* Positive skew

- Negative clock skew



Rule #7: $t_{clk} \geq t_{pmax} + t_{cmax} + t_{su} + t_{skew}$

Rule #8 : $t_{pmin} + t_{cmin} \geq t_h - t_{skew}$

Ex.

<Ans.>

(a) Max clock frequency:

i. with clock skew

$$\begin{aligned} t_{ck} &= t_{pmax} + t_{cmax} + t_{su} + t_{skew} \\ &= 9 \text{ ns} + 6 \text{ ns} + 5 \text{ ns} + 3 \text{ ns} \\ &= 23 \text{ ns} \end{aligned}$$

$$f_{max} = 1/23 \text{ ns} = 43.47 \text{ MHz}$$

ii. without clock skew (p.39)

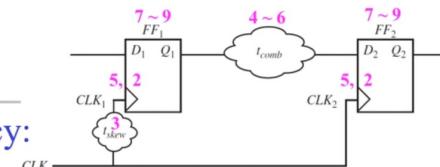
$$f_{max} = 1/20 \text{ ns} = 50 \text{ MHz}$$

(b) The biggest skew:

$$t_{pmin} + t_{cmin} \geq t_h - t_{skew} \Rightarrow 7 \text{ ns} + 4 \text{ ns} + t_{skew} \geq 2 \text{ ns}$$

$$\Rightarrow t_{skew} \geq -9 \text{ ns}$$

⇒ There will be no hold-time violation!



* Negative skew

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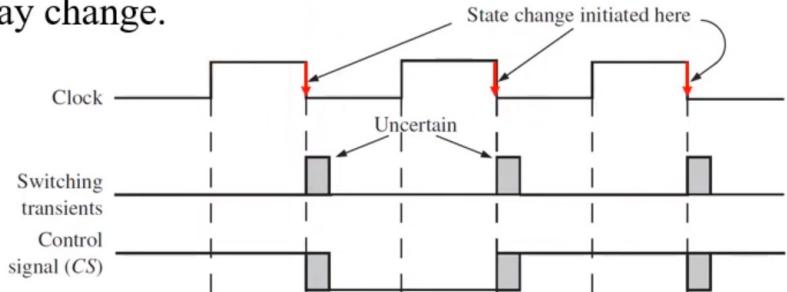
8 Glitches and Sequential Circuits

- **glitches**: temporary false values appeared at the outputs and next states. (caused by asynchronous external inputs often present in sequential circuits)

- glitches in control signals.

■ Problems of glitches in control signals:

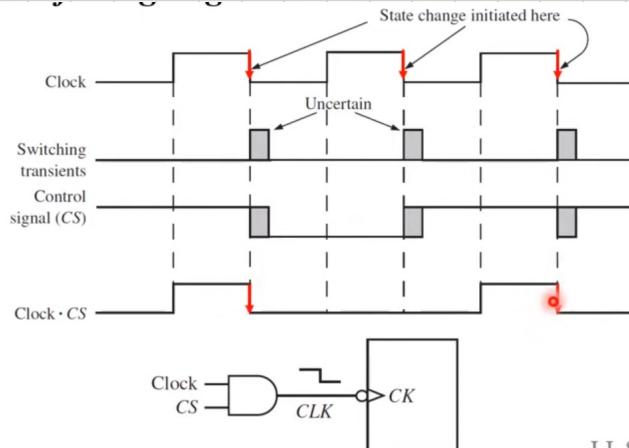
- After the triggering edge of the clock, there is a period of uncertainty during which control signals may change.



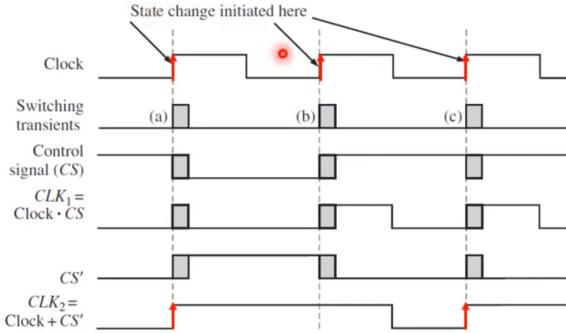
- elimination of glitches

– clock gating

- for falling-edge devices:



- for rising-edge devices:



⚠ clock gating can lead to clock skew & additional timing problems.