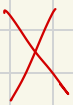
Important Verilog Tips

- DO NOT mix blocking & non-blocking assignments in an always block.

```
always begin
    a <= b;
    c = d;
end
```



- DO NOT make assignments to the same variable from more than one always block.

```
always begin
    a <= 1'b1;
end

always begin
    a <= 1'b0;
end
```