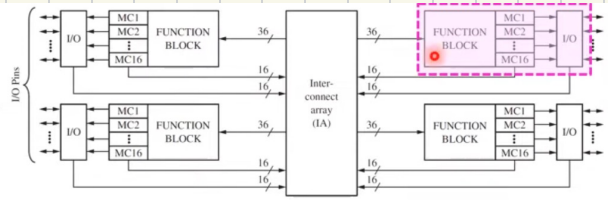
3.3 CPLDs

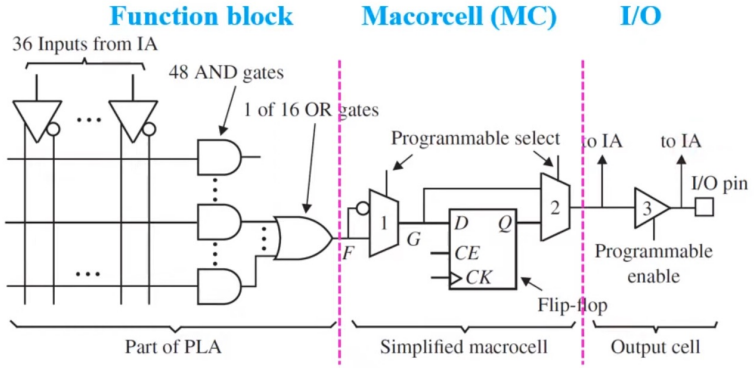
1 What are CPLDs?

- a number of PAL / PLA - like logic blocks
- a programmable interconnect matrix
  - crossbar - like switch
  - N × M crossbar switch
    - Each of the N input lines can be connected to the M output lines simultaneously.
    - Building the switches is expensive but results in predictable timing.
- storage elements : FFs

Ex1. Xilinx CoolRunner

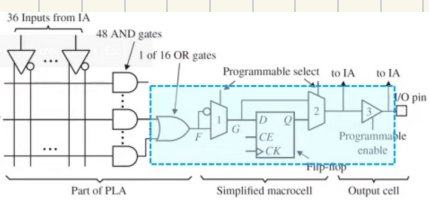


- Function block & macrocell:

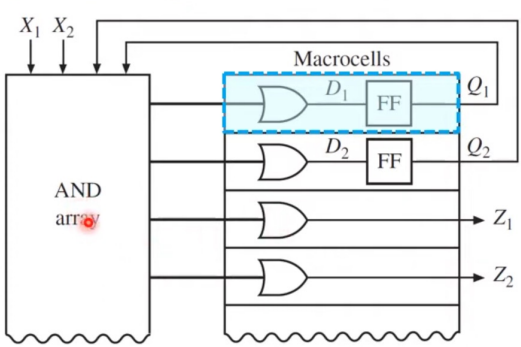


Ex2. Mealy Seq Ckt

Example: Mealy seq ckt

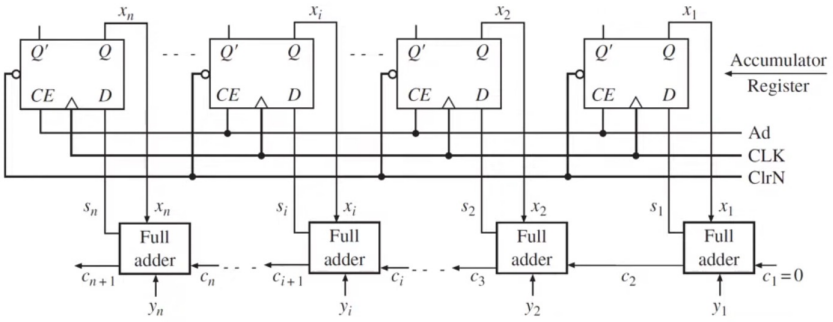


- A Mealy seq ckt w/ 2 inputs, 2 outputs, and 2 flip-flops:



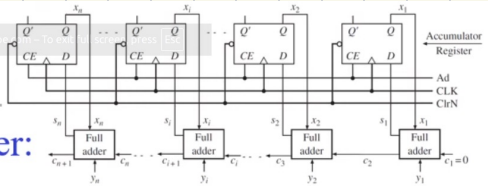
Example: N-Bit Parallel Adder w/ Accumulator

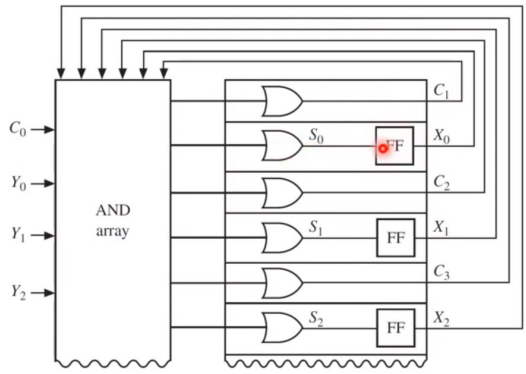
- Implement an *n*-bit parallel adder w/ an accumulator in a CPLD:



<Ans.>

- 3 bits of the adder:





For each accumulator f-f:

$$D_i = X_i^+ = S_i$$
$$= X_i \oplus Y_i \oplus C_i$$

For carry:

$$C_{i+1} = X_i Y_i + X_i C_i + Y_i C_i$$