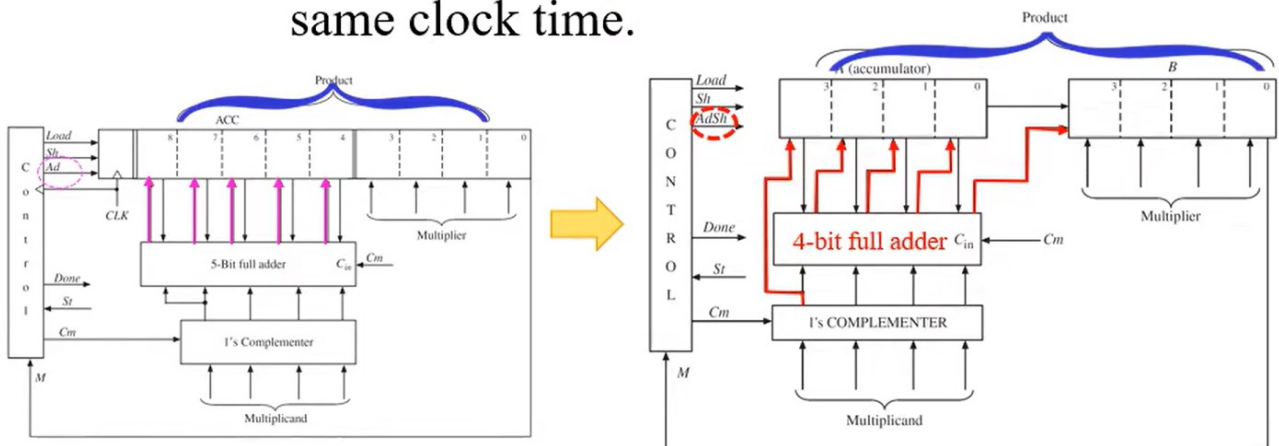


## 4.10.1 Faster Multiplier

### B. Faster Multiplier

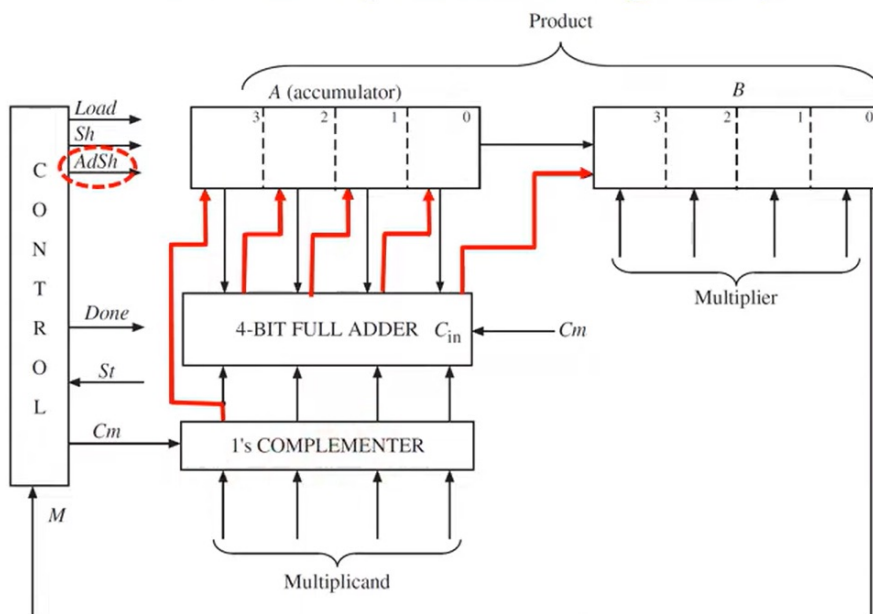
\* In Figure 4.32, the *add* and *shift* operations are done at two separate clock times.

- Speed up the operation of the multiplier:
  - Move *wires* from the *adder output* one position to the right, so adder output is shifted over one position when it is loaded into the accumulator.
  - ⇒ The *add* and *shift* operations can occur at the same clock time.



### Block Diagram

- Hardware required to multiply two 4-bit fractions (includes sign bit):

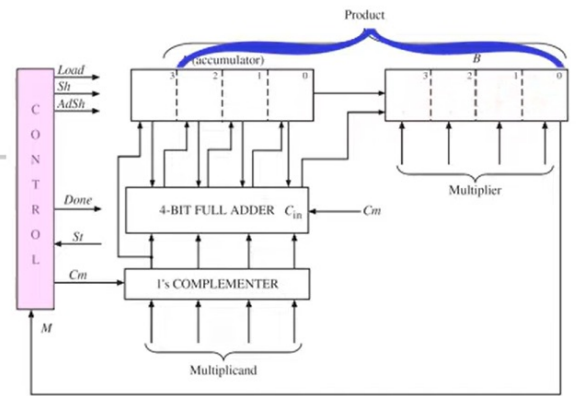
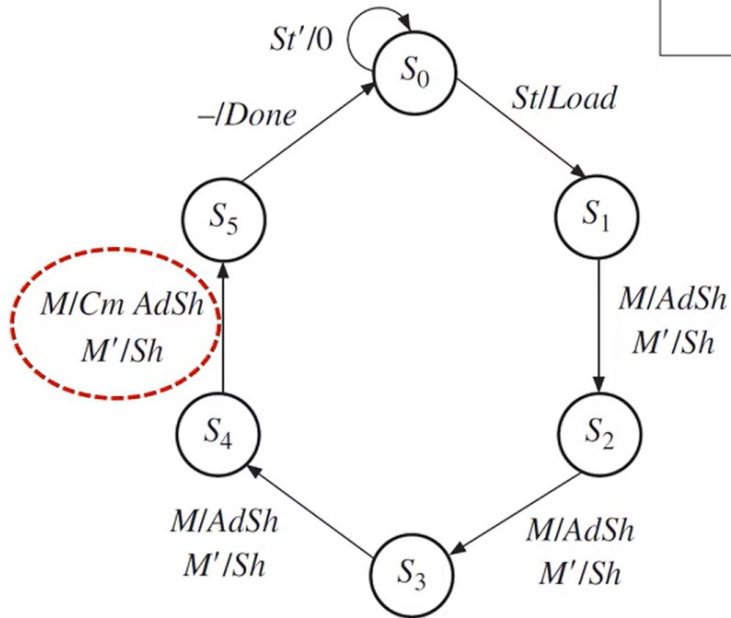


*St*: start signal  
*M*: current multiplier bit  
*Load*: load multiplier into B and clear A  
*Sh*: shift signal, causes A & B to shift right one place w/ sign extension  
*AdSh*: add and shift signal  
*Cm*: complement signal



# State Graph

- State diagram for the control circuit:



\* The add and shift operations are done at the same clock time.