Counters and Registers

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Objectives

- Understand several types of schemes used to decode different types of counters.
- Anticipate and eliminate the effects of decoding glitches.
- Compare the major differences between ring and Johnson counters.
- Analyze the operation of a frequency counter and of a digital clock.
- Recognize and understand the operation of various types of IC registers.

Synchronous Counter Design

- J-K flip-flop excitation table

Transition	Present State	Next State	J	K
0→0	0	0	0	X
0→1	0	1	1	X
1→0	1	0	X	1
1→1	1	1	X	0

Design Procedure

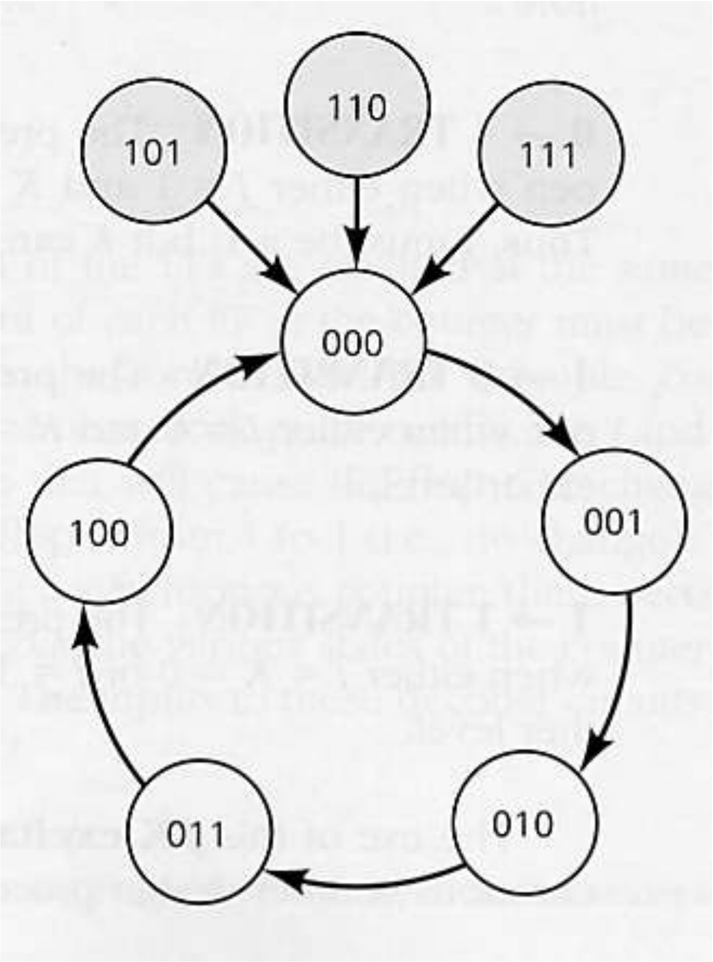
- Step1: Determine the desire number of bits (FFs) and the desired counting sequence.
- Step2: Draw the state transition diagram showing all possible states, including those that are not part of the desired counting sequence.
- Step 3: Use the state-transition diagram to set up a table that lists all PRESENT states and their NEXT states.

Design Procedure (cont'd)

- Step4: Add a column to the above table for each J and K input to produce a circuit excitation table.
- Step 5: Design the logic circuits to generate the levels required at each J and K input.
- Step 6: Implement the final expressions.

Example

- MOD-5 synchronous counter
- 000→001→010→011→100→000→…
- State transition diagram



Present and Next States

	PRESENT State			NEXT State		
	C	*B*	*A*	*C*	*B*	*A*
line 1	0	0	0	0	0	1
2	0	0	1	0	1	0
3	0	1	0	0	1	1
4	0	1	1	1	0	0
5	1	0	0	0	0	0
6	1	0	1	0	0	0
7	1	1	0	0	0	0
8	1	1	1	0	0	0

Circuit Excitation Table

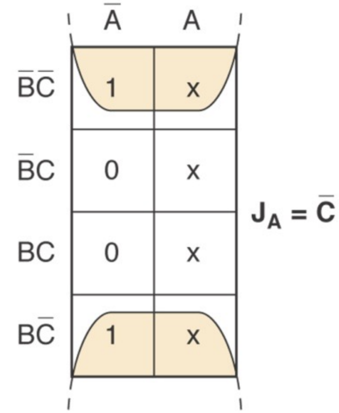
	PRESENT State			NEXT State								
	C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
line 1	0	0	0	0	0	1	0	x	0	x	1	x
2	0	0	1	0	1	0	0	x	1	x	x	1
3	0	1	0	0	1	1	0	x	x	0	1	x
4	0	1	1	1	0	0	1	x	x	1	x	1
5	1	0	0	0	0	0	x	1	0	x	0	x
6	1	0	1	0	0	0	x	1	0	x	x	1
7	1	1	0	0	0	0	x	1	x	1	0	x
8	1	1	1	0	0	0	x	1	x	1	x	1

K-maps

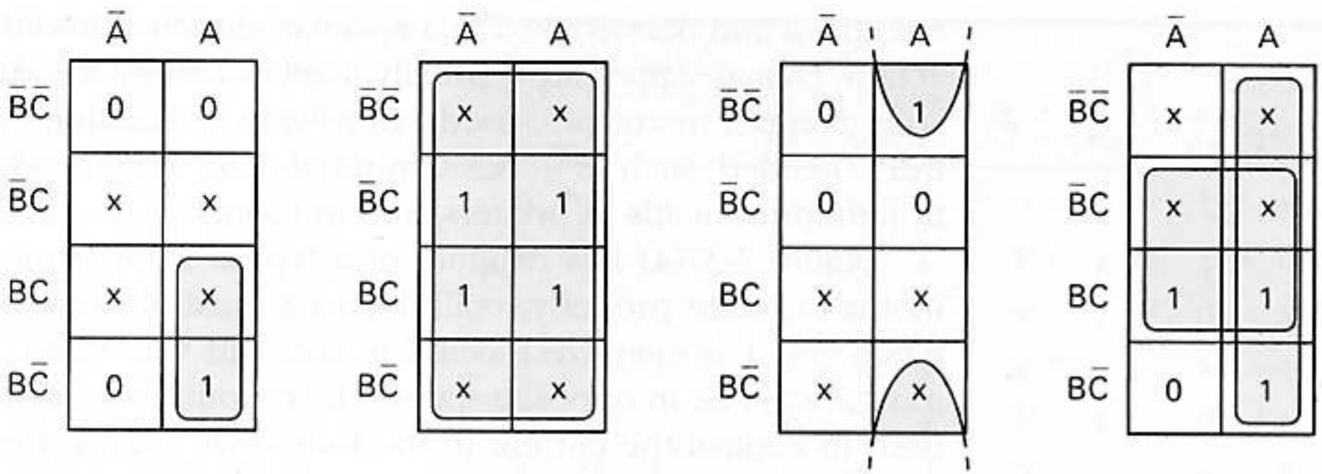
- J_A=C', K_A=1 (Figure 7-34)

PRESENT			
C	B	A	J_A
0	0	0	1
0	0	1	x
0	1	0	1
0	1	1	x
1	0	0	0
1	0	1	x
1	1	0	0
1	1	1	x

(a)

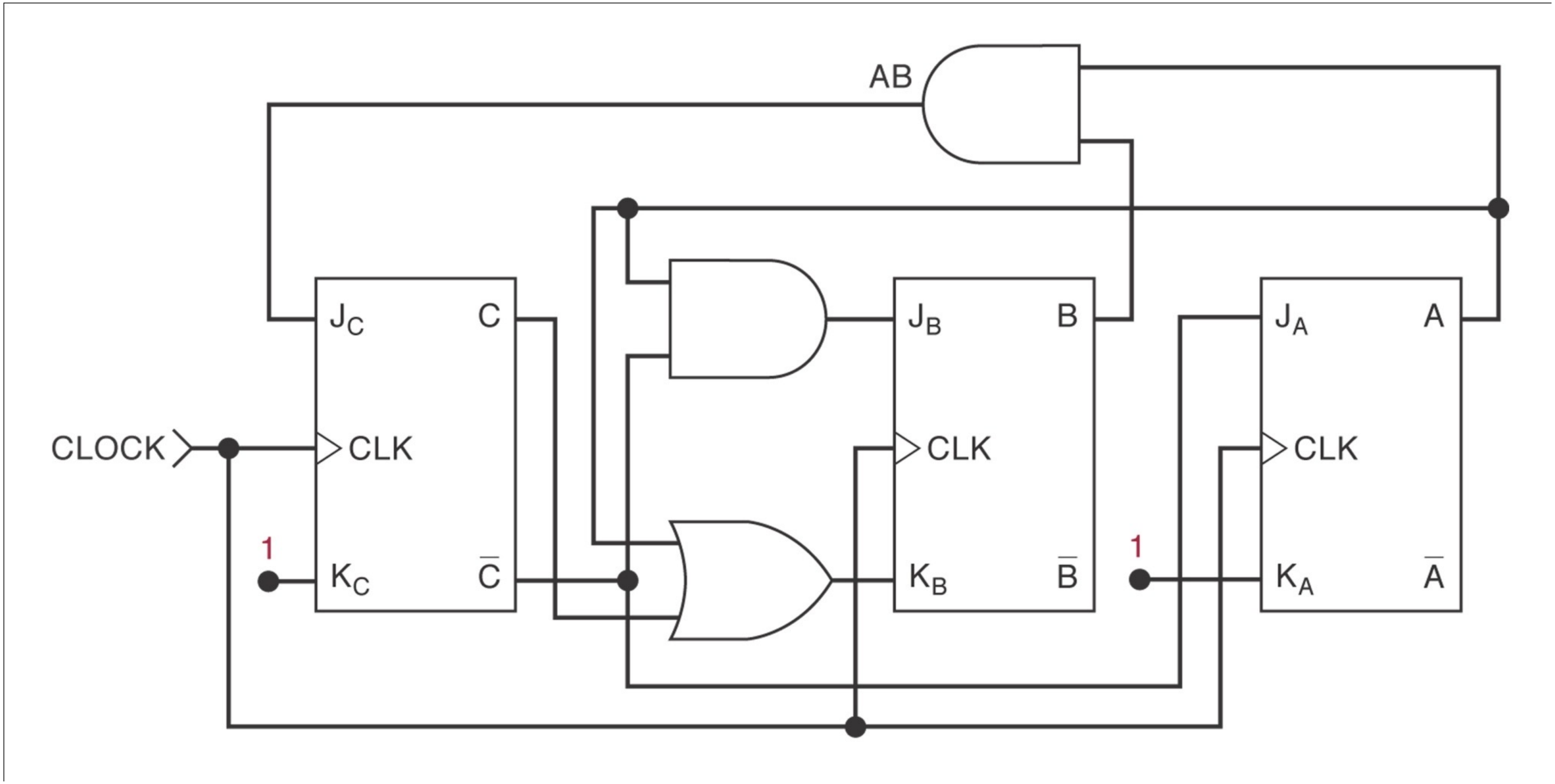


(b)



$J_C = AB$ $K_C = 1$ $J_B = A\bar{C}$ $K_B = A + C$

Final Implementation



Step Motor Control

- A step motor is a motor that rotates in steps rather than in a continuous motion, typically 15 degrees per step.
- Used in positioning of read/write heads on magnetic tapes, in controlling print heads…
- Figure 7.37: CW rotation and CCW rotation.
- Apply the design procedure to generate the circuit.

Step Motor Control (cont'd)

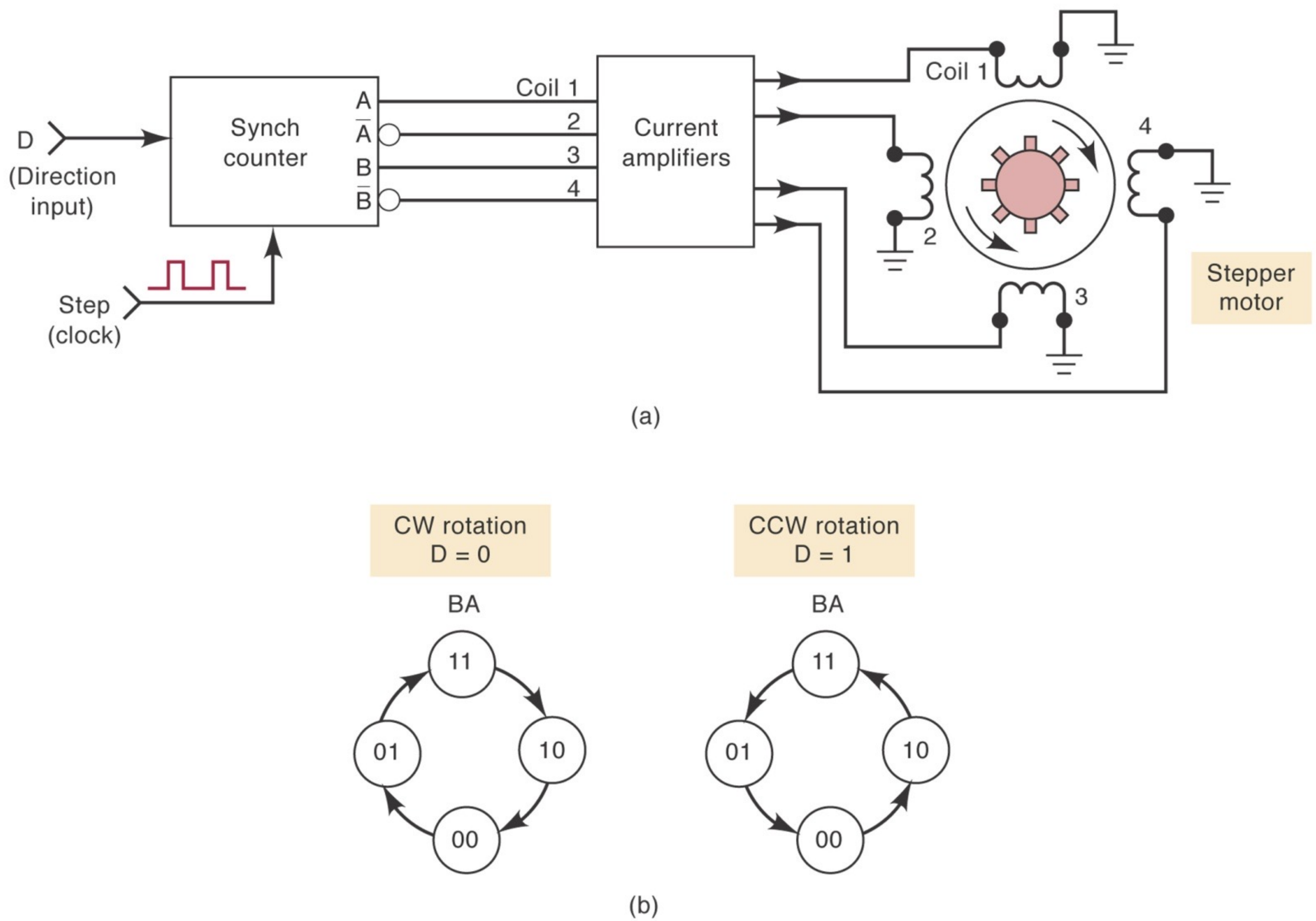
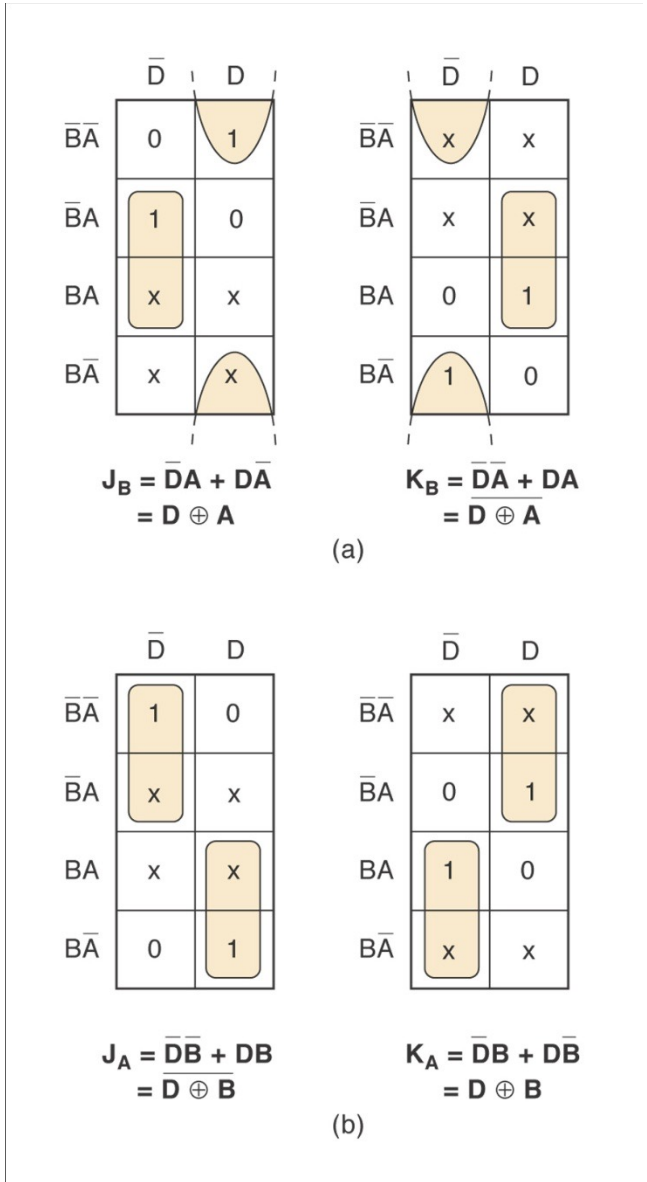
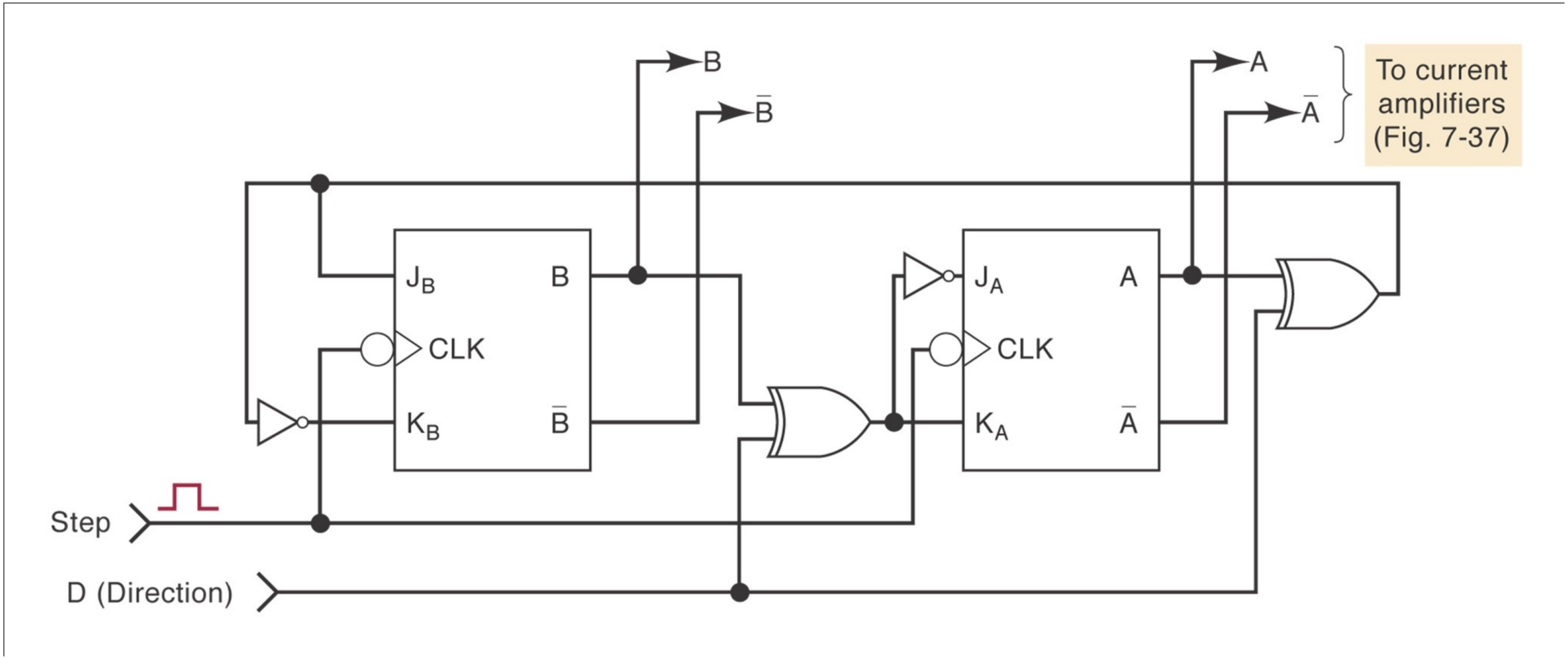


FIGURE 7-38 **(a) K maps for J_B and K_B; (b) K maps for J_A and K_A.**



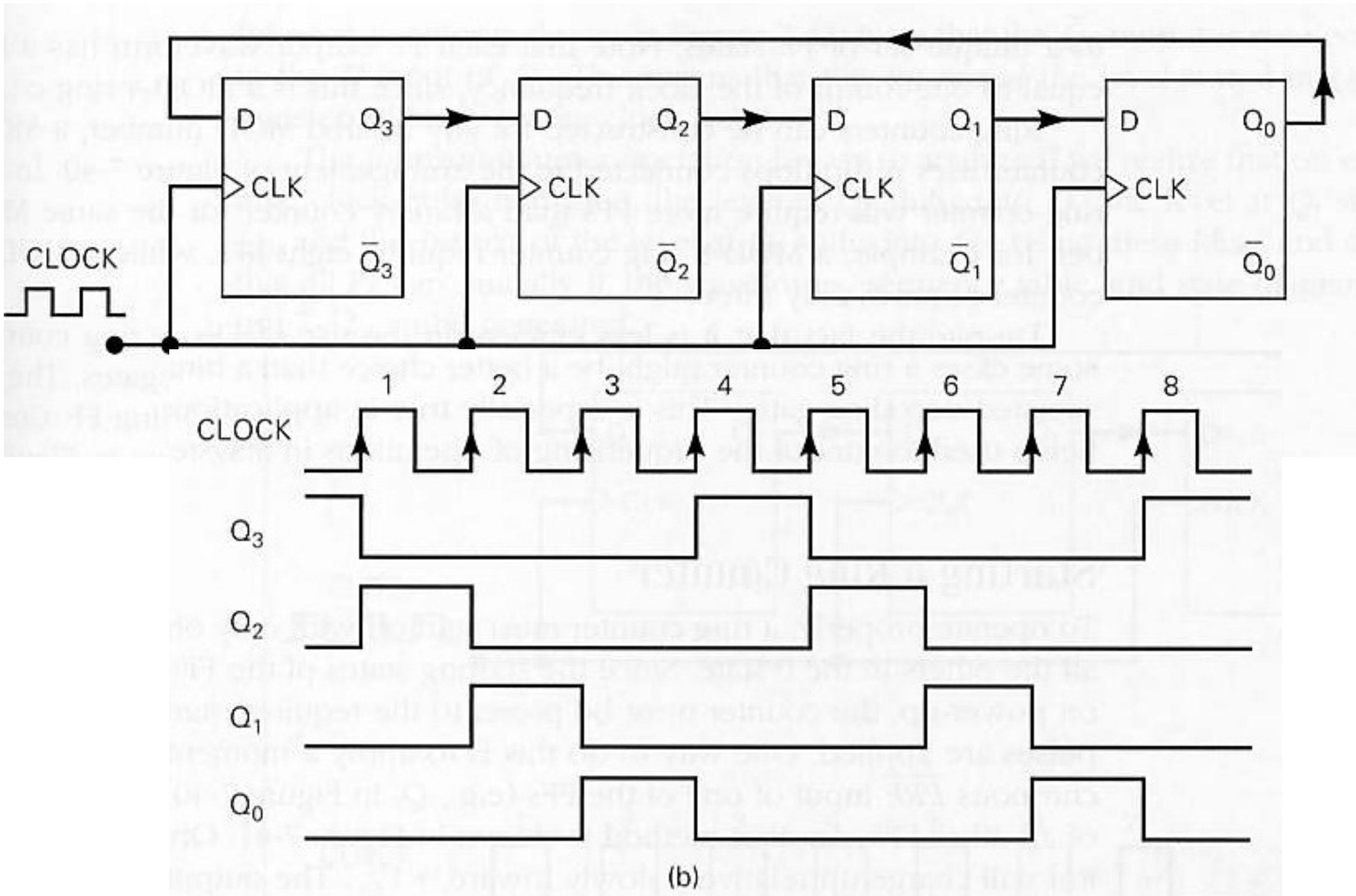
Final Implementation



Shift-Register Counters

- Use feedback, output of last FF is connected back to the first FF in some way.
- Ring counter: circulating shift register.
- See Figure 7-40.
- Why is it still a counter?

Four-Bit Ring Counter

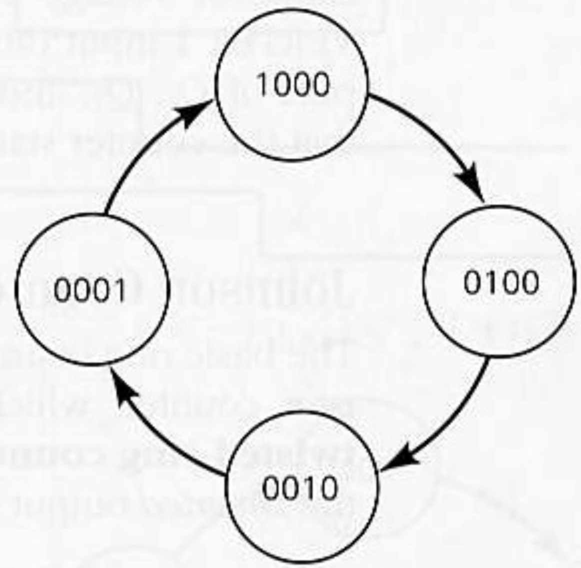


State Transition Diagram

- MOD-4 Counter
- Does not require decoding gates

Q_3	Q_2	Q_1	Q_0	CLOCK pulse
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3
1	0	0	0	4
0	1	0	0	5
0	0	1	0	6
0	0	0	1	7
.	.	.	.	.
.	.	.	.	.

(c)



(d)

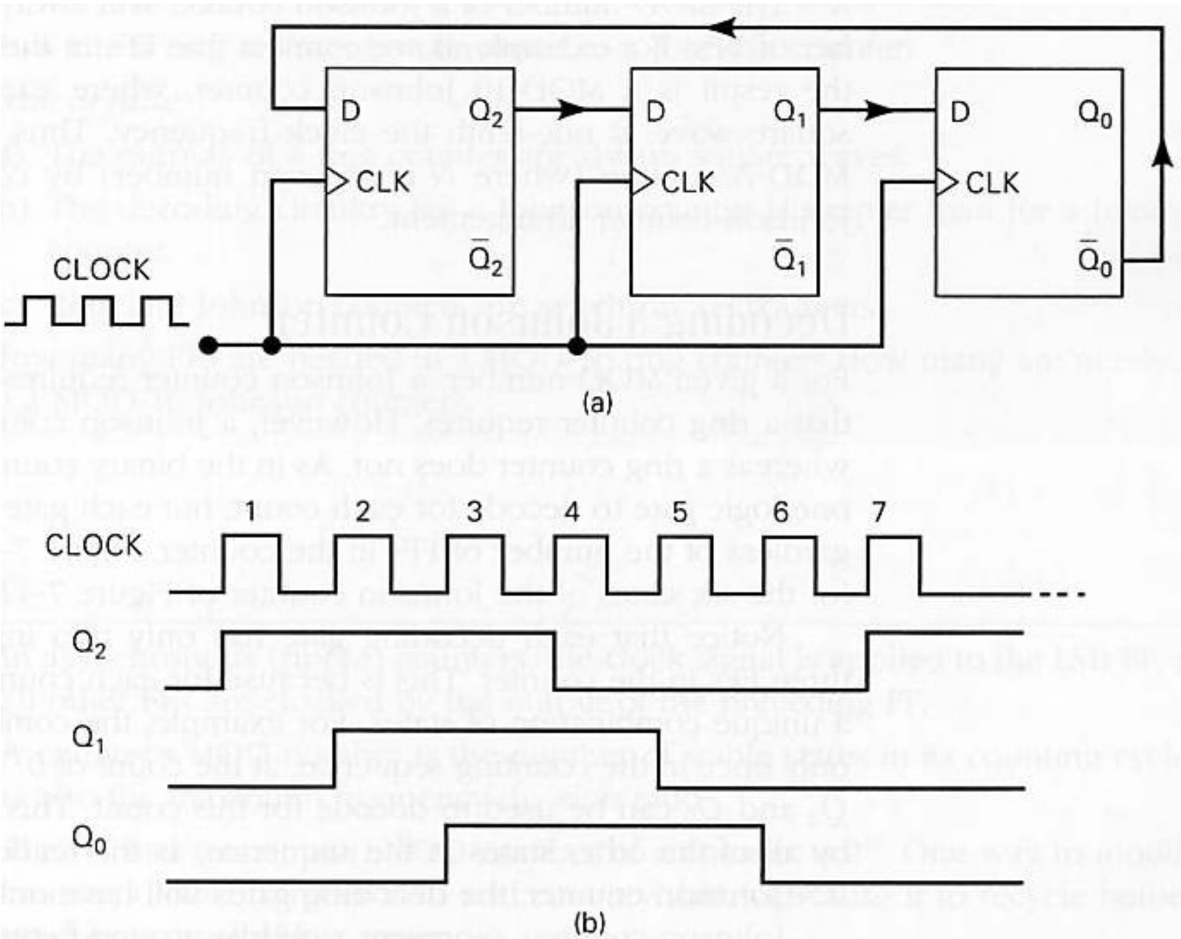
Starting a Ring Counter

- Start off with only one FF in the 1 state and all others in the 0 state.
- Use PRE and CLR inputs and Schmitt-trigger INVERTERS(page 261-262).

Johnson Counter

- Also known as the twisted-ring counter.
- Same as the ring counter except that the inverted output of the last FF is connected to the input of the first FF.
- Counting sequence: 000→100→110→111→011→001→000
- A MOD-6 counter (twice the number of FFs)
- Needs decoding gates.
- Figure 7-62

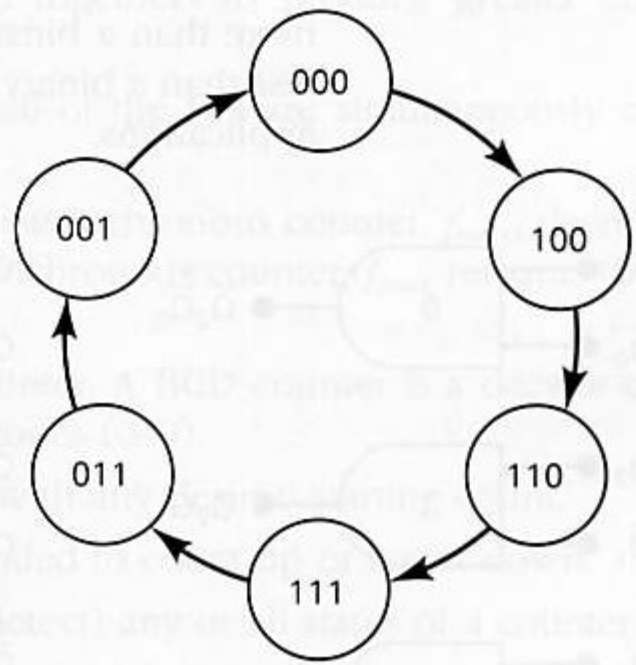
MOD-6 Johnson Counter



State Transition Diagram

Q_2	Q_1	Q_0	CLOCK pulse
0	0	0	0
1	0	0	1
1	1	0	2
1	1	1	3
0	1	1	4
0	0	1	5
0	0	0	6
1	0	0	7
1	1	0	8
.	.	.	.
.	.	.	.
.	.	.	.

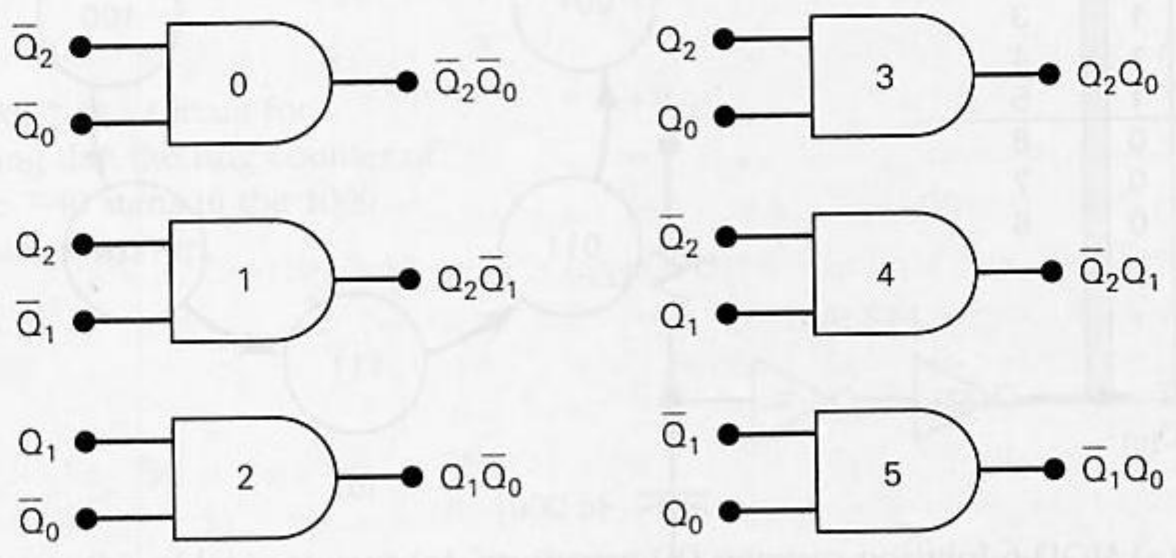
(c)



(d)

Decoding a Johnson Counter

- Each decoding has only two inputs.
- It can be shown that for any size Johnson counter, the decoding gates will have only two inputs.

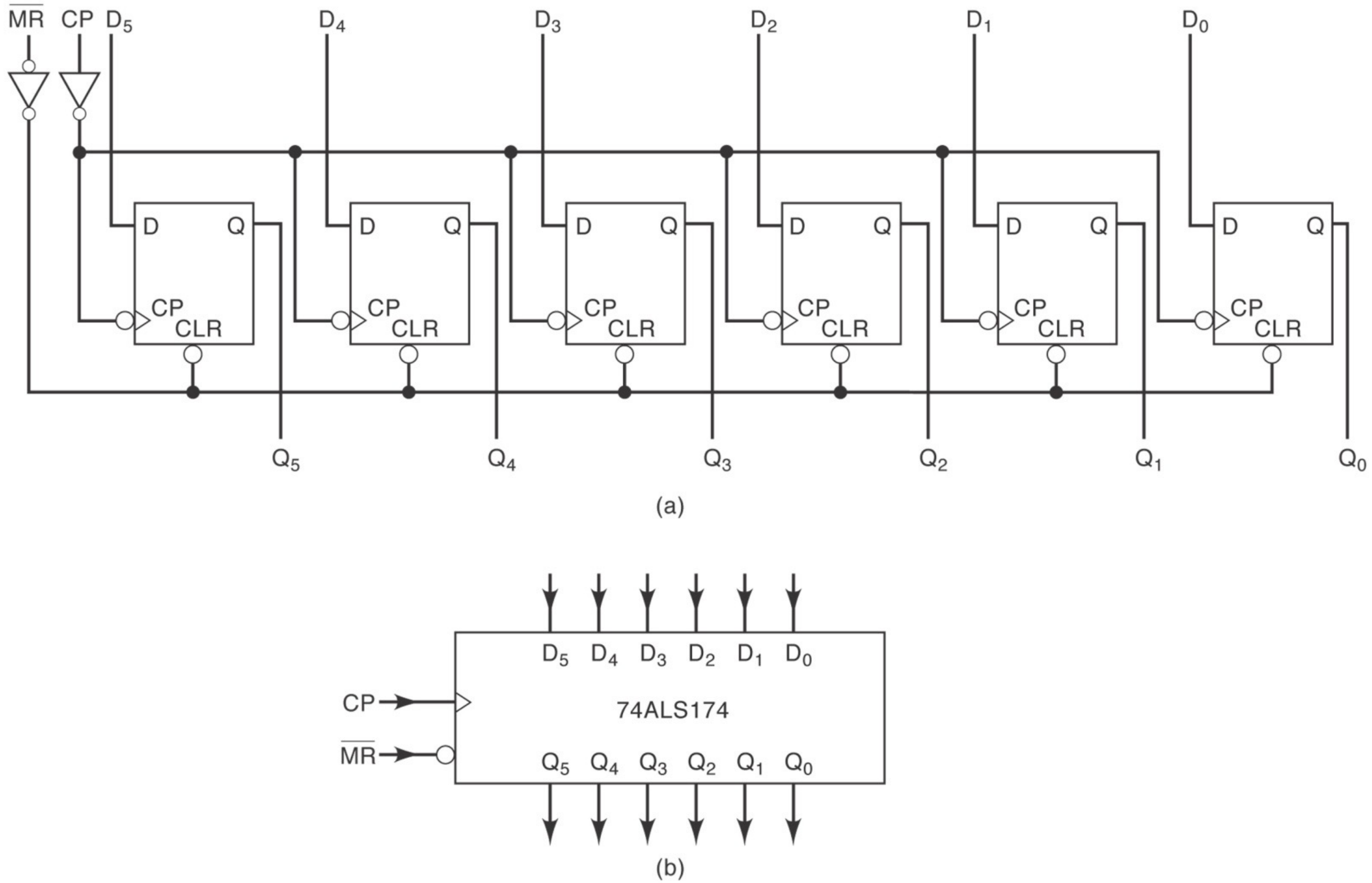


Q_2	Q_1	Q_0	Active gate
0	0	0	0
1	0	0	1
1	1	0	2
1	1	1	3
0	1	1	4
0	0	1	5

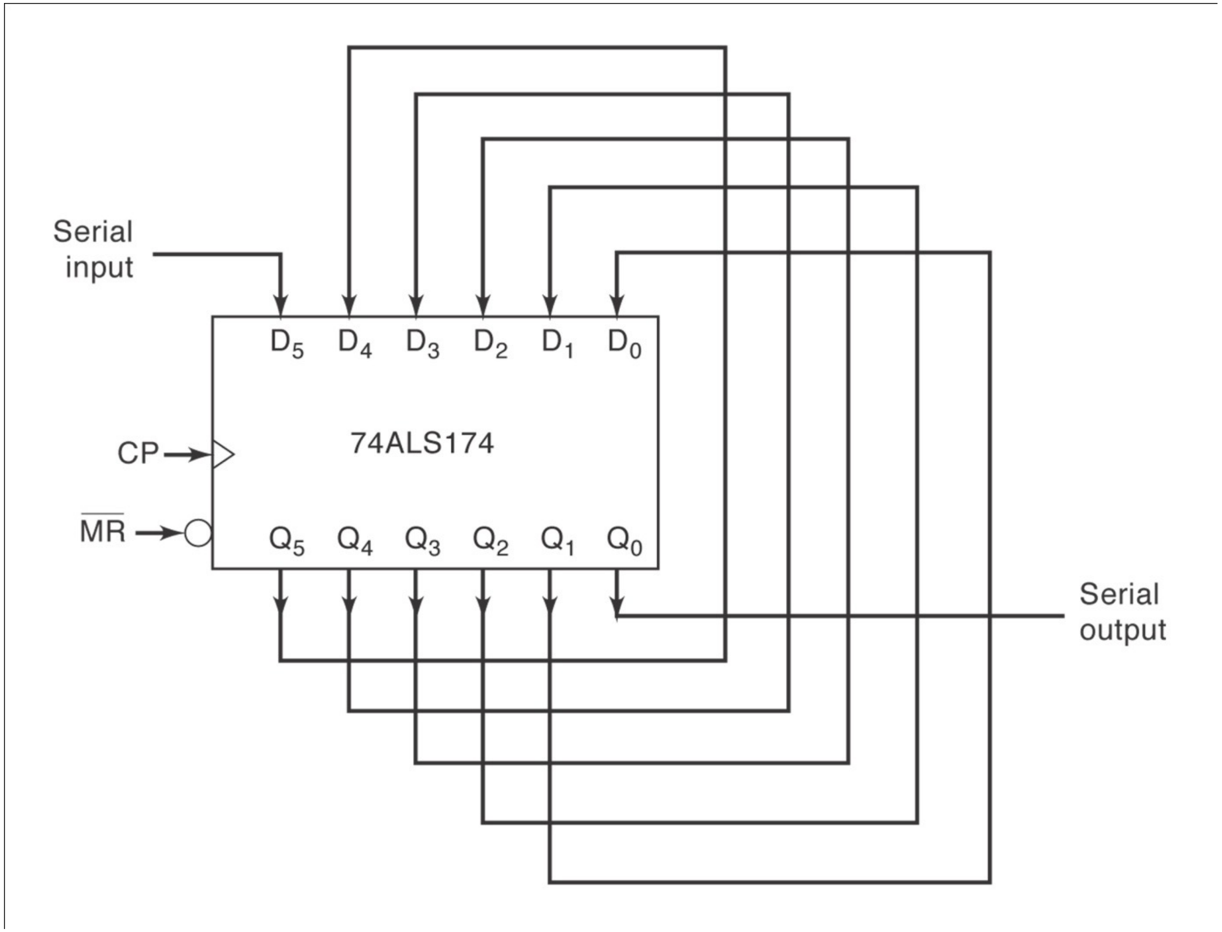
Integrated-Circuit Registers

- Parallel in/Parallel Out: 74174 and 74178
- Serial in/Serial Out: 4731B
- Parallel in/Serial Out:74165,74LS165,74HC165
- Serial in/Parallel Out: 74164,74LS164,74HC164

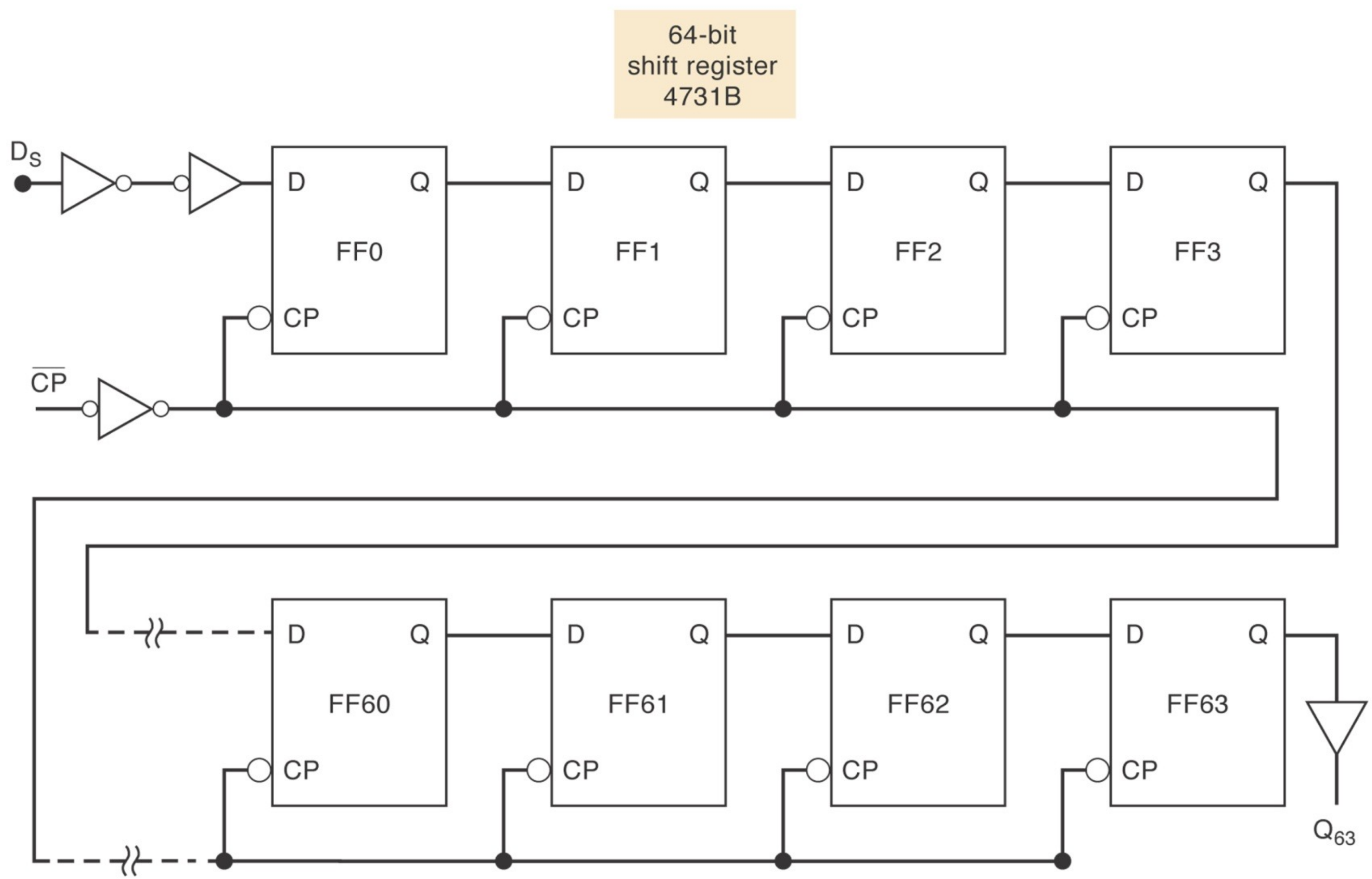
PIPO Register



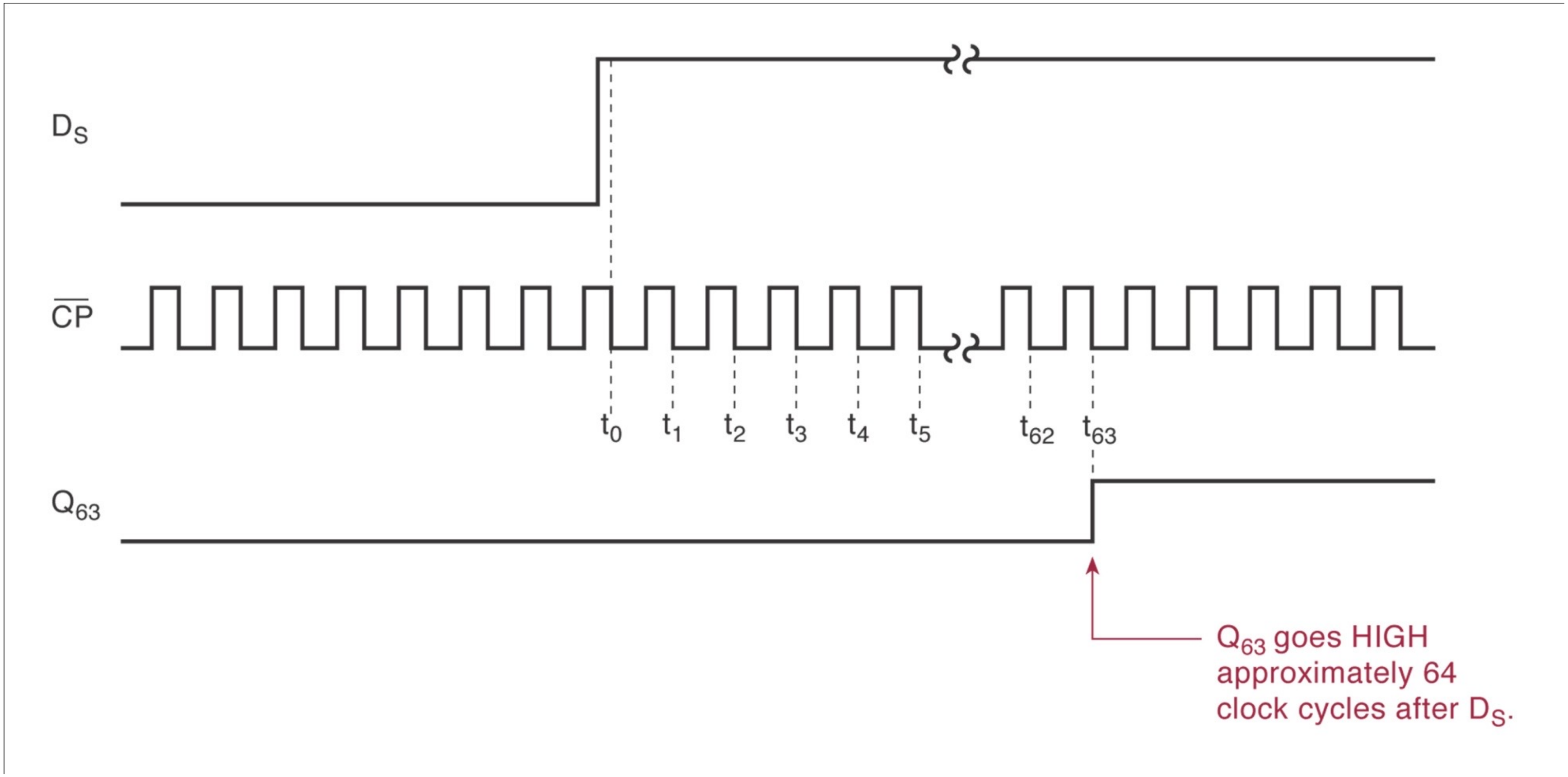
74ALS174 Wired as a Shift Register



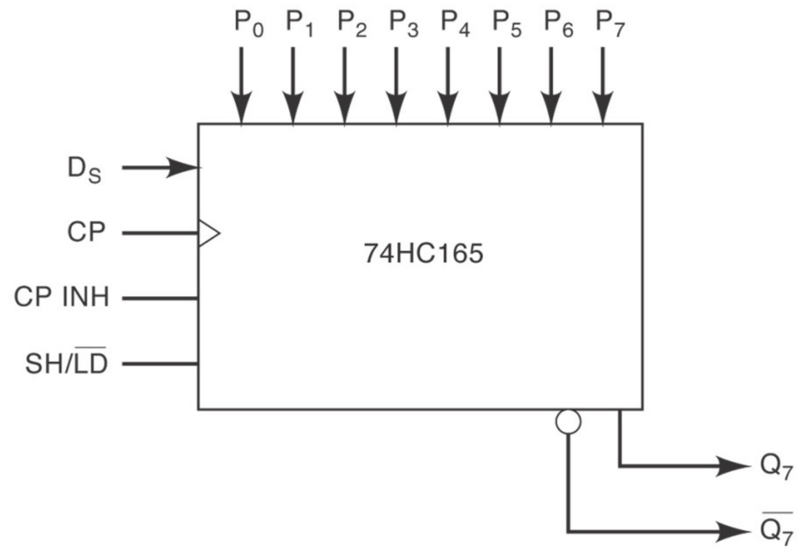
SISO Register



Delay a Digital Signal



PISO Register



(a)

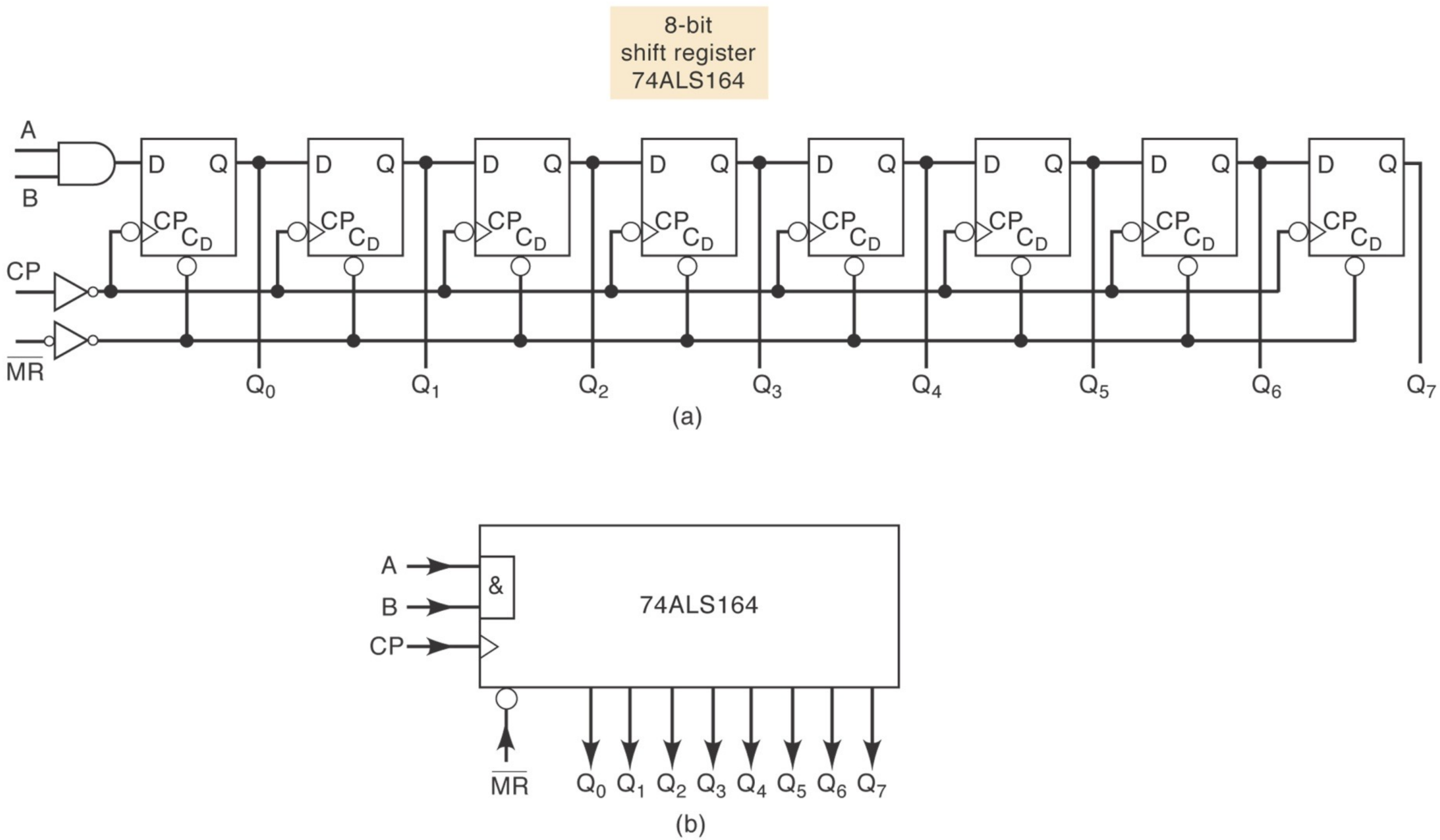
Function Table

Inputs			Operation
$SH/\overline{LD}$	CP	CP INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	↑	L	Shifting
H	L	↑	Shifting

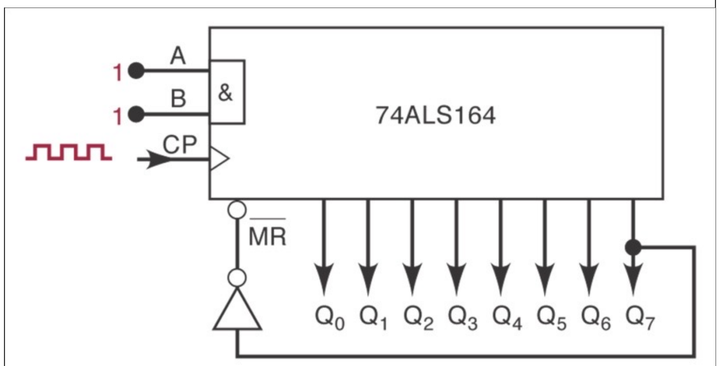
H = high level
L = low level
X = immaterial
↑ = PGT

(b)

SIPO Register



Example 7-23



(a)

Input pulse number	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1

Recycles

Temporary state

(b)