AN3393
Application note

L3G4200D: three axis digital output gyroscope

Introduction

This document is intended to provide usage information and application hints related to ST L3G4200D 3-axial digital gyroscope.

The L3G4200D is an is three-axis angular rate sensor, with a digital I^2C/SPI serial interface standard output.

The device has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

The device may be configured to generate interrupt signals by an independent wake-up event. Thresholds and timing of the interrupt generator are programmable by the end user on the fly.

The L3G4200D has an integrated 32-level first in first out (FIFO) buffer allowing the user to store data for host processor intervention reduction.

The L3G4200D is available in a small thin plastic land grid array package (LGA 4x4x1.1) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

The ultra small size and weight of the SMD package make it an ideal choice for handheld portable applications such as cell phones and PDAs, or any other application where reduced package size and weight are required.

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1 Registers table

Table 1. Registers table

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WHO_AM_I	0Fh	1	1	0	1	0	0	1	1
CTRL_REG1	20h	DR1	DR0	BW1	BW0	PD	Zen	Yen	Xen
CTRL_REG2	21h	0	0	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0
CTRL_REG3	22h	I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty
CTRL_REG4	23h	BDU	BLE	FS1	FS0	-	ST1	ST0	SIM
CTRL_REG5	24h	BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0
REFERENCE	25h	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
OUT_TEMP	26h	Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
STATUS_REG	27h	ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
OUT_X_L	28h	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
OUT_X_H	29h	XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8
OUT_Y_L	2Ah	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
OUT_Y_H	2Bh	YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8
OUT_Z_L	2Ch	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
OUT_Z_H	2Dh	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8
FIFO_CTRL_REG	2Eh	FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0
FIFO_SRC_REG	2Fh	WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0
INT1_CFG	30h	AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
INT1_SRC	31h	-	IA	ZH	ZL	YH	YL	XH	XL
INT1_TSH_XH	32h	-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8
INT1_TSH_XL	33h	THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
INT1_TSH_YH	34h	-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 1. Registers table (continued)

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT1_TSH_YL	35h	THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
INT1_TSH_ZH	36h	-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8
INT1_TSH_Z	37h	THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
INT1_DURATION	38h	WAIT	D6	D5	D4	D3	D2	D1	D0

2 Operating modes

The L3G4200D provides three different operating modes, respectively reported as power-down mode, sleep mode and normal mode.

After power supply is applied, the L3G4200D performs a 10 ms boot procedure to load the trimming parameter. After the boot is completed, the device is automatically configured in power-down mode.

Referring to the L3G4200D datasheet, output data rate (ODR), power down (PD) and Zen, Yen, Xen bits of CTRL_REG1 are used to select the operating modes (power-down mode, low power mode and normal mode) and output data rate (*Table 2* and *Table 3*).

Table 2. Operating mode selection

Operating mode	PD	Zen	Yen	Xen
Power down	0	-	-	-
Sleep	1	0	0	0
Normal mode	1	-	-	-

Table 3. Data rate configuration

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-off LPF1 [Hz]	Cut-off LPF2 [Hz]
00	00	100	32	12.5
00	01	100		25
00	10	100		25
00	11	100		25
01	00	200	54	12.5
01	01	200		25
01	10	200		50
01	11	200		70
10	00	400	78	20
10	01	400		25
10	10	400		50
10	11	400		110
11	00	800	93	30
11	01	800		35
11	10	800		50
1	11	800		110

Table 4 shows the typical values of the power consumption for the different operating modes. Power consumption in normal mode is independent on selected ODR.

Table 4. Power consumption

Operating mode	Power consumption
Power-down	5 µA
Sleep	1.5 mA
Normal	6.1 mA

2.1 Power-down mode

When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. Digital interfaces (I^2C and SPI) are still active to allow communication with the device. The configuration registers content is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

2.2 Sleep mode

While the device is in sleep mode the driving circuitry making the moving mass of the gyroscope oscillating is kept active. Turn-on time from sleep mode to normal mode is drastically reduced.

2.3 Normal mode

In normal mode, data are generated at the data rate (ODR) selected through the DR bits. Data interrupt generation is active and configured through the INT1_CFG register.

2.4 Switch mode timing

Switch mode time is shown in *Table 5*.

Table 5. Turn-on time

Starting mode	Target mode	Turn-on time - TYP
Power-down	Normal	250 ms
Power-down	Self test	250 ms
Sleep	Normal	1/ODR: LPF2 disabled 6/ODR: LPF2 enabled
Normal	Sleep	immediate
Normal	Power-down	immediate
Other settings change	-	1/ODR: LPF2 disabled 6/ODR: LPF2 enabled

3 Startup sequence

Once the device is powered-up, it automatically downloads the calibration coefficients from the embedded flash to the internal registers. When the boot procedure is completed, i.e. after approximately 5 milliseconds, the device automatically enters power-down mode. To turn-on the device and gather angular rate data, it is necessary to select one of the operating modes through CTRL_REG1 and to enable at least one of the axes.

The following general purpose sequence can be used to configure the device:

1. Write CTRL_REG2
2. Write CTRL_REG3
3. Write CTRL_REG4
4. Write CTRL_REG6
5. Write Reference
6. Write INT1_THS
7. Write INT1_DUR
8. Write INT1_CFG
9. Write CTRL_REG5
10. Write CTRL_REG1

3.1 Reading angular rate data

3.1.1 Using the status register

The device is provided with a STATUS_REG which should be polled to check when a new set of data is available. The reading procedure should be the following:

1. Read STATUS_REG
2. If STATUS_REG(3) = 0 then go to 1
3. If STATUS_REG(7) = 1 then some data have been overwritten
4. Read OUT_X_L
5. Read OUT_X_H
6. Read OUT_Y_L
7. Read OUT_Y_H
8. Read OUT_Z_L
9. Read OUT_Z_H
10. Data processing
11. Go to 1

The check performed at step 3 allows to understand whether the reading rate is adequate compared to the data production rate. In case one or more angular rate samples have been overwritten by new data, because of a too slow reading rate, the ZYXOR bit of STATUS_REG is set to 1.

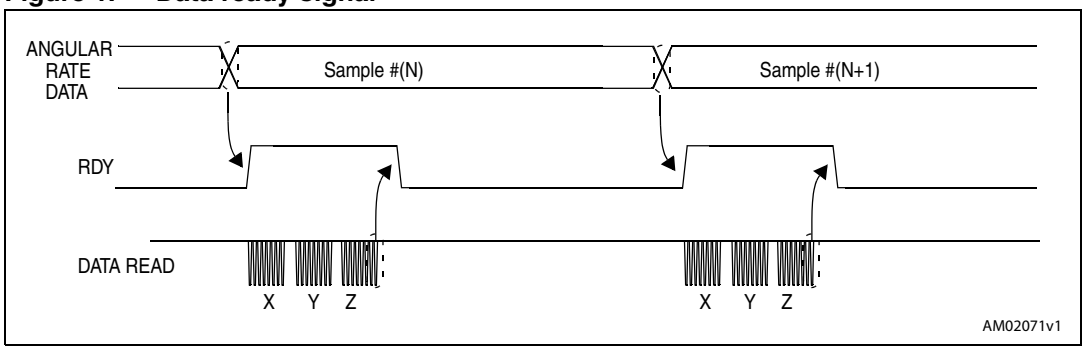
The overrun bits are automatically cleared when all the data present inside the device have been read and new data have not been produced in the meantime.

3.1.2 Using the data-ready (DRY) signal

The device may be configured to have one HW signal to determinate when a new set of measurement data is available for reading. This signal is represented by the XYZDA bit of STATUS_REG. The signal can be driven to DRY/INT2 pin by setting the I2_DRDY bit of CTRL_REG3 to 1 and its polarity set to active-low or active-high through the H_Lactive bit of CTRL_REG3 (see *Section 5.1*).

The data-ready signal rises to 1 when a new set of angular rate data has been generated and it is available for reading.The interrupt is reset when the higher part of one of the enabled channels has been read (29h, 2Bh, 2Dh).

Figure 1. Data ready signal



3.1.3 Using the block data update (BDU) feature

If the reading of the angular rate data is particularly slow and cannot be synchronized (or it is not required) with either the XYZDA bit present inside the STATUS_REG or with the RDY signal, it is strongly recommended to set the BDU (block data update) bit in CTRL_REG4 to 1.

This feature avoids the reading of values (most significant and least significant parts of the angular rate data) related to different samples. In particular, when the BDU is activated, the data registers related to each channel always contain the most recent angular rate data produced by the device, but, in case the reading of a given pair (i.e. OUT_X_H and OUT_X_L, OUT_Y_H and OUT_Y_L, OUT_Z_H and OUT_Z_L) is initiated, the refresh for that pair is blocked until both MSB and LSB parts of the data are read.

Note: BDU only guarantees that OUT_X(Y, Z)_L and OUT_X(Y,Z)_H have been sampled at the same moment. For example, if the reading speed is too low, it may read X and Y sampled at T1 and Z sampled at T2.

3.2 Understanding angular rate data

The measured angular rate data are sent to OUT_X_H, OUT_X_L, OUT_Y_H, OUT_Y_L, OUT_Z_H, and OUT_Z_L registers. These registers contain, respectively, the most significant part and the least significant part of the angular rate signals acting on the X, Y, and Z axes.

The complete angular rate data for the X (Y, Z) channel is given by the concatenation OUT_X_H & OUT_X_L (OUT_Y_H & OUT_Y_L, OUT_Z_H & OUT_Z_L) and it is expressed as a 2's complement number.

3.2.1 Data alignment

Angular rate data are represented as 16-bit numbers and are left justified.

3.2.2 Big-little endian selection

The L3G4200D allows to swap the content of the lower and the upper part of the angular rate registers (i.e. OUT_X_H with OUT_X_L), to be compliant with both little-endian and big-endian data representations.

"Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first). This mode corresponds to bit BLE in CTRL_REG4 reset to 0 (default configuration).

On the contrary, "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

3.2.3 Example of angular rate data

Table 6 provides a few basic examples of the data that is read in the data-registers when the device is subject to a given angular rate. The values listed in the table are given under the hypothesis of perfect device calibration (i.e. no offset, no gain error,....) and practically show the effect of the BLE bit.

Table 6. Output data registers content vs. angular rate (FS = 250 *dps*)

Angular rate values	BLE = 0		BLE = 1	
	Register address			
	28h	29h	28h	29h
0 dps	00h	00h	00h	00h
100 dps	A4h	2Ch	2Ch	A4h
200 dps	49h	59h	59h	49h
-100 dps	5Ch	C4h	C3h	5Ch
-200 dps	B7h	A6h	A6h	B7h

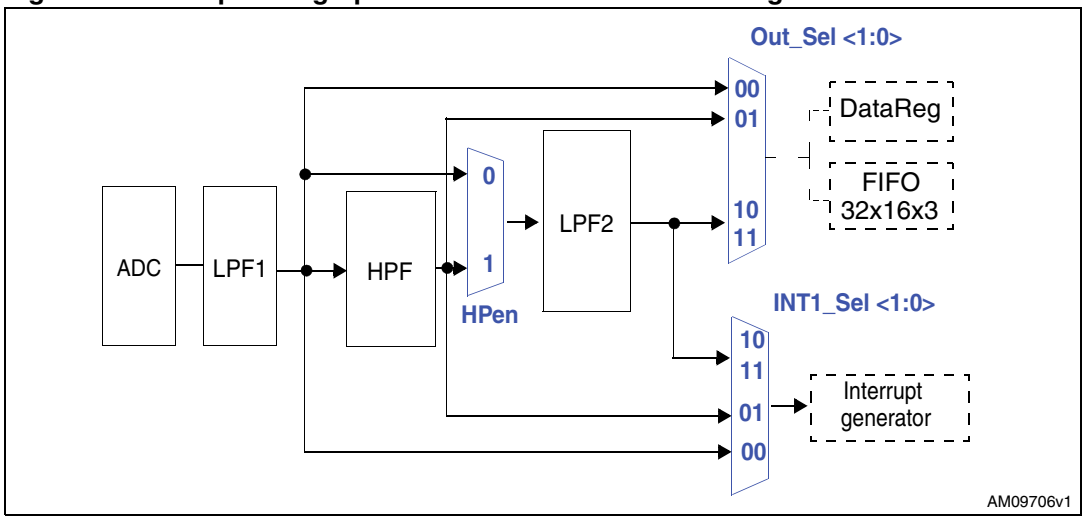
4 Digital filters

The L3G4200D provides embedded low-pass and as well as high-pass filtering capability to easily delete the DC component of the measured angular rate. As shown in *Figure 2*, through HPen, INTx_Sel and Out_Sel bits of CTRL_REG5 configuration, it is possible to independently apply the filter on the output/fifo data and/or on the interrupts data. This means that it is possible, i.e., to get filtered data while interrupt generation works on unfiltered data.

Table 7. CTRL_REG5 register

BOOT	FIFO_EN	-	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Figure 2. Low-pass/High-pass filter connections block diagram



4.1 Filters configuration

Referring to *Table 8*, HPen and Out_sel bits are used to drive unfilterd or filterd data to the output registers and to the FIFO:

Table 8. Out_Sel configuration setting

Hpen	OUT_SEL1	OUT_SEL0	Description
x	0	0	Data in DataReg and FIFO are non-high-pass-filtered
x	0	1	Data in DataReg and FIFO are high-pass-filtered
0	1	x	Data in DataReg and FIFO are low-pass-filtered by LPF2
1	1	x	Data in DataReg and FIFO are high-pass and low-pass-filtered by LPF2

Referring to *Table 9*, HPen and Int_sel bits are used to drive unfilterd or filterd data to the interrupt generator circuitry:

Table 9. INT_SEL configuration setting

Hpen	INT_SEL1	INT_SEL2	Description
x	0	0	Non-high-pass-filtered data are used for interrupt generation
x	0	1	High-pass-filtered data are used for interrupt generation
0	1	x	Low-pass-filtered data are used for interrupt generation
1	1	x	High-pass and low-pass-filtered data are used for interrupt generation

4.2 Low pass filters

The bandwidth of the low-pass filters depends on the selected ODR. The low-pass filters cut-off frequencies (f_t) are shown in *Table 12*.

Table 10. Low pass filters cut-off frequency

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-off LPF1 [Hz]	Cut-off LPF2 [Hz]
00	00	100	32	12.5
00	01	100		25
00	10	100		25
00	11	100		25
01	00	200	54	12.5
01	01	200		25
01	10	200		50
01	11	200		70
10	00	400	78	20
10	01	400		25
10	10	400		50
10	11	400		110
11	00	800	93	30
11	01	800		35
11	10	800		50
1	11	800		110

4.3 High Pass filter

The bandwidth of the high-pass filter depends on the selected ODR and on the settings of HPCFx bits of CTRL_REG2. The high-pass filter cut-off frequencies (f_t) are shown in *Table 12*.

Table 11. CTRL_REG2 register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. Value loaded at boot. This value must not be changed

Table 12. High pass filter cut-off frequency [Hz]

HPCF3-0	ODR [Hz]			
	100	200	400	800
0000	8	15	30	56
0001	4	8	15	30
0010	2	4	8	15
0011	1	2	4	8
0100	0.5	1	2	4
0101	0.2	0.5	1	2
0110	0.1	0.2	0.5	1
0111	0.05	0.1	0.2	0.5
1000	0.02	0.05	0.1	0.2
1001	0.01	0.02	0.05	0.1

Referring to *Table 13*, three operating modes are possible for the high-pass filter:

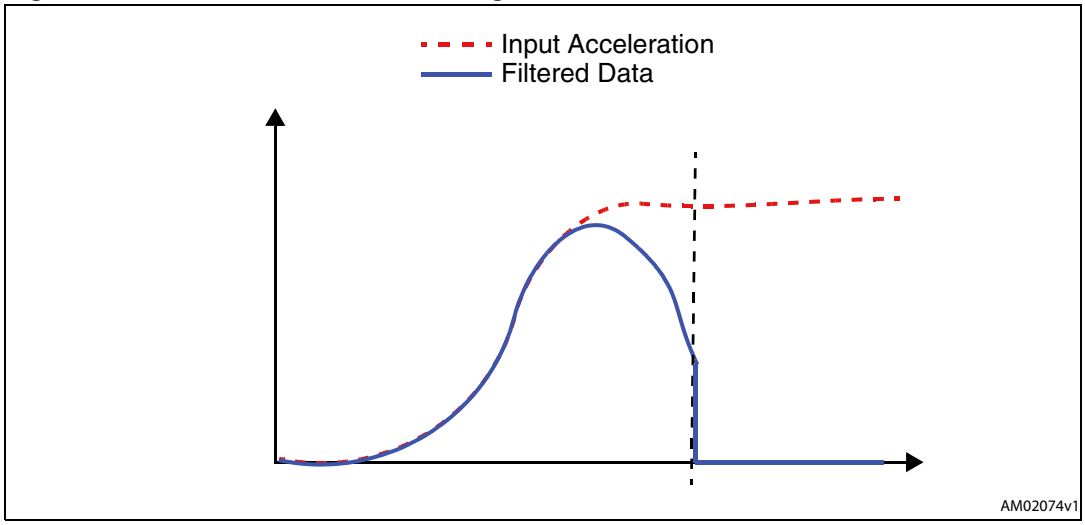
Table 13. High pass filter mode configuration

HPM1	HPM0	High Pass filter Mode
0	0	Normal mode (reset reading REFERENCE register)
0	1	Reference signal for filtering
1	0	Normal mode (reset reading REFERENCE register)
1	1	Autoreset on interrupt event

4.3.1 Normal mode

In this configuration the high-pass filter can be reset reading the REFERENCE register, instantly deleting the DC component of the angular rate.

Figure 3. HP_FILTER_RESET readings



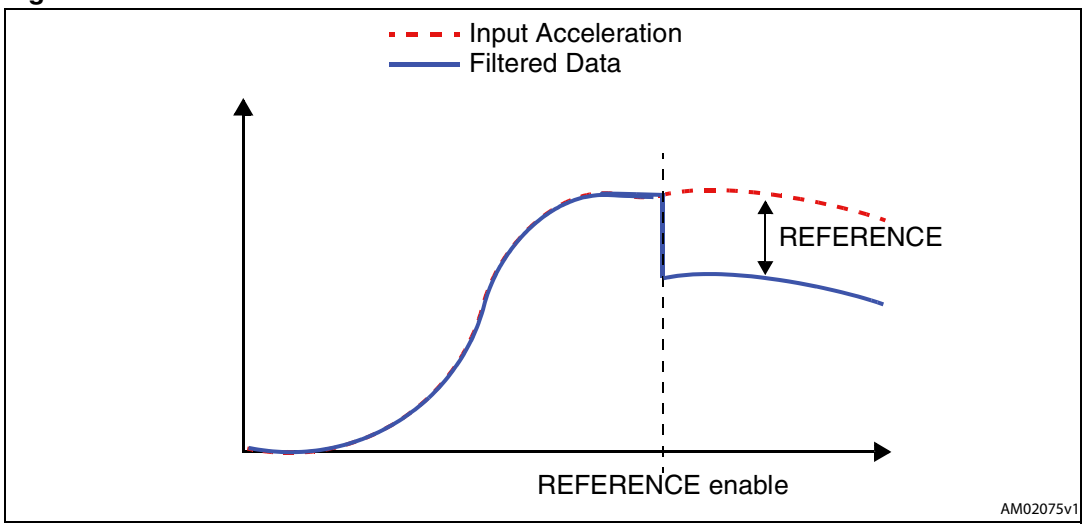
4.3.2 Reference mode

In this configuration the output data is calculated as the difference between the input angular rate and the content of the reference register. This register is in 2' complement representation and the value of 1 LSB of these 8-bit registers depends on the selected full scale (*Table 14*).

Table 14. Reference mode LSB value

Full scale	Reference mode LSB value (mdps)
250	~2
500	~4
2000	~16

Figure 4. Reference mode

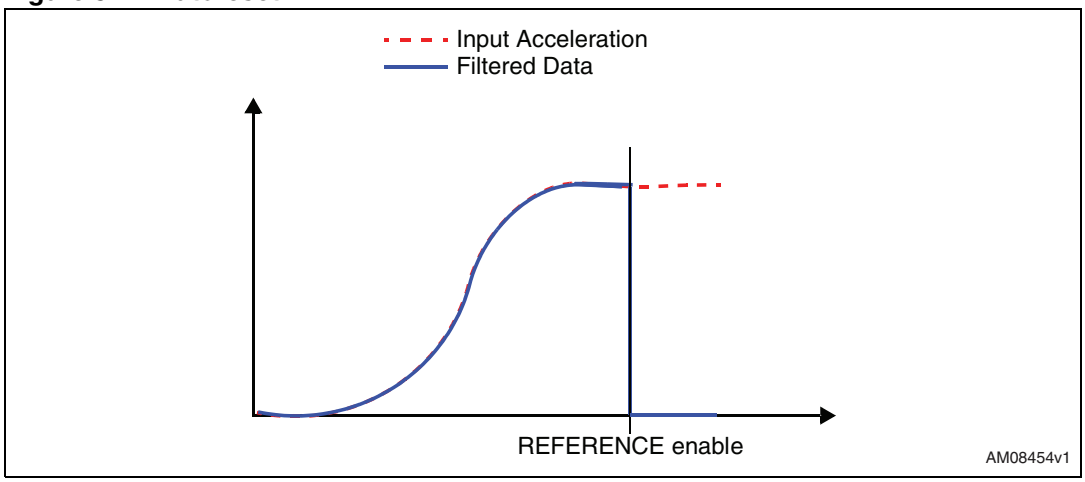


4.3.3 Autoreset

In this configuration the filter is automatically reset when the configured interrupt event occurs. HP_RESET is, however, used to set the filter instantaneously.

Note: XYZ dataset used to reset the filter is the one after the interrupt.

Figure 5. Autoreset



5 Interrupt generation

The L3G4200D interrupt signal can be configured in a very flexible way allowing to recognize independent rotations of X,Y and Z axis. That signal can be driven to INT1pin. INT2 pin is dedicated to DRY and FIFO interrupts.

5.1 Interrupt pin configuration

The device is provided with two pins which can be activated to generate either the data-ready or the interrupt signals. The functionality of the pins is selected through CTRL_REG3(22h). Refer to and to the block diagram given in *Figure 6*.

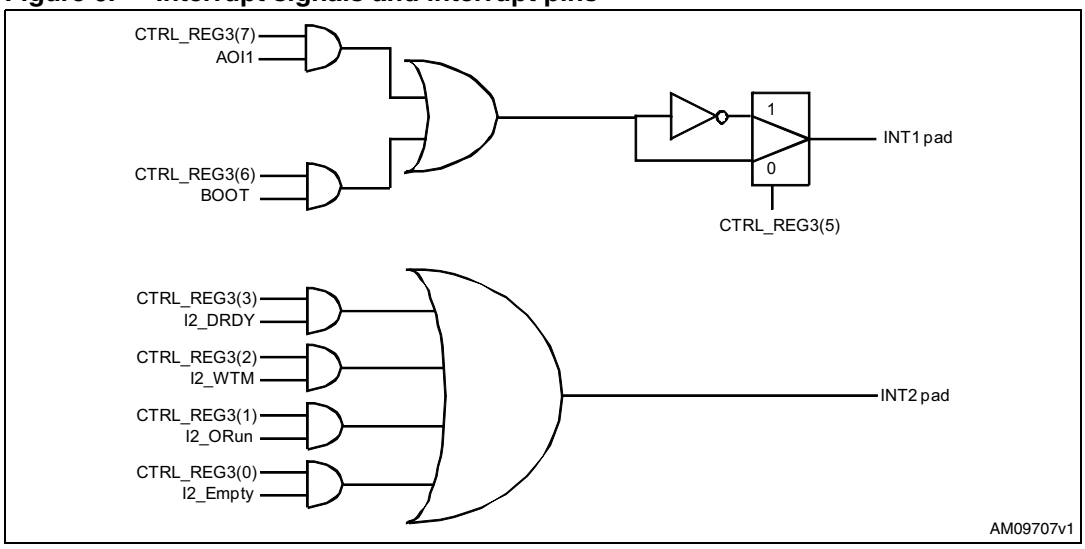
Table 15. CTRL_REG3 register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 16. CTRL_REG3 description

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: Disable; 1: Enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: Disable; 1: Enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: High; 1:Low)
PP_OD	Push-Pull / Open drain. Default value: 0. (0: Push-Pull; 1: Open drain)
I2_DRDY	Date Ready on DRDY/INT2. Default value 0. (0: Disable; 1: Enable)
I2_WTM	FIFO Watermark interrupt on DRDY/INT2. Default value: 0. (0: Disable; 1: Enable)
I2_ORun	FIFO Overrun interrupt on DRDY/INT2 Default value: 0. (0: Disable; 1: Enable)
I2_Empty	FIFO Empty interrupt on DRDY/INT2. Default value: 0. (0: Disable; 1: Enable)

Figure 6. Interrupt signals and interrupt pins



5.2 Interrupt configuration

The L3G4200D offers several possibilities to personalize the interrupt signal. The registers involved in the interrupt generation behavior are INT1_CFG, INT1_THS and INT1_DURATION.

Table 17. INT1_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 18. INT1_CFG description

AND/OR	AND/OR combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch Interrupt Request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)

Table 19. Interrupt mode configuration

AOI	Interrupt mode
0	OR combination of interrupt events
1	AND combination of interrupt events

Whenever an interrupt condition is verified the interrupt signal is generated and by reading the INT1_SRC register it is possible to understand which condition happened.

Reading INT1_SRC also clears INT1_SRC IA bit (and eventually the interrupt signal on INT1 pin) and allows the refreshment of data in the INT1_SRC register if the latched option was chosen.

5.3 Threshold

Threshold registers INT1_THS_xH and INT_THS_xL (respectively MSB and LSB) define the reference angular rates used by interrupt generation circuitry.

Table 20. INT1_THS_xH register

-	THSx14	THSx13	THSx12	THSx11	THSx10	THSx9	THSx8

Table 21. INT1_THS_xL register

THSx7	THSx6	THSx5	THSx4	THSx3	THSx2	THSx1	THSx0

The value of 1 LSB of the threshold depends on the selected full scale (*Table 22*).

Table 22. Threshold LSB value

Full scale	Threshold LSB value (mdps)
100	~3
200	~6.1
400	~12.2
800	~24.5

5.4 Duration

The content of the Dx bits of the duration register sets the minimum duration of the interrupt event to be recognized.

Table 23. INT1_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 24. INT1_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

Duration steps and maximum values depend on the ODR chosen.

Duration time is measured in N/ODR, where N is the content of the duration register and ODR is 100, 200, 400, 800.

Table 25. Duration LSB value in normal mode

ODR (Hz)	Duration LSB value (ms)
100	10
200	5
400	2.5
800	1.25

WAIT bit of INT1_DURATION register has the following meaning:

Wait =’0’: the interrupt falls immediately if signal crosses the selected threshold (*Figure 7*)

Wait =’1’: if signal crosses the selected threshold, the interrupt falls only after the duration has counted number of samples at the selected data rate, written into the duration counter register (*Figure 8*).

Figure 7. Wait disabled

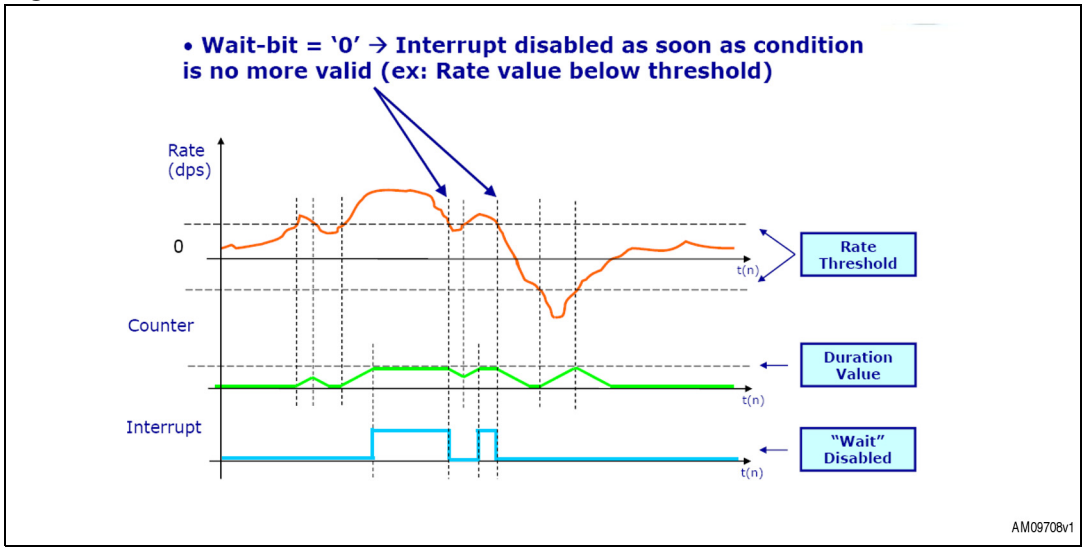
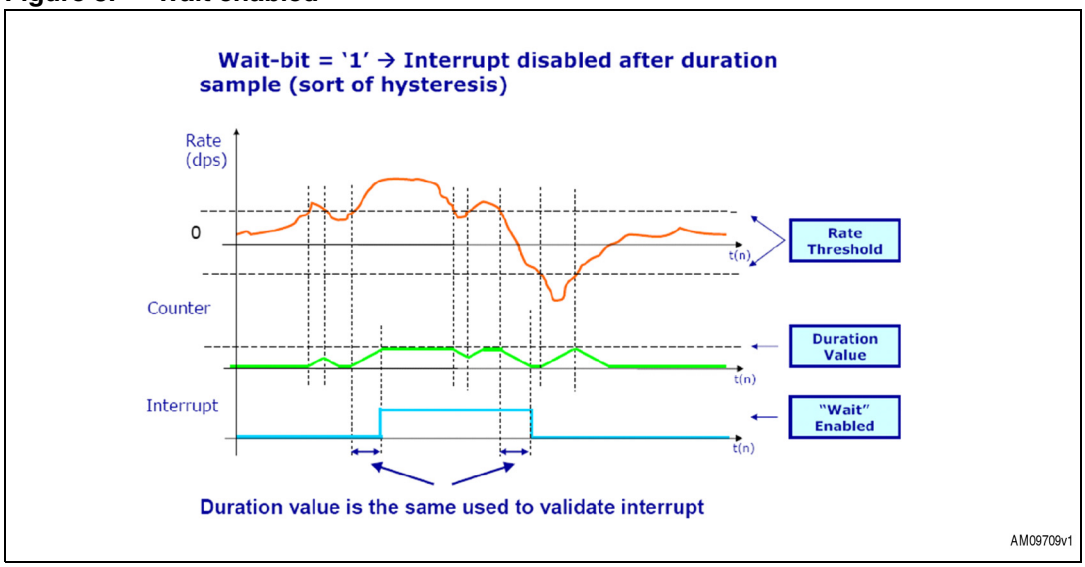


Figure 8. Wait enabled



5.5 Selective axis movement and wake-up interrupts

The L3G4200D interrupts signal can behave as selective axis movement detection and wake-up. Whenever an interrupt condition is verified, the interrupt signal is generated and by reading the INT1_SRC register it is possible to understand which condition happened.

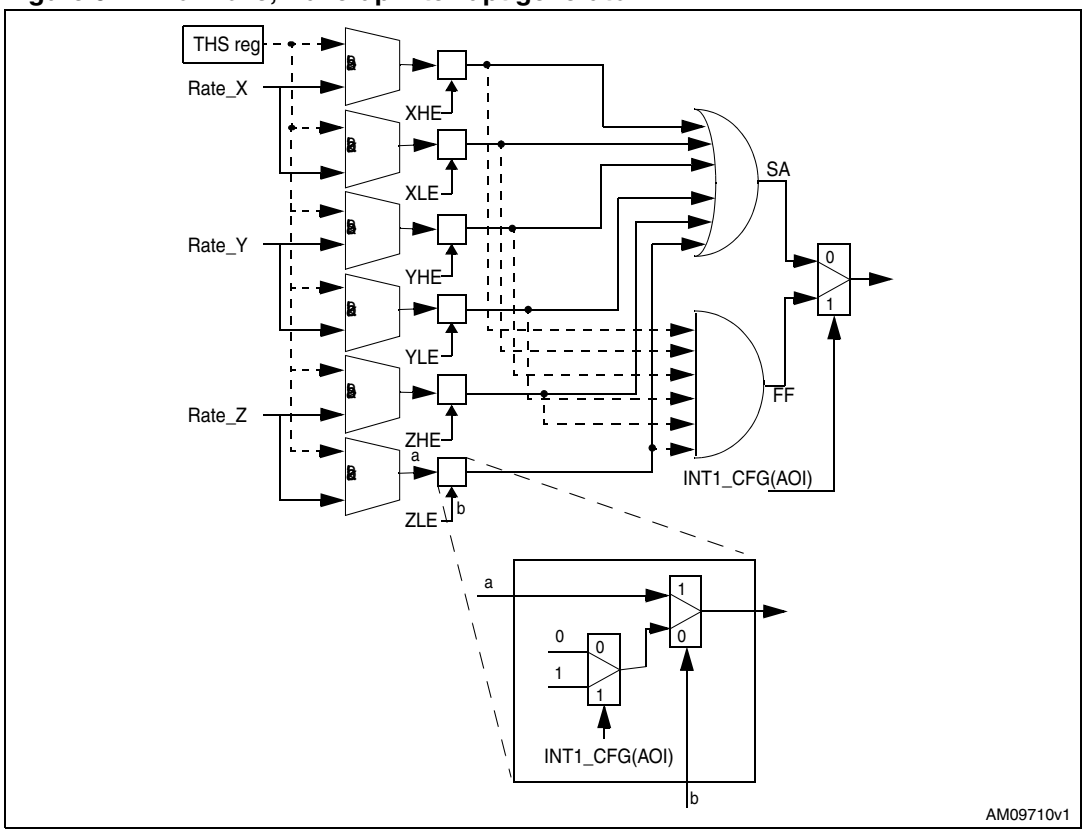
The selective axis movement detection signal (SA) and wake-up signal (WU) interrupt generation block is represented in *Figure 9*.

The SA or WU interrupt generation is selected through the AOI bit in the INT1_CFG register. If the AOI bit is '0', signals coming from comparators for the axis enabled through the INT1_CFG register are put in logical OR. In this case, interrupt is generated when at least one of the enabled axes exceeds the threshold written in module in INT1_THS_xH and INT1_THS_xL registers. Otherwise, if the AOI bit is '1', signals coming from comparators enter a "NAND" port. In this case an interrupt signal is generated only if all the enabled axes are passing the threshold.

LIR bit of INT1_CFG allows to decide if the interrupt request must be latched or not. If LIR bit is '0' (default value), the interrupt signal goes high when the interrupt condition is satisfied and returns to low immediately if the interrupt condition is no longer verified. Otherwise, if the LIR bit is '1', whenever an interrupt condition is applied the interrupt signal remains high even if the condition returns to a non-interrupt status until a reading to the INT1_SRC register is performed.

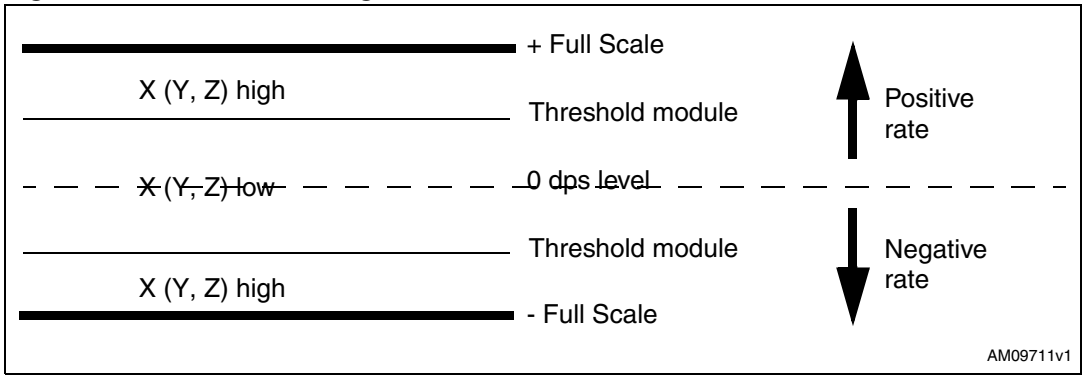
The ZHIE, ZLIE, YHIE, YLIE, XHIE, and HLIE bits of the INT1_CFG register allow to decide on which axis the interrupt decision must be performed and on which direction the threshold must be passed to generate the interrupt request.

Figure 9. No-move, wake-up interrupt generator



The threshold module which is used by the system to detect any no-move or wake-up event is defined by the INT1_THS register. The threshold value is expressed over 7 bits as an unsigned number and is symmetrical around the zero-g level. XH (YH, ZH) is true when the unsigned angular rate value of the X (Y, Z) channel is higher than INT1_THS. Similarly, XL (YL, ZL) low is true when the unsigned angular rate value of the X (Y, Z) channel is lower than INT1_THS. Refer to *Figure 10* for more details.

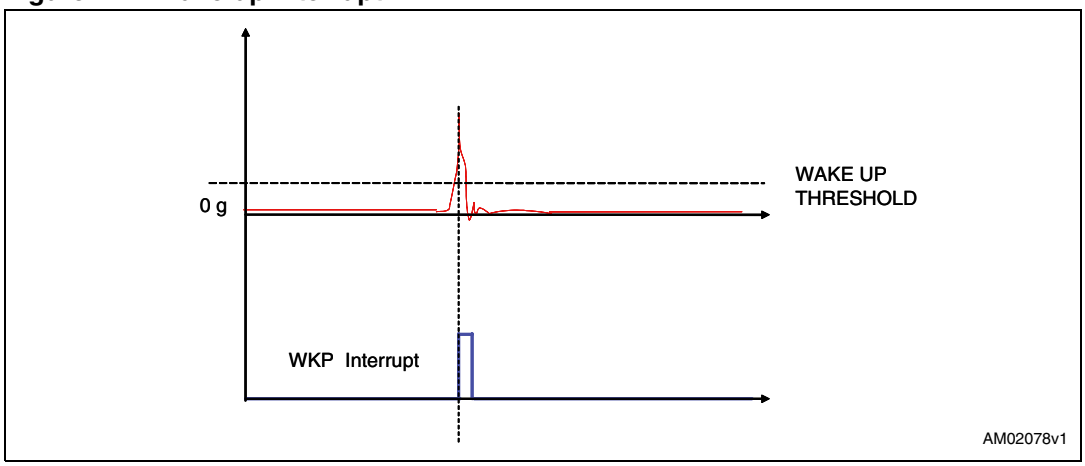
Figure 10. NM_WU_CFG high and low



5.5.1 Wake-up

Wake-up interrupt refers to a specific configuration of the INT1_CTRL register that allows interrupt generation when the angular rate on the configured axis exceeds a defined threshold (*Figure 11*).

Figure 11. Wake-up interrupt



5.5.2 HP filter bypassed

This paragraph provides a basic algorithm which shows the practical use of the wake-up feature. In particular, with the code below, the device is configured to recognize when the absolute angular rate along either the X axis exceeds a preset threshold (100 dps used in the example). The event which triggers the interrupt is latched inside the device and its occurrence is signalled through the use of the INT1 pin.

1	Write 0Fh into CTRL_REG1	// Turn-on the sensor and enable X, Y, and Z // ODR = 100 Hz
2	Write 00h into CTRL_REG2	// High-pass filter disabled
3	Write 80h into CTRL_REG3	// Interrupt driven to INT1 pad
4	Write 00h into CTRL_REG4	// FS = 250 *dps*
5	Write 2Ch into INT1_THS_XH	// Threshold = 100 dps
6	Write A4h into INT1_THS_XL	// Threshold = 100 dps
7	Write 00h into INT1_DURATION	// Duration = 0
8	Write 02h into INT1_CFG	// Enable XH interrupt generation
9	Poll INT1 pad; if INT1=0 then go to 8	// Poll INT1 pin waiting for the // wake-up event
10	Read INT1_SRC	// Return the event that has triggered the // interrupt
11	(Wake-up event has occurred; insert your code here)	// Event handling
12	Go to 8	

5.5.3 Using the HP filter

The code provided below gives a basic routine which shows the practical use of the wake-up feature performed on high-pass filtered data. In particular the device is configured to recognize when the high-frequency component of the angular rate applied along either the X, Y, or Z axis exceeds a preset threshold (100 dps used in the example).
The event which triggers the interrupt is latched inside the device and its occurrence is signalled through the use of the INT1 pin.

1	Write 0Fh into CTRL_REG1	// Turn-on the sensor and enable X, Y, and Z // ODR = 100 Hz
2	Write 00h into CTRL_REG2	// High-pass filter in normal mode
3	Write 80h into CTRL_REG3	// Interrupt driven to INT1 pad
4	Write 00h into CTRL_REG4	// FS = 250 *dps*

5	Write 05h into CTRL_REG5	// Data in DataReg and FIFO are high-pass filtered
		// High-pass-filtered data are used for interrupt
		// generation

6	Write 2Ch into INT1_THS_XH	// Threshold = 100 dps
7	Write A4h into INT1_THS_XL	// Threshold = 100 dps

8	Write 2Ch into INT1_THS_YH	// Threshold = 100 dps
9	Write A4h into INT1_THS_YL	// Threshold = 100 dps
10	Write 2Ch into INT1_THS_ZH	// Threshold = 100 dps
11	Write A4h into INT1_THS_ZL	// Threshold = 100 dps
12	Write 00h into INT1_DURATION	// Duration = 0

13	Read REFERENCE	// Dummy read to force the HP filter to
		// current angular rate value
		// (i.e. set reference angular rate)

14	Write 6Ah into INT1_CFG	// Enable XH, YH and ZH interrupt generation // Interrupt latched
15	Poll INT1 pad; if INT1=0 then go to 8	// Poll INT1 pin waiting for the // wake-up event
16	Read INT1_SRC	// Return the event that has triggered the // interrupt
17	(Wake-up event has occurred; insert your code here)	// Event handling
18	Go to 15	

At step 13, a dummy reading at the REFERENCE register is performed to set the current/reference angular rate/tilt state against which the device performed the threshold comparison.

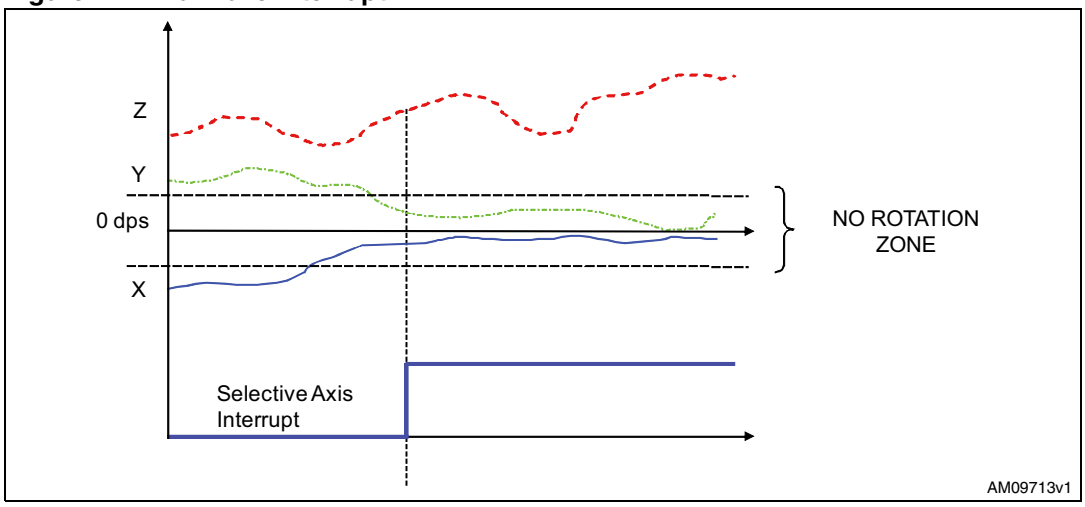
This reading may be performed any time it is required to set current rate as a reference state without waiting for the filter to settle.

5.6 Selective axis movement detection

Selective axis movement detection refers to a specific configuration of INT1_CTRL register that allows to recognize when the device is rotating only around the selected axes.

Referring to *Figure 12*, a “no rotation zone” is defined around the zero-dps level where the angular rates are small enough to be considered as zero. It is possible to create a configuration of INT1_CFG register so that an interrupt is generated only if, i.e., angular rate for rotation around x and y axes are around zero while it is different from zero for z axis. This means the device is doing a pure yaw rotation.

Figure 12. No-move interrupt



This paragraph provides the basics for the use of the selective axis movement detection feature. Here below is reported the example code which implements the SW routine for the selective axis movement recognition:

1	Write 0Fh into CTRL_REG1	// Turn-on the sensor and enable X, Y, and Z // ODR = 100 Hz
3	Write 80h into CTRL_REG3	// Interrupt driven to INT1 pad
4	Write 00h into CTRL_REG4	// FS = 250 *dps*
6	Write 2Ch into INT1_THS_XH	// Threshold = 60 dps
7	Write A4h into INT1_THS_XL	// Threshold = 60 dps
8	Write 2Ch into INT1_THS_YH	// Threshold = 60 dps
9	Write A4h into INT1_THS_YL	// Threshold = 60 dps
10	Write 2Ch into INT1_THS_ZH	// Threshold = 60 dps
11	Write A4h into INT1_THS_ZL	// Threshold = 60 dps
12	Write 01h into INT1_DURATION	// Duration = 10 ms
13	Write 65h into INT1_CFG	// Enable XL, YL and ZH interrupt generation in AND // configuration. Interrupt latched
14	Poll INT1 pad; if INT1=0 then go to 8	// Poll INT1 pin waiting for the // wake-up event
15	Read INT1_SRC	// Return the event that has triggered the // interrupt
16	(Wake-up event has occurred; insert your code here)	// Event handling
17	Go to 15	

The code sample exploits a threshold set at 60 dps selective axis movement detection and the event is notified by the hardware signal INT1. At step 7, the INT1_DURATION register is configured like this to ignore events that are shorter than 1/DR = 1/100 ~= 10 msec in order to avoid false detections. Once the selective axis movement detection has occurred, a reading of the INT1_SRC register clears the request and the device is ready to recognize other events.

6 First in first out (FIFO) buffer

In order to decrease the host processor interaction and facilitate post processing data for events recognition, L3G4200D embeds a first in first out buffer (FIFO) for each of the three output channels, X, Y, and Z.

FIFO use allows a consistent power saving for the system, it can wake-up only when needed and burst the significant data out from the FIFO.

The FIFO buffer can work according to four different modes that guarantee a high-level of flexibility during application development: Bypass mode, FIFO mode, Stream mode, and Stream-to-FIFO mode.

The programmable watermark level and FIFO overrun event can be enabled to generate dedicated interrupts on the DRDY/INT2 pin.

6.1 FIFO description

The FIFO buffer is able to store up to 32 angular rate samples of 16 bits for each channel; data are stored in the 16-bit 2's complement left justified representation.

The data samples set consists of 6 bytes (Xl, Xh, Yl, Yh, Zl, and Zh) and they are released to the FIFO at the selected output data rate (ODR).

The new sample set is placed in the first empty FIFO slot until the buffer is full, therefore, the oldest value is overwritten.

Table 26. FIFO buffer full representation (32nd sample set stored)

Output registers	**0x28h**	**0x29h**	**0x2Ah**	**0x2Bh**	**0x2Ch**	**0x2Dh**
	Xl(0)	Xh(0)	Yl(0)	Yh(0)	Zl(0)	Zh(0)
FIFO index	**FIFO sample set**					
FIFO(0)	Xl(0)	Xh(0)	Yl(0)	Yh(0)	Zl(0)	Zh(0)
FIFO(1)	Xl(1)	Xh(1)	Yl(1)	Yh(1)	Zl(1)	Zh(1)
FIFO(2)	Xl(2)	Xh(2)	Yl(2)	Yh(2)	Zl(2)	Zh(2)
FIFO(3)	Xl(3)	Xh(3)	Yl(3)	Yh(3)	Zl(3)	Zh(3)
...	...	...	...	...	...	...
...	...	...	...	...	...	...
FIFO(30)	Xl(30)	Xh(30)	Yl(30)	Yh(30)	Zl(30)	Zh(30)
FIFO(31)	Xl(31)	Xh(31)	Yl(31)	Yh(31)	Zl(31)	Zh(31)

Table 27. FIFO overrun representation (33rd sample set stored and 1st sample discarded)

Output registers	0x28h	0x29h	0x2Ah	0x2Bh	0x2Ch	0x2Dh
	XI(1)	XH(1)	YI(1)	YH(1)	ZI(1)	ZH(1)
FIFO index	Sample set					
FIFO(0)	XI(1)	XH(1)	YI(1)	YH(1)	ZI(1)	ZH(1)
FIFO(1)	XI(2)	XH(2)	YI(2)	YH(2)	ZI(2)	ZH(2)
FIFO(2)	XI(3)	XH(3)	YI(3)	YH(3)	ZI(3)	ZH(3)
FIFO(3)	XI(4)	XH(4)	YI(4)	YH(4)	ZI(4)	ZH(4)
...	...	...	...	...	...	...
...	...	...	...	...	...	...
FIFO(30)	XI(31)	XH(31)	YI(31)	YH(31)	ZI(31)	ZH(31)
FIFO(31)	XI(32)	XH(32)	YI(32)	YH(32)	ZI(32)	ZH(32)

Table 26 represents the FIFO full status when 32 samples are stored in the buffer while *Table 27* represents the next step when the 33rd sample is inserted into FIFO and the 1st sample is overwritten. The new oldest sample set is made available in the output registers.

When FIFO is enabled and mode is different from bypass, the L3G4200D output registers (28h to 2Dh) always contain the oldest FIFO sample set.

6.2 FIFO registers

The FIFO buffer is managed by three different accelerometer registers, two of these allow to enable and configure the FIFO behavior, the third provides information about the buffer status.

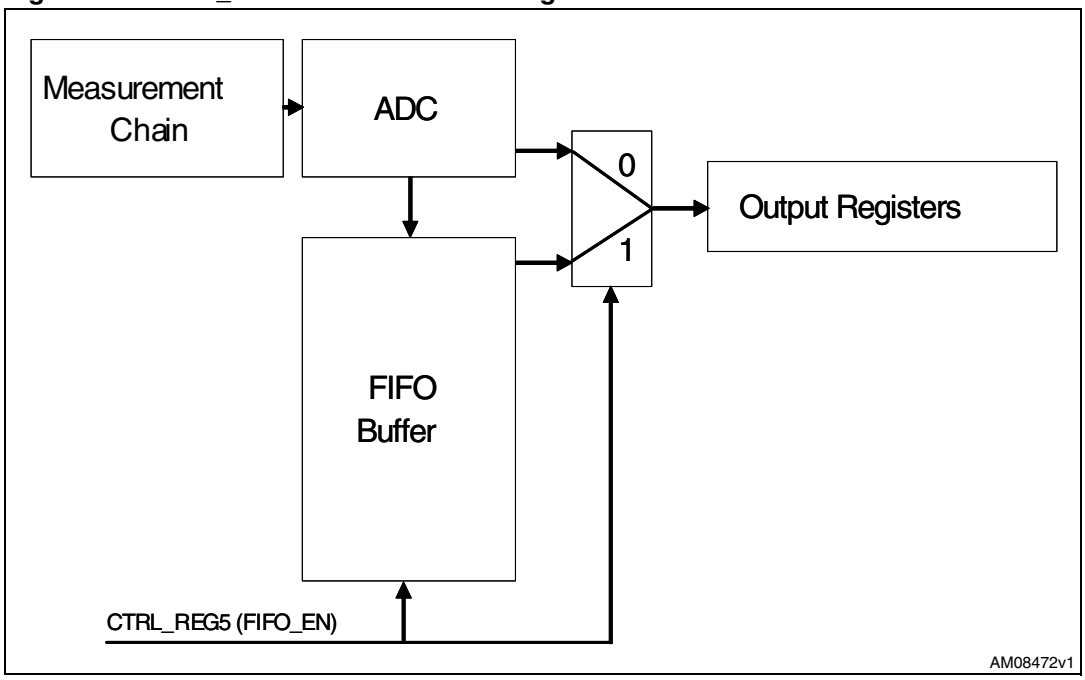
6.2.1 Control register 5 (0x24)

The FIFO_EN bit in CTRL_REG5 must be set to 1 in order to enable the internal first in first out buffer; while this bit is set, the gyroscope output registers (28h to 2Dh) don't contain the current angular rate value but they always contain the oldest value stored in FIFO.

Table 28. FIFO enable bit in CTRL_REG5

b7	b6	b5	b4	b3	b2	b1	b0
X	FIFO_EN	X	X	X	X	X	X

Figure 13. FIFO_EN connection block diagram



6.2.2 FIFO control register (0x2E)

This register is dedicated to FIFO mode selection and watermark configuration.

Table 29. FIFO_CTRL_REG

b7	b6	b5	b4	b3	b2	b1	b0
FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

FM[1:0] bits are dedicated to define the FIFO buffer behavior selection:

1. FM[2:0] = (0,0,0): Bypass mode
2. FM[2:0] = (0,0,1): FIFO mode
3. FM[2:0] = (0,1,0): Stream mode
4. FM[2:0] = (0,1,1): Stream to FIFO mode
5. FM[2:0] = (1,0,0): Bypass-to-FIFO mode

The trigger used to activate stream-to-FIFO and bypass-to-stream modes is related to the IA bit value of the selected INT1_SRC register and does not depend on the interrupt pin value and polarity. The trigger is generated also if the selected interrupt is not driven to an interrupt pin.

WTM[4:0] bits are intended to define the watermark level; when FIFO content exceeds this value the WTM bit is set to “1” in the FIFO source register.

6.2.3 FIFO source register (0x2F)

This register is updated at every ODR and provides information about the FIFO buffer status.

Table 30. FIFO_SRC_REG

b7	b6	b5	b4	b3	b2	b1	b0
WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

- WTM bit is set high when FIFO content exceeds watermark level.
- OVRN bit is set high when FIFO buffer is full, this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is reset when the first sample set has been read.
- EMPTY flag is set high when all FIFO samples have been read and FIFO is empty.
- FSS[4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time that one sample set is retrieved from FIFO.

Register content is updated synchronous to the FIFO write and read operation.

Table 31. FIFO_SRC_REG behavior assuming FTH[4:0] = 15

WTM	OVRN	EMPTY	FSS[4:1]	Unread FIFO samples	Timing
0	0	1	00000	0	t0
0	0	0	00001	1	t0 + 1/ODR
0	0	0	00010	2	t0 + 2/ODR
...	...	...	...	...	...
0	0	0	01111	15	t0 + 15/ODR
1	0	0	10000	16	t0 + 16/ODR
...	...	...	...	...	...
1	0	0	11110	30	t0 + 30/ODR
1	0	0	11111	31	t0 + 31/ODR
1	1	0	11111	32	t0 + 32/ODR

The watermark flag, the FIFO overrun and FIFO empty event can be enabled to generate a dedicated interrupt on the DRY/INT2 pin by configuring CTRL_REG3.

Table 32. CTRL_REG3 (0x22)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	I2_WTM	I2_ORun	I2_Empty

- I2_WTM bit drives watermark flag (WTM) on the DRY/INT2 pin.
- I2_OVRN bit drives overrun event (OVRN) on the DRY/INT2Y pin.
- I2_Empty bit drives empty event (EMPTY) on the DRY/INT2 pin

If one ore more bits are set to “1”, the DRY/INT2 pin status is the logical OR combination of the three signals.

6.3 FIFO modes

The L3G4200D FIFO buffer can be configured to operate in five different modes selectable by the FM[2:0] field in FIFO_CTRL_REG. Available configurations ensure a high-level of flexibility and extend the number of functions usable in application development.

Bypass, FIFO, Stream, Stream-to-FIFO and Bypass-to-stream modes are described in the following paragraphs.

6.3.1 Bypass mode

When bypass mode is enabled, FIFO is not operational: buffer content is cleared, output registers (0x28 to 0x2D) are frozen at the last value loaded, and the FIFO buffer remains empty until another mode is selected.

Follow these steps for bypass mode configuration:

1. Turn-on FIFO by setting the FIFO_En bit to “1” in control register 5 (0x24). After this operation the FIFO buffer is enabled but isn’t collecting data, output registers are frozen to the last samples set loaded.
2. Activate bypass mode by setting the FN[2:0] field to “000” in the FIFO control register (0x2E). If this mode is enabled, FIFO source register (0x2F) is forced equal to 0x20.

Bypass mode must be used in order to stop and reset the FIFO buffer when a different mode is operating. Note that placing the FIFO buffer into bypass mode clears the whole buffer content.

6.3.2 FIFO mode

In FIFO mode, the buffer continues filling until full (32 sample set stored,) then it stops collecting data and the FIFO content remains unchanged until a different mode is selected.

Follow these steps for FIFO mode configuration:

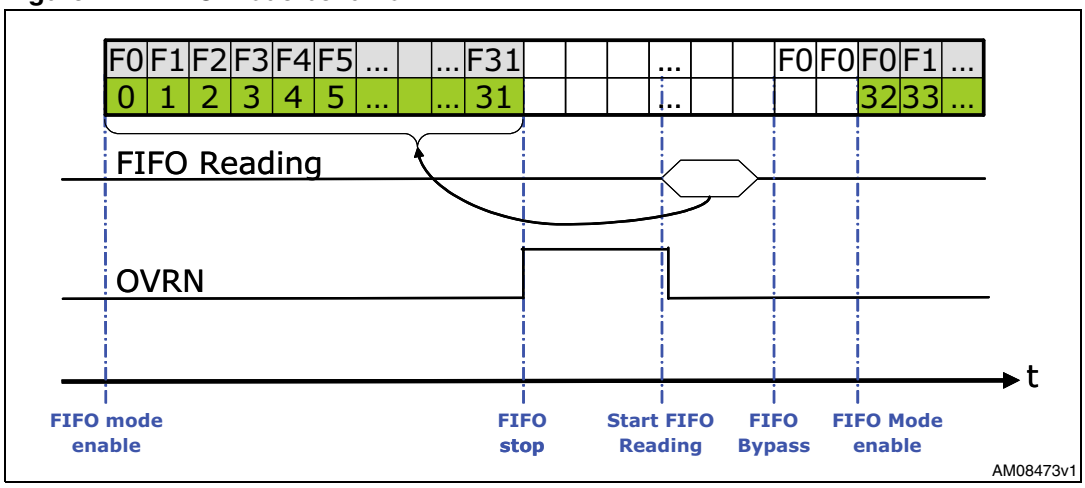
1. Turn-on FIFO by setting the FIFO_En bit to “1” in control register 5 (0x24). After this operation the FIFO buffer is enabled but isn’t collecting data, output registers are frozen to the last samples set loaded.
2. Activate FIFO mode by setting the FN[2:0] field to “001” in the FIFO control register (0x2E).

By selecting this mode, FIFO starts data collection and source register (0x2F) changes according to the number of samples stored. At the end of the procedure, the source register is set to 0xDF and the OVRN flag generates an interrupt if the I2_OVRN bit is selected in control register 5. Data can be retrieved when OVRN is set to”1”, performing a 32 sample set reading from the output registers, data can be retrieved also on the WTM flag instead of OVRN if the application requires a lower number of samples. Communication speed is not so important in FIFO mode because data collection is stopped and there is no risk of overwriting acquired data. Before restarting FIFO mode, at the end of the reading procedure it is necessary to transit from bypass mode.

A FIFO mode application hint is reported below:

1. Set FIFO_En = 1: Enable FIFO
2. Set FN[2:0] = (0,0,1): Enable FIFO mode
3. Wait OVRN or WTM interrupt
4. Read data from gyroscope output registers
5. Set FN[2:0] = (0,0,0): Enable bypass mode
6. Repeat from point 2

Figure 14. FIFO mode behavior



If FIFO mode is enabled, the buffer starts to collect data and fill all the 32 slots (from F0 to F31) at the selected output data rate. When the buffer is full, the OVRN bit goes up and data collection is permanently stopped; the user can decide to read FIFO content at any time because it is maintained unchanged until bypass mode is selected. The reading procedure is composed of a 32 sample set of 6 bytes for a total of 192 bytes and retrieves data starting from the oldest sample stored in FIFO (F0). The OVRN bit is reset when the first sample set has been read. The bypass mode setting resets FIFO and allows the user to enable FIFO mode again.

6.3.3 Stream mode

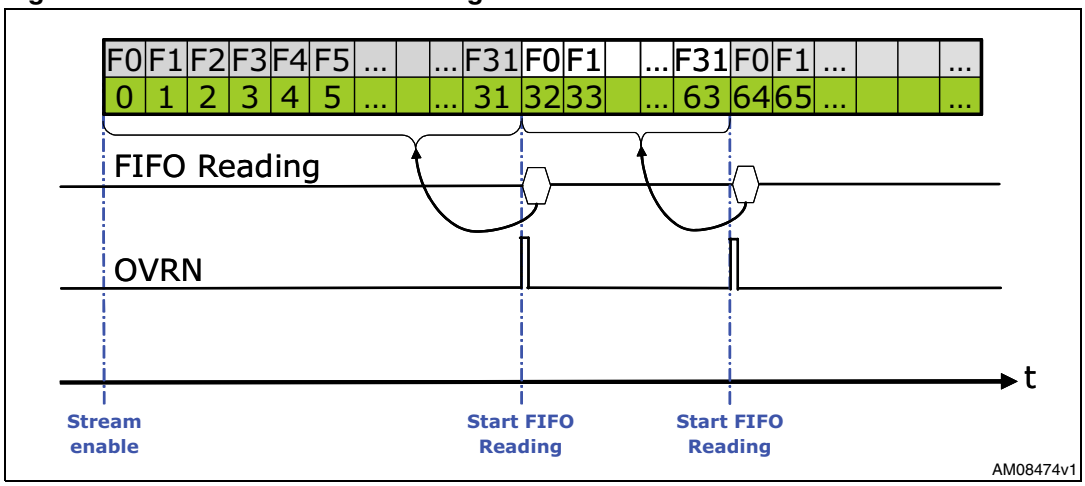
In stream mode FIFO continues filling, when the buffer is full, the FIFO index restarts from the beginning and older data is replaced by the current. The oldest values continue to be overwritten until a read operation makes free FIFO slots available. Host processor reading speed is most important in order to free slots faster than new data is made available. FM[2:0] bypass configuration is used to stop this mode.

Follow these steps for FIFO mode configuration:

1. Turn-on FIFO by setting the FIFO_En bit to “1” in control register 5 (0x24). After this operation the FIFO buffer is enabled but isn’t collecting data, output registers are frozen to the last samples set loaded.
2. Activate stream mode by setting the FN[2:0] field to “011” in the FIFO control register (0x2E).

As described, for FIFO mode, data can be retrieved when OVRN is set to"1" performing a 32 sample set reading from output registers, data can be retrieved also on the WTM flag if the application requires a smaller number of samples.

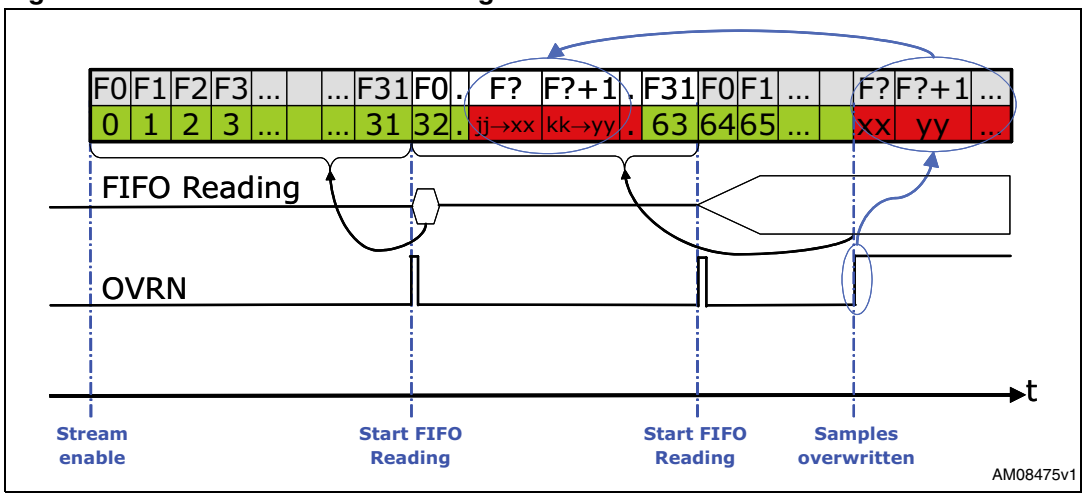
Figure 15. Stream mode fast reading behavior



In stream mode, the FIFO buffer is continuously filling (from F0 to F31) at the selected output data rate. When the buffer is full the OVRN flag goes up and the suggested solution is to read all FIFO samples (192 bytes) faster then 1*ODR, in order to make free FIFO slots available for the new angular rate samples. This allows to avoid loss of data and to decrease the host processor interaction increasing system efficiency. If the reading procedure is not fast enough, three different cases can be observed:

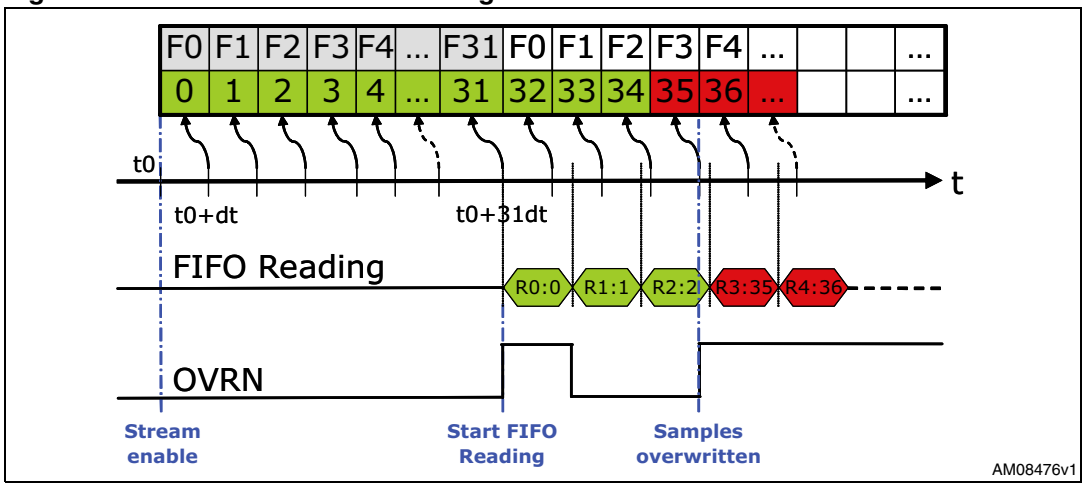
1. FIFO sample set (6 bytes) reading faster than 1*ODR: data are correctly retrieved because a free slot is made available before new data is generated.
2. FIFO sample set (6 bytes) reading synchronous to 1*ODR: data are correctly retrieved because a free slot is made available before new data is generated but FIFO benefits are not exploited. This case is equivalent to read data on data ready interrupt and does not reduce the host processor interaction compared to the standard accelerometer reading.
3. FIFO sample set (6 bytes) reading slower than 1*ODR: in this case some data is lost because data recovery is not fast enough to free slots for new angular rate data *Figure 16*. The number of correctly recovered samples is related to the difference between the current ODR and the FIFO sample set reading rate.

Figure 16. Stream mode slow reading behavior



In *Figure 16*, due to slow reading, data from “jj” are not retrieved because they are replaced by the new gyroscope samples generated by the system.

Figure 17. Stream mode slow reading zoom



After stream mode enable, FIFO slots are filled at the end of each ODR time frame. The reading procedure must start as soon as the OVRN flag is set to “1”, data are retrieved from FIFO at the beginning of the reading operation. When a read command is sent to the device, the output registers content is moved to the SPI/I^{2}C register and the current oldest FIFO value is shifted into the output registers in order to allow the next read operation. In the case of a reading slower than 1*ODR, some data can be retrieved from FIFO after that new sample is inserted into the addressed location. In *Figure 17* the fourth read command starts after the refresh of the F3 index and this generates a disconnect in the reading data. The OVRN flag advises the user that this event has taken place. In this example, three correct samples have been read, the number of correctly recovered samples is dependent on the difference between the current ODR and the FIFO sample set reading timeframe.

6.3.4 Stream-to-FIFO mode

This mode is a combination of the stream and FIFO modes described above. In stream-to-FIFO mode, the FIFO buffer starts operating in stream mode and switches to FIFO mode when the selected interrupt occurs.

Follow these steps for stream-to-FIFO mode configuration:

1. Configure desired interrupt generator using register INT1_CFG (0x30).
2. Turn-on FIFO by setting the FIFO_En bit to “1” in control register 5 (0x24). After this operation the FIFO buffer is enabled but isn’t collecting data, output registers are frozen to the last samples set loaded.
3. Activate stream-to-FIFO mode by setting the FN[2:0] field to “011” in the FIFO control register (0x2E).

The interrupt trigger is related to the IA bit in the INT1_SRC register and it is generated even if the interrupt signal is not driven to an interrupt pad. Mode switch is performed if both IA and OVRN bits are set high. Stream-to-FIFO mode is sensitive to the trigger level and not to the trigger edge, this means that if stream-to-FIFO is in FIFO mode and the interrupt condition disappears, the FIFO buffer returns to stream mode because the IA bit becomes zero. It is suggested to latch the interrupt signal used as the FIFO trigger in order to avoid losing interrupt events. If the selected interrupt is latched, it is needed to read the register INT1_SRC to clear the IA bit; after reading, the IA bit takes 2*ODR to go low.

In stream mode the FIFO buffer continues filling, when the buffer is full, the OVRN bit is set high and the next samples overwrite the oldest. When trigger occurs, two different cases can be observed:

1. If the FIFO buffer is already full (OVRN = “1”), it stops collecting data at the first sample after trigger. FIFO content is composed of #30 samples collected before the trigger event, the sample that has generated the interrupt event and one sample after trigger.
2. If FIFO isn’t yet full (initial transient), it continues filling until it is full (OVRN = “1”) and then, if trigger is still present, it stops collecting data.

Figure 18. Stream-to-FIFO mode: interrupt not latched

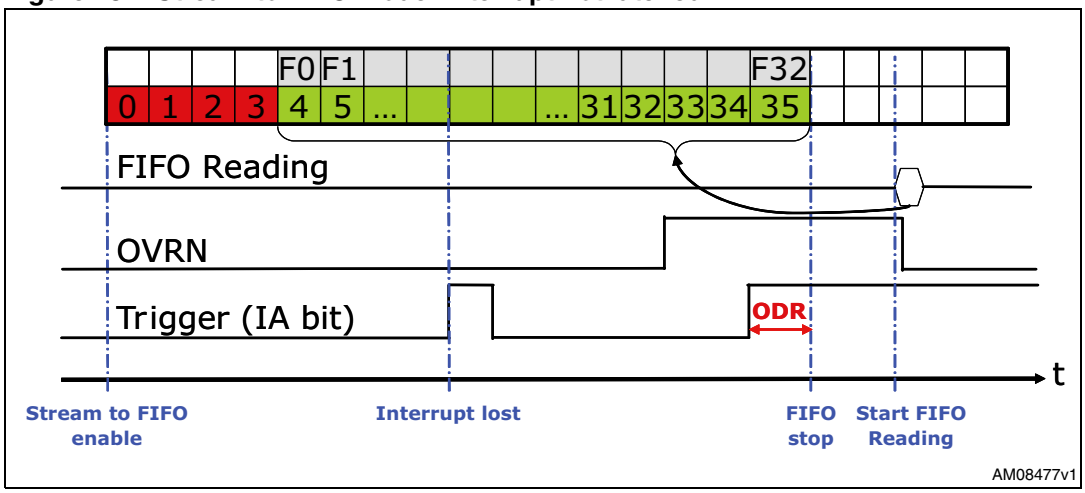
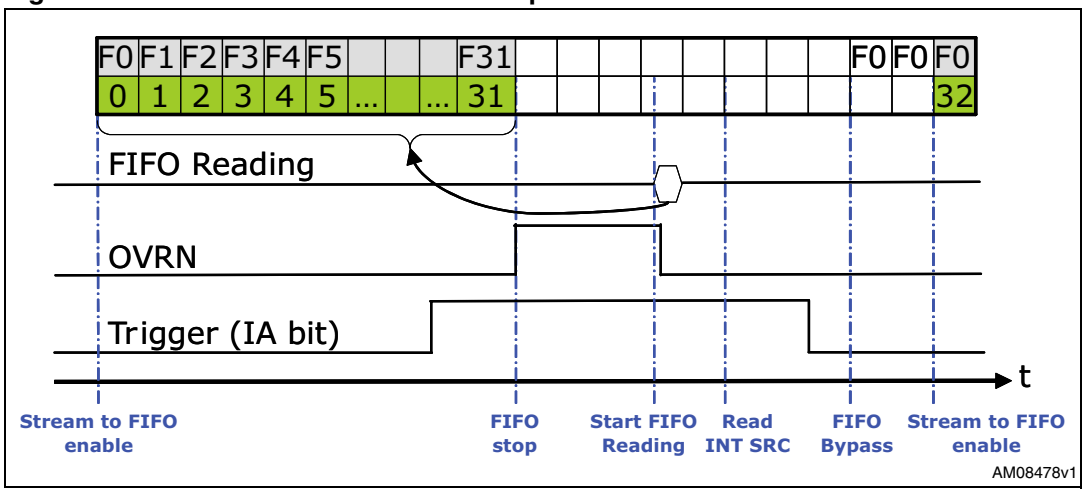


Figure 19. Stream-to-FIFO mode: interrupt latched



Stream-to-FIFO can be used in order to analyze the samples history that generate an interrupt; the standard operation is to read FIFO content when FIFO mode is triggered and FIFO buffer is full and stopped.

6.3.5 Bypass-to-stream mode

This mode is a combination of the bypass and stream modes described above. In bypass-to-stream mode, the FIFO buffer starts operating in bypass mode and switches to stream mode when the selected interrupt occurs.

Follow these steps for bypass-to-stream mode configuration:

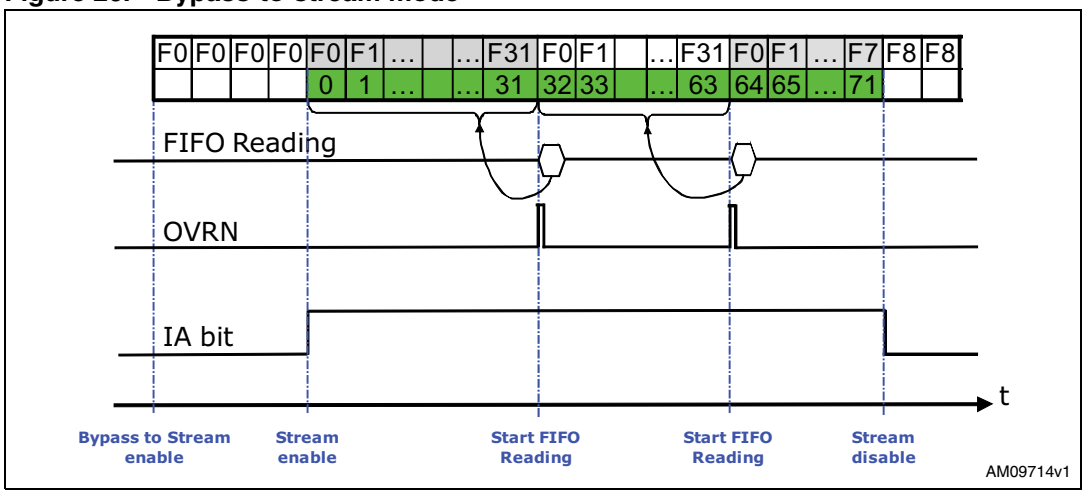
1. Configure desired interrupt generator using register INT1_CFG (0x30).
2. Turn-on FIFO by setting the FIFO_En bit to “1” in control register 5 (0x24). After this operation the FIFO buffer is enabled but isn’t collecting data, output registers are frozen to the last samples set loaded.
3. Activate bypass-to-stream mode by setting the FN[2:0] field to “100” in the FIFO control register (0x2E).

The interrupt trigger is related to the IA bit in the INT1_SRC register and it is generated even if the interrupt signal is not driven to an interrupt pad. Bypass-to-stream mode is sensitive to the trigger level and not to the trigger edge, this means that if bypass-to-stream is in stream mode and the interrupt condition disappears, the FIFO buffer returns to bypass mode because the IA bit becomes zero.

It is suggested to latch the interrupt signal used as the stream trigger in order to avoid losing interrupt events. If the selected interrupt is latched, it is needed to read the register INT1_SRC to clear the IA bit; after reading, the IA bit takes 2*ODR to go low.

In stream mode the FIFO buffer continues filling. When the buffer is full, the OVRN bit is set high and the next samples overwrite the oldest.

Figure 20. Bypass-to-stream mode

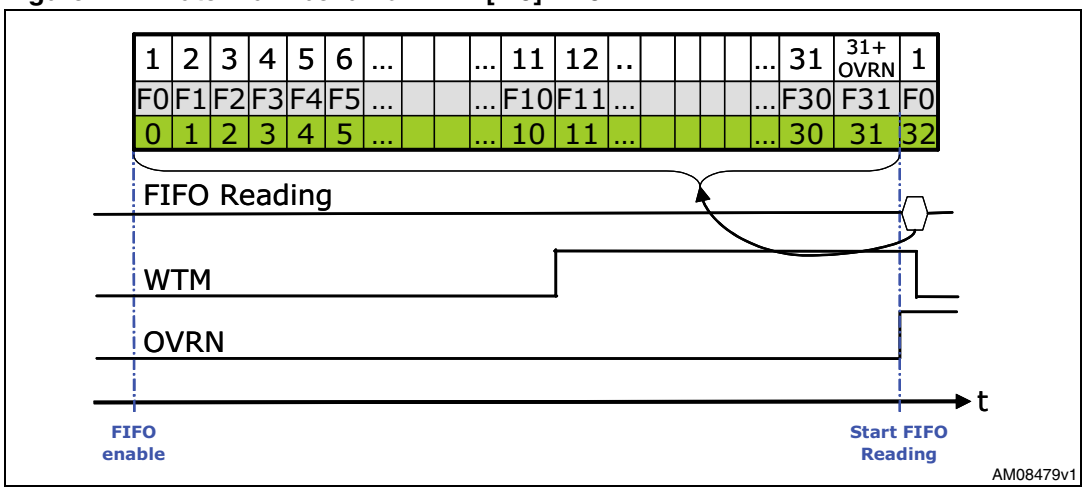


Bypass-to-stream can be used in order to start the acquisition when the configured interrupt is generated.

6.4 Watermark

Watermark is a configurable flag that can be used to generate specific interrupt in order to know when the FIFO buffer contains at least the number of samples defined as the watermark level. The user can select the desired level in a range from 0 to 31 using the WTM[4:0] field in the FIFO control register while the FIFO source register FSS[4:0] always contains the number of samples stored in FIFO. If FSS[4:0] is greater than WTM[4:0], the WTM bit is set high in the FIFO source register, on the contrary, WTM is driven low when the FSS[4:0] field becomes lower than WTM[4:0]. FSS[4:0] increases by one step at the ODR frequency and decreases by one step every time that a sample set reading is performed by the user.

Figure 21. Watermark behavior - FTH[4:0] = 10



In *Figure 21*, the first row indicates the FSS[4:0] value, the second row indicates the relative FIFO slot and last row shows the incremental FIFO data. Assuming WTM[4:0] = 10, the WTM flag changes from “0” to “1” when the eleventh FIFO slot is filled (F10). *Figure 22* shows that the WTM flag goes down when the FIFO content is less than WTM[4:0], it means that nine unread sample sets remain in FIFO.

The watermark flag (WTM) can be enabled to generate a dedicated interrupt on the DRY/INT2 pin by setting the I2_WTM bit high in CTRL_REG3.

6.5 Retrieve data from FIFO

When FIFO is enabled and the mode is different to bypass, reading output registers (28h to 2Dh) return the oldest FIFO sample set.

Whenever output registers are read, their content is moved to the SPI/I^2C output buffer. FIFO slots are ideally shifted up one level in order to release room for a new sample reception and output registers load the current oldest value stored in the FIFO buffer.

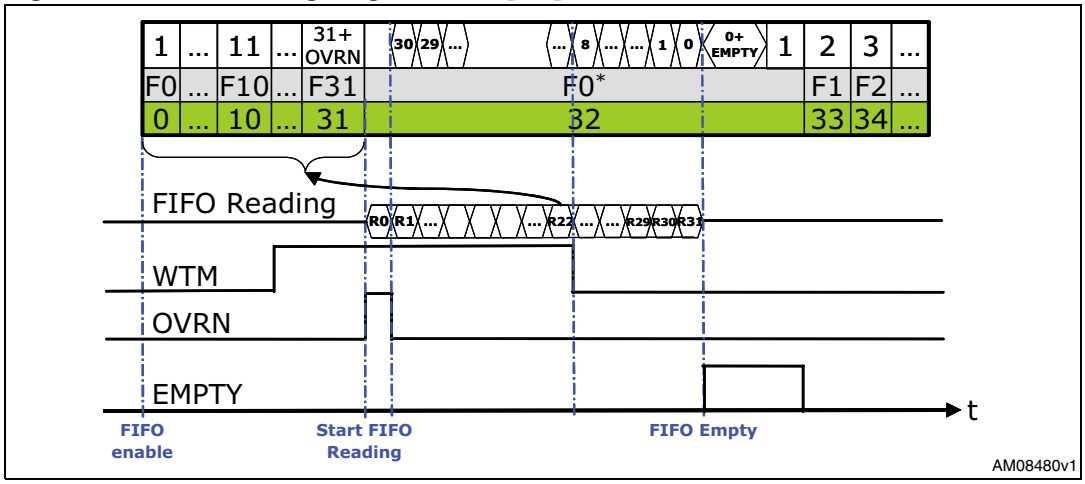
The whole FIFO content is retrieved performing thirty two read operations from gyroscope output registers, every other reading operation returns the same last value until a new sample set is available in the FIFO buffer.

Data can be retrieved from FIFO using every reading byte combination in order to increase the application flexibility (ex: 196 single byte reading, 32 reading of 6 bytes, 1 multiple reading of 196 bytes, etc.).

It is suggested to read all FIFO slots in a multiple byte reading of 196 bytes (6 output registers by 32 slots) faster than 1*ODR. In order to minimize communication between master and slave the reading address is automatically updated by the device; it rolls back to 0x28 when register 0x2D is reached.

In order to avoid losing data, the right ODR must be selected according to the serial communication rate available. In the case of standard I^2C mode being used (max rate 100 kHz), a single sample set reading takes 830 µs while total FIFO download is about 17.57ms. I^2C speed is lower than SPI and it needs about 29 clock pulses to start communication (start, slave address, device address+write, restart, device address+read) plus an additional 9 clock pulses for every byte to read. If this suggestion were followed, the complete FIFO reading would be performed faster than 1*ODR, this means that using a standard I^2C, the selectable ODR must be lower than 57 Hz. If a fast I^2C mode is used (max rate 400 kHz), the selectable ODR must be lower than 228 Hz.

Figure 22. FIFO reading diagram - FTH[4:0] = 10



In *Figure 22* "Rx" indicates a 6-byte reading operation and "F0*" represents a single ODR slot stretched for diagram convenience.

7 Temperature sensor

The L3G4200D is provided with an internal temperature sensor that is suitable for delta temperature measurement. Temperature data are generated with a frequency of 1 Hz and are stored inside the OUT_TEMP register in two's complement format, with a sensitivity if -1 LSB/°C.

8 Revision history

Table 33. Document revision history

Date	Revision	Changes
29-Apr-2011	1	Initial release.