SmallSEOTools

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3D Stacking Abhinav, MSc 2nd Year We all want performance from our devices and microprocessor companies are investing billions of dollars in R&D are coming up with really innovating and revolutionary technologies that are going to make moore's law to get to its saturation point. As more and more devices are going hand held that companies have to decide whether to have a headphone jack or a slightly bigger battery internal components of our devices has to be miniaturized. To tackle this problem major microprocessor giants are coming up with new form of circuit fabrication packaging which do not require to have discrete removable auxiliary components such as RAM like what we have today, for example 2019 both AMD and Intel unveiled chipsets from this paradigm, AMD called it their chiplet design and intel named it FOVEROS, which had the codename lakefield for this. These kinds of CPU ‘s are more likely to come in HPC(high performance computing) and server parts then in mainstream consumer market. FOVEROS was designed to be a low power performance centric chipset. Last year Microsoft confirmed to come equipped with this chipset in its revolutionary 2 screen folding Surface Duo. To be honest, I think it was more of a marketing move lower the market share that Qualcomm has with their ARM based chips like 8c X which were designed for these kind of devices Intel’s implementation had one flaw instead of having direct interaction between the processor and memory stacked like floors of building memory addresses and content had to be passed by lift like pillars in the 3D packaging with one logic box layer storing content from memory in a manner similar to buffer cache in UNIX systems but it hardly differs it from Intel’s previously announced 2.5D technology which had video memory instead of main memory. But nevertheless they made techies excited and motivated others in the same industry to come up with their own implementation which at the end of the day going to make our devices faster or I should rather say space efficient. For now what we should be excited for is have a day and have a eco-system where we can have a set processor from different vendors that we could stack on to one another to have better performance from those processors instead of getting bottlenecked by caches provided by processor which is fixed for its lifecycle. Which could seem to be a bit unbeneficial because they might lose their monopoly but this was the main selling point for ARM processors because manufacturers had flexibility and that is why you can never spot a homo sapien homoholding a phone that has Intel CPU, it might have Intel’s modem (iPhones for instance) and that is why they played a great gamble on foldable devices because they might be the next gen that people might switch to after phones. In conclusion SOC needs to have different subsystems for encryption, modems and so on, a space efficient technique is required otherwise cost would blow the roof. 3D stacking could minimize the cost and help Intel gain a much needed market share in portable devices which in a way going to help us getting a better product!

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