Kunendran Kajavathanan

github.com/Kajavathanan linkedin.com/in/kajavathanan kajavathanankunendran@gmail.com

Education

University of the West of England May. 2023 – Present
B.Eng(Hons) in Electrical and Electronic Engineering

Institute of Technology, University of Moratuwa Mar 2020 -Mar 2024
Diploma in Electronic and Telecommunication Engineering *Current GPA: 3.39/4.0*

Certifications

SystemVerilog for ASIC/FPGA Design and Simulation : Skill Surf
Machine Learning Engineer- Stage 1 : SLIIT
Microcontroller based Embedded System Design : University of Moratuwa

Skills

Expertise: Design Verification(UVM), RTL Design
Programming Languages: C++, SystemVerilog, Tcl
Protocols: AXI, UART, PCIE, APB, AHB
Tools and Framework: Siemens Questa, Vivado, Vitis, Git/GitHub
Languages: Tamil-native, English-Excellent

Projects

Single-Cycle RISC-V Processor Design | *SystemVerilog, Questa, Git, VS Code* Jul. 2024
- Implemented Risc-V instructionset Architecture, Including logical and Memory location instruction.
- Developed control logic to manage instruction execution within a single clock cycle.
- Developed a comprehensive Testbench in System Verilog to simulate and Verify the Design.

FPGA-Based Block RAM Design and Implementation Project | *Vivado, Vitis, Questa* May. 2024
- FPGA-based project focused on the design, implementation, and verification of Block RAM using Xilinx tools.
- Used Zybo-Z7 board to implement the design and Used Gtk term to read Data from Ports.
- Implemented UART communication to interact with the FPGA, enabling real-time data reading and writing via a serial terminal.

UVM Verification of SBE Decoder with AXI4-Stream Agent | *System Verilog, Questa Git, VS Code* Feb. 2024
- Created a UVM-compliant AXIS agent with AXIS interface capabilities.
- Conducted thorough UVM verification of the SBE decoder module, ensuring robust performance and reliability.

UVM Verification of Single-Port and Dual-Port RAM | *SystemVerilog, Questa, Git, VS Code* Nov. 2023
- UVM verification of single-port and dual-port RAM modules, addressing write collision issues.
- Utilized OOP to enhance the UVM testbench for robust and efficient verification.
- This project demonstrated strong expertise in advanced verification techniques and contributed to reliable memory design solutions.

Work Experience

Accelr | *Associate Electronic Engineer* March. 2024 – Sep 2024

- Hands-on experience in UVM verification, designed RTL for basic architectures, and expanded my knowledge of the RISC-V architecture.
- Worked with Hardware Accelerator Team to Verifiy the Designed SBE Decoder.This included creating test cases and running simulations to ensure the decoder functioned correctly and met performance requirements.
- Conducted research and development on PCIe protocol delivering presentations to fellow engineers to enhance their understanding of high-speed communication standards.

Accelr | *Electronic Intern* Sep. 2023 – March. 2024

- Hands-on experience in UVM verification, designed RTL for basic architectures, and expanded my knowledge of the RISC-V architecture.
- Worked with RTL Design Engineers to Design a UDP Parser and Designed multiple versions to find effficient way to produce results.

Airport and Aviation, Srilanka | *Electronic Intern* March. 2023 – Sep. 2023

- Assisting in the design and testing of electronic systems related to air safety and aviation electronics. Involved in designing voice communication system for Ratmalana Airport
- Designed Redundant voice communication system with the engineering team.Which composed of Amplifiers and push to talk features works in specific frequencies.
- Optimize the Design of Arduino based GPS Clock used in Jaffna International Airpot which helped overcome the heating issues in voltage Regulators and provided support to automating Recordings of Air traffic controllers with python scripts.