

Integrated photonic deep neural network with end-to-end on-chip backpropagation training

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Abstract

Integrated photonic neural networks (PNNs) have demonstrated significant potential to complement the digital electronic counterparts [1–3]. Nevertheless, robust and repeatable performance of scalable integrated PNNs is directly tied to the quality of their training. Error backpropagation (BP), which relies on nonlinear activation gradient computation, is the mainstream algorithm to train digital neural networks due to its scalability, versatility, and implementation efficiency [4]. Consequently, its adoption is highly desirable for the training of scalable PNNs. Despite such benefits and due to the lack of scalable on-chip activation gradient [5], PNNs have mostly been trained using a digital computer to run BP, which is inadequate in addressing device variations, or through gradient-free algorithms that do not fully benefit from the versatility of BP training. Here, we report the demonstration of an integrated photonic deep neural network with end-to-end on-chip gradient-descent BP training. All linear and nonlinear computations are performed on a single photonic chip, leading to scalable and robust training despite the considerable—but typical—fabrication-induced device variations. Two nonlinear data classification tasks are demonstrated in which the chip performance matches that of the ideal digital model, both in accuracy and robustness. Integrating the advantages of BP training with PNNs allows for generalization to various PNN architectures, paving the way for scalable and reliable next-generation photonic computing systems.

1 Introduction

Artificial intelligence and machine learning have transformed many areas of science and technology, and this transformation is only accelerating [6–8]. Artificial neural networks (ANNs) that try to mimic the human brain model, are a class of machine learning models that can learn to automatically perform specific tasks [9] in a variety of applications such as pattern recognition [10–12] as well as natural language processing and language models [13–16], through training and inference. ANNs, in the form of multi-layer perceptrons, typically consist of multiple layers of interconnected neurons, where each neuron generates an output based on the linear weighted-sum of its inputs followed by a nonlinear activation function. Although digital electronic processors will remain the primary platform for implementing ANNs, they face energy and throughput challenges due to electrical signal transmission loss and parasitic elements as well as limited clock speed. Leveraging alternative processing modalities could support the continued growth of ANNs by addressing such challenges. Low-loss signal transmission, parallel processing via wavelength, mode, and space multiplexing, and computation by propagation make optical signal processing a promising candidate [1–3]. Recently, several PNNs have been reported that are on par with or surpass the performance of digital ANNs [17–22]. While a general large-scale photonic processor that can compete with the advanced digital processors such as GPUs and TPUs seems to be a distant goal, some applications can specifically benefit from PNNs. For instance, in applications where the signal of interest is in the optical domain, energy efficiency and latency of the system can be improved with PNNs that eliminate the need for front-end high-speed opto-electronic and analog-digital conversions. Object recognition in images and videos [17–19, 23–25], nonlinearity compensation in optical fiber links [26], Fourier neural network [27], signal recovery [28], and inter-channel distortion compensation in wavelength-division multiplexing optical communication systems [29] are among such applications.

As with digital ANNs, PNNs must first be trained to find the optimal weights (*i.e.*, operating points of photonic devices) for inference, where the accuracy of inference is directly tied to the accuracy of training. PNN training can be viewed from two main aspects: the optimization algorithm and the

actual implementation method, where the choice of the former affects the latter. Gradient descent error BP training is widely used in digital ANNs. In this method, that starts from the output layer and propagates backward, the gradient of the loss function with respect to the weights of each layer is calculated and used to tune the weights and minimize the loss function through several iterations (epochs). As BP training offers efficient weight update and scalability to deep neural networks, its photonic implementation is highly desired. However, it involves the computation of the gradient of the nonlinear activation function [30]. This requires on-chip realization of both nonlinear activation and its gradient that is particularly challenging [5]. Hence, most PNNs either rely on offline BP training on a digital computer [17,26,31,32], or use alternative gradient-free training algorithms such as finite difference method [33], direct feedback alignment [34], associative learning [35], and forward training [20,36]. Recently, a hybrid photonic BP training has been demonstrated, where the photonic chip includes the linear weights of one neural layer [37]. Therefore, realizing a deep neural network requires re-using the same chip and employing a digital computer for nonlinear activation function and its gradient that limit scalability. In another recent work [38], BP training is demonstrated using free-space optics where the nonlinear activation is implemented via atomic transitions in a vapor cell. Despite impressive results, physical size and energy consumption of such bench-top setups as well as the need for special materials limit their large-scale deployment compared to integrated solutions. Two key aspects highlight the challenges of the previous integrated systems. On one hand, digital gradient-based BP training, although scalable, uses an ideal network model that does not typically include accurate photonic device models which results in sub-optimal training. Even if the device models are incorporated into the digital model, it is very hard to take the effect of process and environment variations into account. On the other hand, alternative gradient-free algorithms do not offer the versatility of gradient-based BP training.

Here we report the demonstration of the first integrated photonic deep neural network, to our knowledge, that performs the full end-to-end on-chip gradient descent BP training. Fabricated in a standard silicon photonic foundry, the chip includes forward and backward paths with multiple layers of photonic neurons with optical linear weights and opto-electronic nonlinear activations. The forward path consists of an input layer to modulate light with the input data, a hidden layer, and an output layer. The output of the forward path is fed back to the backward path to calculate the gradient of the loss function and tune the weights of the forward path using nominally identical on-chip devices. As proof of concept, we experimentally solve two nonlinear data classification problems with inference accuracy on par with that of the equivalent ideal digital models. Moreover, our on-chip training method compensates for fabrication-induced variations, and we show its robustness and superiority over digital BP training of PNN in presence and with no prior knowledge of the device-to-device variations. PNNs can significantly boost the performance of digital ANNs for select applications; however, high-quality training is crucial to their effectiveness. This work enables robust, repeatable, and scalable on-chip BP training PNN for the next generation of hybrid deep learning systems.

2 Neural network training using error backpropagation

Figure 1 conceptually shows the BP training process. The forward path of the neural network consists of N layers, where the output of the l^{th} layer ($a^{(l)}$) can be written as

$$a^{(l)} = \sigma^{(l)}(z^{(l)}) = \sigma^{(l)}(w^{(l)}a^{(l-1)}). \quad (1)$$

Here, $w^{(l)}$ is the weight matrix, $z^{(l)}$ is the weighted-sum output, and $\sigma^{(l)}$ is the nonlinear activation function of the l^{th} layer. The training process starts with calculating the cost function $C(\hat{y}, a^{(N)})$, which measures the output error between the expected output \hat{y} and actual output $a^{(N)}$. The main goal of gradient-descent BP training is to find the derivative of the cost function with respect to the weights of the network ($\partial C / \partial w^{(l)}$), and adjust the weights accordingly so that it minimizes the cost function. For that we define the error of the l^{th} layer as [39]

$$\delta^{(l)} = \frac{\partial C}{\partial z^{(l)}}. \quad (2)$$

In BP training, we start from calculating the error of the last layer

$$\delta^{(N)} = \frac{\partial C}{\partial z^{(N)}} = \frac{\partial C}{\partial a^{(N)}} \sigma'^{(N)}(z^{(N)}). \quad (3)$$

Then, by backpropagating the error of the last layer towards the first layer, the error of the l^{th} layer can be written as [39]

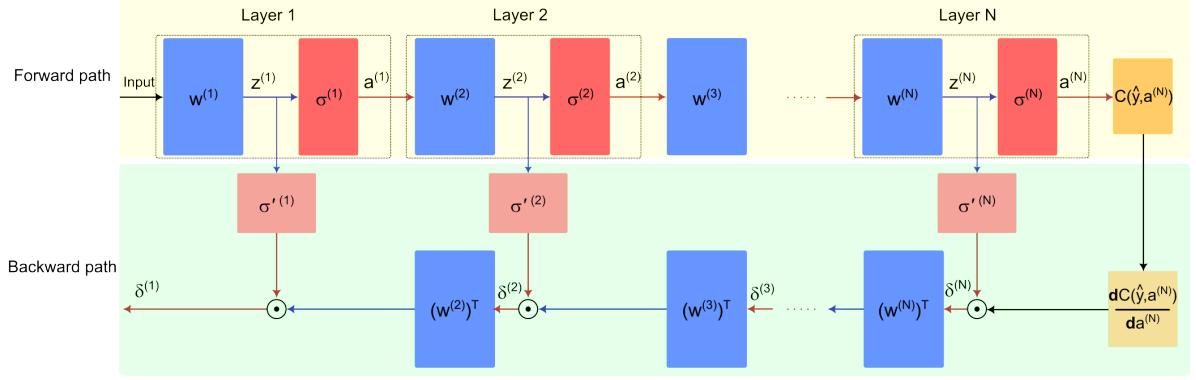


Fig. 1: Backpropagation training of a neural network. The neural network consists of N layers. $w^{(l)}$, $z^{(l)}$ and $\sigma^{(l)}$ are the weight matrix, the weighted-sum output, and the nonlinear activation function, respectively. The forward path generates an output by passing the input through neural layers and the output error is calculated using the cost function $C(\cdot)$. The backward path computes the error for each layer ($\delta^{(l)}$), starting with the output layer and backpropagating the error towards the input layer.

$$\delta^{(l)} = ((w^{(l+1)})^T \delta^{(l+1)} \odot \sigma'^{(l)}). \quad (4)$$

where T and \odot denote matrix transpose and Hadamard (element-wise) product, respectively. Using the calculated errors, the weights of the l^{th} layer can be updated using the following equation

$$w^{(l)} \rightarrow w^{(l)} - \eta(\delta^{(l)} a^{(l-1)}). \quad (5)$$

where η is the learning rate.

It can be seen that, to perform on-chip BP training, linear weight and sum, and nonlinear activation, as well as its gradient, are required. Integrated photonic implementation of the linear computation is more straightforward and has been demonstrated using a variety of approaches such as using P-doped-intrinsic-N-doped (PIN) modulators [17], PN phase modulators in a Mach-Zehnder interferometer (MZI) [19], network of MZIs with thermal phase shifters [20], phase change materials [23], and micro-ring modulators [26] to name a few. The more challenging part is the realization of the nonlinear activation and its gradient. Despite several demonstrations of on-chip photonic activation function, to the best of our knowledge, fully integrated end-to-end photonic implementation of BP training has not been reported yet, mainly due to the need for both nonlinear activation and its gradient. In this work we propose multiple techniques for realization of these functions using standard silicon photonic components.

Among several activation functions used in neural networks, sigmoid and rectified linear unit (ReLU) functions, and their variations, are very widely employed. Figure 2 shows our proposed opto-electronic schemes to approximate these functions and their gradients using intensity modulators (IMs) and micro-ring modulators (MRMs). As shown in Fig. 2a, in the forward path, an IM can be biased at high attenuation via a bias voltage ($V_{forward}$) and as the input voltage V_{in} increases, optical attenuation drops which results in a sigmoid-like function. The gradient function in the backward path can be realized using two cascaded IMs with opposite polarities (shown with different colors) simultaneously driven by the input with an offset voltage (*i.e.*, $V_{in} - V_{backward}$). For input values around $V_{backward}$, attenuation by both IMs is minimum, and increasing/decreasing input results in higher attenuation. We can also use an add-drop MRM to approximate sigmoid and its gradient as shown in Fig. 2b. The MRM is biased on-resonance (off-resonance using $V_{backward}$) and the output taken from through (drop) port implements sigmoid (gradient) function. A similar approach applies to ReLU approximation. A single IM can be used for the ReLU and its gradient which is a step function (Fig. 2c). The IM is initially biased at high attenuation in both cases and the only difference is the amplifier gain that is much higher for ReLU gradient. Similarly, the MRM is biased at resonance and by switching the electrical gain the through output approximates ReLU and its gradient (Fig. 2d). In both cases of ReLU approximation, $V_{forward}$ should be properly adjusted to avoid the flattening of the response. It is important to mention that other variations of sigmoid function [40], such as logistic sigmoid, hyperbolic tangent (tanh), and arc-tangent Function (arctan), as well as ReLU variations [41] like leaky ReLU, parametric ReLU, and exponential linear unit (ELU) can be implemented using the the proposed architectures.

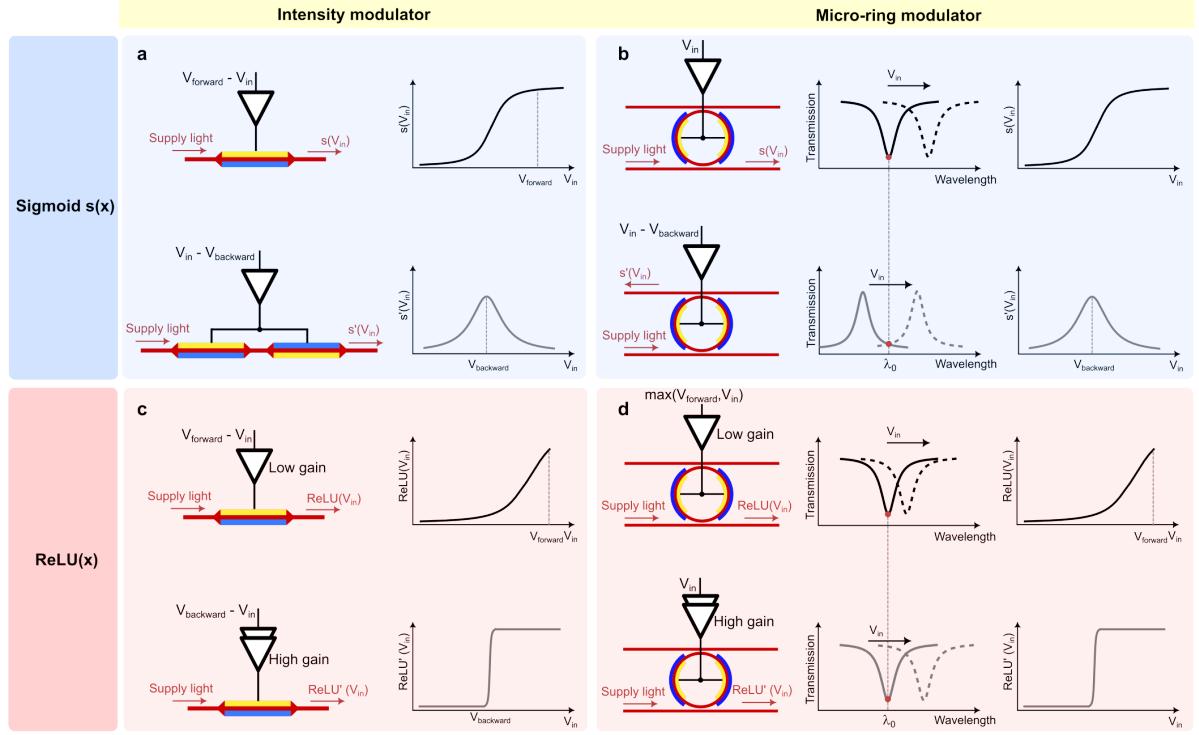


Fig. 2: Photonic nonlinear activation functions and gradients using IM and MRM. **a**, One IM is used to implement sigmoid function and two cascaded IMs approximate the gradient function. **b**, The through port of an add-drop MRM that is biased at resonance is used for sigmoid and the drop port for the gradient when the ring is biased off-resonance using $V_{backward}$. ReLU and its gradient (step function) can be implemented by switching the electrical gain using **c**, an IM initially biased at high attenuation, and **d**, a MRM that is biased at resonance.

Both IM and MRM are available in silicon photonic fabrication processes and can be used to implement ReLU and sigmoid functions in a PNN. In this work and as proof of concept, we utilize IM to implement ReLU activation and its gradient (Fig. 2c) in a photonic deep neural network and demonstrate full on-chip BP training and inference. Nevertheless, more details and experimental verification of all four implementations of Fig. 2 are presented in Supplementary Notes.

3 Photonic deep neural network implementation

Figure 3a shows the schematic of the implemented neural network, consisting of a forward path for inference, and a backward path for error calculation and BP training. The forward path starts with the input layer where two inputs, x_1 and x_2 , normalized between 0 and 1, are generated using two PIN attenuators. x_1 and x_2 are fully connected to the eight two-input weights ($w^{(1)} : 8 \times 2$) of the hidden layer, generating eight weighted-sum outputs ($z_i^{(1)}, i = [1, 8]$). Then, $z_1^{(1)}$ to $z_8^{(1)}$ pass through eight identical IM-based ReLU-like activation functions ($\sigma^{(1)}$), resulting in the outputs of the hidden layer ($a_i^{(1)}, i = [1, 8]$). The ReLU-like functions are generated using the circuit shown in Fig. 2c. Each output of the hidden layer is connected to a linear weight unit of the output layer ($w^{(1)} : 1 \times 8$), generating the weighted-sum of the eight inputs ($z^{(2)}$). The output, after passing through another ReLU activation function $\sigma^{(2)}$, is used to calculate the cost function $C(\hat{y}, a^{(2)})$. Note that $\sigma^{(2)}$ and $C(\hat{y}, a^{(2)})$ are implemented in the microcontroller unit. In this work, we use the mean squared error (MSE) as the cost function. Therefore, for n input data points, the cost function is calculated as

$$C(\hat{y}, a^{(2)}) = \frac{1}{n} \sum_{i=1}^n (\hat{y}_i - a_i^{(2)})^2. \quad (6)$$

As detailed in equations 1 to 5, in BP training, the goal is to update the network weights to minimize the cost function. To do so, we need to calculate the error associated with each layer (in this case $\delta^{(1)}$)

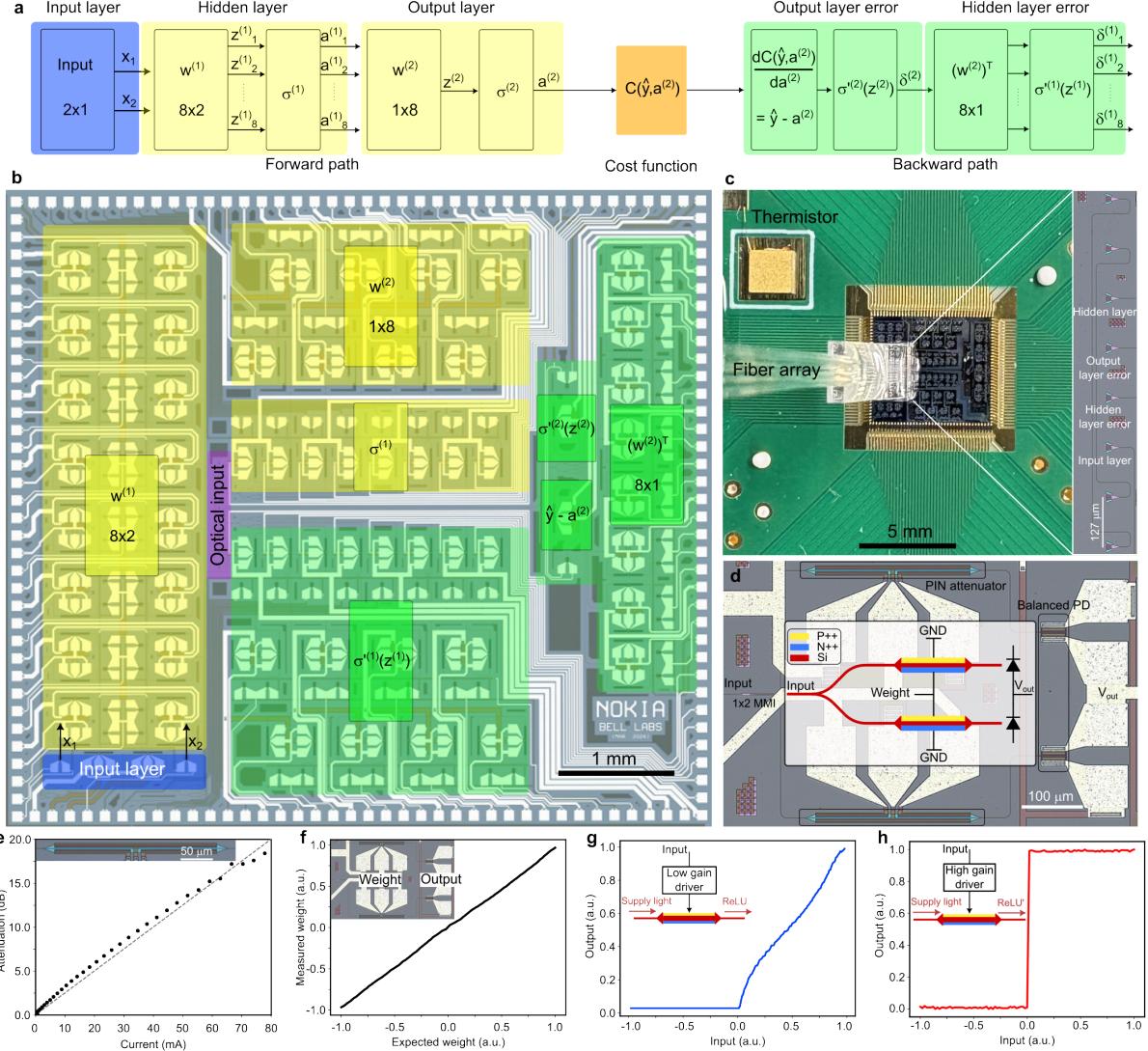


Fig. 3: Silicon photonic deep neural network chip. **a**, Schematic of the neural network architecture implemented on the silicon chip. The forward path consists of an input layer, a hidden layer and an output layer. The backward path calculates the errors corresponding to the hidden and output layers (*i.e.*, $\delta^{(1)}, \delta^{(2)}$). **b**, Silicon photonic chip photograph showing different network layers. **c**, Wirebonded and packaged chip with an 8-channel fiber array and a thermistor. Inset shows the grating coupler array. **d**, Chip photo and schematic of the linear weight. Two PIN attenuators are used in a push-pull configuration to implement positive and negative weights after balanced PD. **e**, Measured PIN attenuation as a function of injected current. **f**, Measured linear relationship between the input and output of the weight unit of panel **d**. Measured response of the **g**, ReLU (with low-gain amplifier) and **h**, its gradient (with high-gain amplifier), each implemented using a single PIN attenuator.

and $\delta^{(2)}$). According to equation 3, the output layer error $\delta^{(2)}$ is equal to $(\hat{y} - a^{(2)})\sigma'^{(2)}(z^{(2)})$, as shown in Fig. 3a. Similarly, $\delta_1^{(1)}$ to $\delta_8^{(1)}$ can be calculated using equation 4 by calculating the Hadamard product of the $(w^{(2)})^T \delta^{(2)}$ and $\sigma'^{(1)}(z^{(1)})$ (Fig. 3a). After error backpropagation, the results are used to update the weights of the hidden and output layers according to equation 5 and with fixed learning rate. On-chip training algorithm is further discussed in Supplementary Notes.

Figure 3b shows the photograph of chip fabricated in the Advanced Micro Foundry (AMF) silicon photonic process (see Supplementary Notes for more details). All computation blocks of Fig. 3a are highlighted on the chip. The picture of the packaged chip is shown in Fig. 3c. An 8-channel standard single-mode fiber array is attached to the chip to couple the input laser via an array of grating couplers. Four grating couplers in the middle of the array are routed to different layers of the network (Fig. 3c inset), and the ones at the two ends are used for fiber alignment (see Supplementary Notes for

details). The thermistor is mainly used for temperature monitoring. The PNN chip operates across a large optical bandwidth and does not require active temperature control (see Supplementary Notes). Figure 3d illustrates the linear weight unit in which the input optical signal is equally split into two signals using a 1×2 multi-mode interferometer (MMI). The signals are amplitude-modulated by two PIN attenuators connected in a push-pull configuration allowing for weights between -1 and 1 after balanced photo-detection (PD). The measured PIN attenuation as a function of the injected current is shown in Fig. 3e. Figure 3f compares the expected and measured weight values. As discussed before, a single PIN attenuator implements both ReLU function and its gradient. As shown in Fig. 3g, in low-gain mode, a ReLU-like behavior is observed. In the high-gain mode, a step function (ReLU gradient) is measured and shown in Fig. 3h.

4 Data classification training and inference demonstration

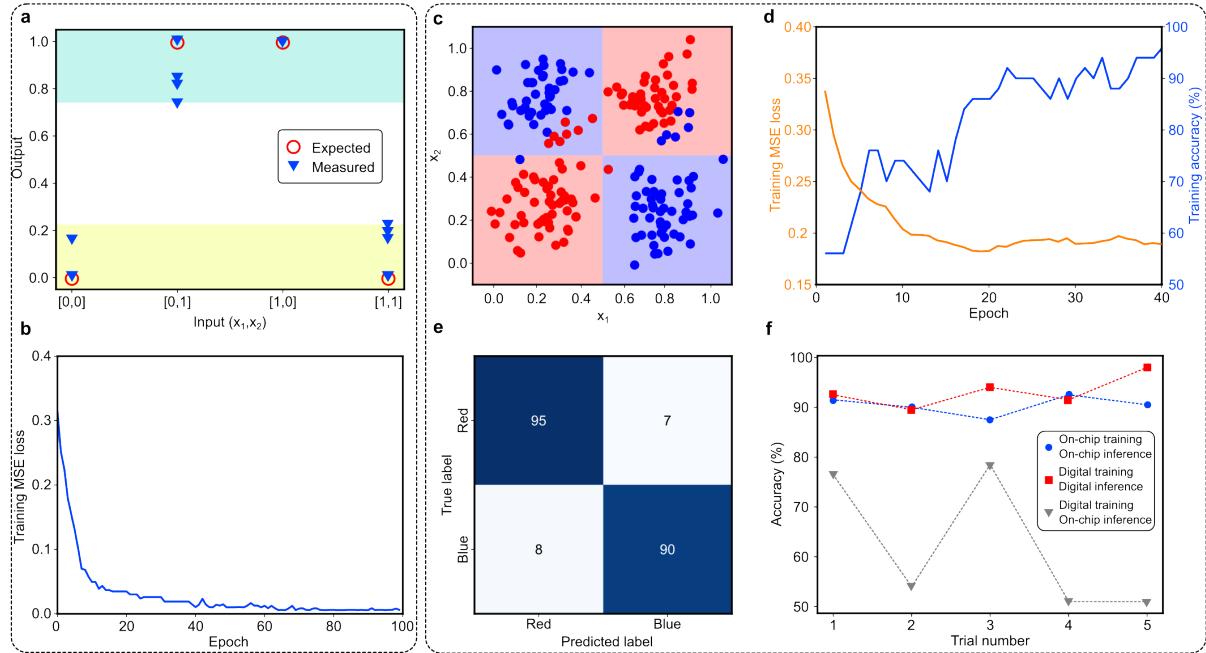


Fig. 4: Nonlinear data classification demonstration. **a**, Measured (blue triangles) and expected (red circles) XOR operation after on-chip BP training. The process is repeated multiple times and the cyan and yellow shaded regions show the variations in the output levels. **b**, MSE loss for XOR training. **c**, 2D point separation dataset. The blue and red shaded regions show true (expected) classes and points show the measured results. **d**, On-chip BP training MSE loss and accuracy and **e**, the confusion matrix corresponding to the results in panel c. **f**, Inference robustness for trials with different weight initializations. The graph compares end-to-end on-chip training and inference (blue), digital training and inference as the reference case (red), and digital training followed by on-chip inference (grey).

As proof of concept, we experimentally demonstrate two nonlinear data classification problems, namely logic XOR operation and a two-dimensional (2D) point separation task. The measurement setup is explained in details in Supplementary Notes. To show the logic XOR operation, the weights are randomly initialized around zero. Once on-chip training is performed, the PNN separates the two output classes for different input pairs. This process is repeated multiple times and Fig. 4a shows the normalized output levels after training where clear separation between output levels can be seen. Regions corresponding to logic “1” and “0” are shown in cyan and yellow, respectively. Figure 4b plots the training MSE loss as a function of the number of epochs.

As a more complex task, we solve a 2D point separation problem. The dataset consists of 200 randomly generated (x_1, x_2) points and the task is to separate them into blue and red points. The blue region corresponds to where $0 < x_1 < 0.5$ and $0.5 < x_2 < 1$ as well as where $0.5 < x_1 < 1$ and $0 < x_2 < 0.5$. The red region corresponds to $0 < x_1, x_2 < 0.5$ and $0.5 < x_1, x_2 < 1$. Figure 4c shows the blue and red shaded regions. To train the network, 50 points are randomly selected and the on-chip

BP training is run for 40 epochs. Figure 4d shows the training loss and accuracy as a function of the number of epochs. Highest inference accuracy of 92.5% (points shown in Fig. 4c) is achieved and Fig. 4e illustrates the corresponding confusion matrix.

One of the major advantages of full on-chip BP training is that it can compensate for the device-to-device variations caused by fabrication and environmental effects resulting in a more robust training and inference. In contrast, it is very challenging to take such variations into account in digital training of PNNs. We discuss and show the measured on-chip device variations in Supplementary Notes. To demonstrate this robustness, we consider three scenarios. On-chip training and inference (our proposed method), digital training and on-chip inference (conventional approach), and digital training and inference (reference case). The reference case is implemented in Python using the Tensorflow library [42] and the exact same neural network architecture as shown in Fig. 3a is implemented digitally. Figure 4f compares the inference accuracy of these three cases when repeated five times (trial number). In each trial, a different set of weight initializations is used. It can be seen that when the network is digitally trained (grey graph), inference accuracy varies considerably. This is expected as the training model does not incorporate actual device models and variations. Note that in a 2-class dataset, 50% accuracy corresponds to chance-level and is considered the baseline. However, when trained using the proposed on-chip BP training, the inference is significantly more robust and repeatable, without any prior knowledge of the actual variations. Moreover, comparing the blue and red curves shows that on-chip training and inference achieves accuracy on par with the reference digital training and inference, both in terms of absolute value as well as robustness.

5 Summary and discussion

We demonstrated the first end-to-end on-chip photonic deep neural network BP training and inference. Linear weights, nonlinear activation, and gradient are integrated on a single silicon photonic chip. As proof of concept, we experimentally solved nonlinear inference tasks of logic XOR operation and 2D points separation with inference accuracies on par with digital models. We showed that in presence of fabrication-induced variations, the robustness and repeatability of our on-chip training addresses the variability of digital training of photonic neural networks.

The proposed architecture benefits from per-layer supply light which enables scaling to larger networks. This results in a well-defined output signal power range for each layer, independent of other layers. However, the chip in Fig. 3 uses separate forward and backward paths that increase the number of optical inputs as each nonlinear block (main function or its gradient) requires a separate supply light. This necessitates more input optical power as well as more complex on-chip photonic routing which increases the chip area. To address this challenge, we propose a hardware reuse architecture that uses a single nonlinear block both for inference and training (the original function and its gradient), resulting in a reduction of the number of optical inputs and nonlinear blocks by a factor of two. In the modified architecture, the weight blocks also incorporate the multiplication of weight and error matrices (*i.e.*, $w^T \delta$ in Equation 4) such that during inference, error values are set to one and during training the matrix multiplication is performed. The nonlinear activation blocks are mode-switched by switching the electrical connection of one IM in Fig. 2a, the output optical port of the MRM in Fig. 2b, or the gain reconfiguration in Figs. 2c and d, depending the type of the nonlinear function. Details of the proposed architecture are presented in Supplementary Notes. Further scalability via chip area and energy reduction can be achieved using monolithic integration of electronic and photonic components [43, 44]. In this case, all required electronic control circuits can be placed next to the corresponding photonic circuit. This significantly reduces parasitic components, overall system footprint, and packaging complexities.

The focus of this work is mainly on improving training robustness and repeatability. Nevertheless, to enhance the processing speed, both for training and inference, high-speed amplitude modulation can be used. Silicon photonic MRMs enable modulation bandwidths beyond 67 GHz [45] within a small footprint, at the cost of requiring wavelength alignment and calibration. To ease the calibration requirements, compact electro-absorption modulators can be used that operate across a wide wavelength range while achieving modulation bandwidth of higher than 50 GHz [46].

To fully leverage the low latency and energy efficiency of PNNs, ensuring robustness is essential. Our end-to-end on-chip BP training and inference combines the versatility of BP training algorithm, high-yield fabrication of silicon photonic chips, and performance robustness which pave the way for larger scale deployment of PNNs to boost the performance of digital processing platforms.

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6 Data availability

The data supporting findings of this study is available from the corresponding author upon reasonable request.

7 Author contributions

F.A. conceived the idea. F. Ashtiani and M.H. Idjadi taped-out the chip, designed the electronic circuit board, and conducted the measurements. K.W. Kim packaged the photonic chip. F. Ashtiani wrote the paper. All authors reviewed the paper.

8 Competing interests

The authors declare no competing interests.

9 Additional information

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10 Supplementary Notes

Supplementary note 1: Experimental verification of sigmoid and ReLU approximation using IM and MRM

In this work and the implemented photonic chip, we used IM-based ReLU activation and its gradient as the nonlinearity and demonstrated training and inference for two classification tasks. Nonetheless, other proposed circuits shown in Fig. 2 can also serve as activation. Therefore, we conducted a series of measurements to demonstrate all nonlinear activation approximations. Supplementary Figure 1 shows the normalized measured activations and the corresponding gradients for all proposed architectures. In all plots, blue dots and red curves represent experimental and theoretical graphs, respectively. Supplementary Figures 1a and b show the results for sigmoid function and Supplementary Figs. 1c and d illustrate the results for ReLU function. Decent agreement between measurement and theory can be seen. It should be noted that to demonstrate MRM-based sigmoid and ReLU functions, we used an add-drop micro-disk modulator fabricated in AIM Photonics silicon photonic process with a similar response as a typical MRM (Supplementary Figs. 1b and d) [47]. The IM-based results are based on the same PIN attenuators (IMs) used in the PNN chip (Supplementary Figs. 1c and d).

Supplementary note 2: Training algorithm

On-chip training process follows the commonly used gradient descent-based BP algorithm. Supplementary Figure 2 illustrates the training process. The training dataset is stored in the microcontroller memory and the input pairs are loaded to the input layer as a vector ($X = (x_1, x_2)$). In parallel, hidden layer weights are loaded and the weighted-sum vector $W^{(1)}X$ is read and transferred to the ReLU non-linearity activation to generate $a^{(1)} = \sigma(W^{(1)}X)$. The optical output is routed to the output layer weight block and the resulting weighted-sum $W^{(2)}a^{(1)}$ is stored in the microcontroller memory. After applying another ReLU nonlinearity and calculating the cost function, the gradient of output layer activation $\sigma'(z^{(2)})$ is calculated on the chip and is then multiplied by the derivative of the cost function $\hat{y} - a^{(2)}$, which results in output layer error $\delta^{(2)}$. Next, the hidden layer error is calculated using the result of the previous step to generate $\delta^{(1)} = (W^{(2)})^T\delta^{(2)} \odot \sigma'(z^{(1)})$. Finally, the hidden and output layer weights are updated according to equation 5.

This process continues for the target number of epochs. The number of epochs is set such that the MSE loss stabilizes and does not become smaller. A learning rate (η) of 0.05 is used for on-chip BP training. Note that other variations of BP training such as adaptive learning rate, adding momentum to weight update, and Adam optimizer [48] can also be used in the proposed on-chip training.

Supplementary note 3: Chip fabrication

The photonic chip was fabricated in the AMF SOI silicon photonic process. The platform features $3\text{ }\mu\text{m}$ buried oxide and all on-chip routing is done using single-mode waveguides that are 220 nm thick and 500 nm wide, with a measured loss of less than 2 dBcm^{-1} . Supplementary Table 1 shows the specifications of the on-chip photonic components.

Supplementary note 4: Experimental setup and control electronics

Supplementary Figure 3a shows the picture of the experimental setup. The output of a tunable laser (santec TSL-570) at 1550 nm and 7 dBm optical power is split into four signals using fiber splitters. Each of the four signal passes through a polarization controller and connected to one input of the 8-channel fiber array attached to the chip. As shown in Fig. 3c, the fiber array is glued to the chip and proper alignment is done using the four end grating couplers (two on each end). The other four grating couplers couple the light to the input waveguide of each layer of the network (shown in Fig. 3c). The on-board thermistor is used to monitor the temperature and a temperature variation of about $\pm 2^\circ\text{C}$ around room temperature (22°C) was observed. No temperature control loop is used as the PIN attenuator works across a 100 nm bandwidth around 1550 nm and is not sensitive to such temperature variations. However, for implementations using resonance-based devices such as MRMs, temperature stabilization is necessary for reliable operation.

To write/read the data to/from the photonic chip, a custom electronic circuit board is designed. Supplementary Figure 3b shows the block diagram of the control electronics as well as a picture of the assembled board. The narrow and wide arrows represent single- and multi-signal connections, respectively. Four 12-bit 16-channel serial digital-to-analog converters (DACS) convert the data stored in the memory, including the weights and the inputs to the nonlinear activation functions and their gradients. The serial interface of the microcontroller and the DACs consists of data, clock, and chip-select signals.

An array of 60 operational amplifiers (OPAMPs) is used to drive the on-chip PIN attenuator. Read-out circuitry consists of six 8-bit parallel analog-to-digital converters (ADCs) to read 45 signals coming out of the photonic chip. The interface of the ADC array and the microcontroller includes 8 data lines, one chip select, and three address lines. A complete list of the components used in the experimental setup are provided in Supplementary Table 2.

Supplementary note 5: On-chip device variations

As discussed before, one of the primary goals of end-to-end on-chip BP training is to compensate for the device variations. Such variations, if not accounted for properly, can significantly degrade the repeatability, robustness, and accuracy of training and inference. While Fig. 4f shows the robustness of our implementation, it is important to study the actual device variations. Typical variations in thickness, width, and loss of a single-mode waveguide in AMF process are about 2.2%, 1.2%, and 17%, respectively [49]. Such variations result in considerable change in the effective index of refraction (n_{eff}) and the group index (n_g). Our MODE simulations show that the standard deviation of variations in n_{eff} and n_g are 0.0189 and 0.01, respectively, affecting the performance of the on-chip photonic devices.

To find out the actual effect of such variations, we conducted detailed measurements of all on-chip linear and nonlinear computation. Supplementary Figure 4 shows the variations of different on-chip photonic computation blocks. In all graphs, the area shaded in blue shows the variation and the red line corresponds to the average. Note that Figs. 3f, g, and h show the average graphs. Supplementary Figures 4a, b, c, and d correspond to the weight blocks of the hidden layer, output layer, output layer error calculation, and hidden layer error calculation, respectively. The photonic circuit for all weights is similar to the one shown in Fig. 3d. For weights between -1 and 1, a variation up to 0.273 can be seen which is significant. Supplementary Figure 4e shows the multiply-accumulate (MAC) operation accuracy using the on-chip weight blocks where the mean and standard deviation of error is measured to be -0.0047 and 0.3662, respectively. The ReLU activation and gradient approximations exhibit variations that are illustrated in Supplementary Figs. 4g and h. The variations in the gradient graphs is more significant mainly due to one of the PIN attenuators whose response is considerably different from others. Considering these measured variations, the on-chip training compensates for the errors as evident from the robustness test shown in Fig. 4f. In contrast, digital training does not perform robustly as it does not include the actual on-chip device variations.

Supplementary note 6: Hardware reuse architecture for scaling up

Per-layer supply light enables scaling as it prevents optical loss propagation across multiple layers. Each nonlinear block, both in the forward and backward paths, requires an interdependent supply light. Therefore, for an N -layer network, $2N$ supply lights are needed. This results in larger overall optical power consumption as well as more on-chip optical routing which increases the chip area. To address this challenge, we propose a hardware reuse architecture as shown in Supplementary Fig. 5. The idea is to use a single nonlinear block in each layer both in inference and training. In this figure, the forward path consists of modified weight and nonlinear activation blocks such that the same blocks can be configured for training and inference. The modified weight block of the i^{th} layer consists of two arrays of IMs, one to encode matrix $(\delta^{(i)})^T$ and one to encode matrix $w^{(i)}$. In the inference mode, the first array is transparent (transmission of one) and the input to the block is multiplied by the weight matrix. In BP training mode however, the error matrix $(\delta^{(i)})^T$ is loaded to the first array of modulators and the output of the modified weight block is equal to $(\delta^{(i)})^T w^{(i)}$. Note that equation 4 can be written as

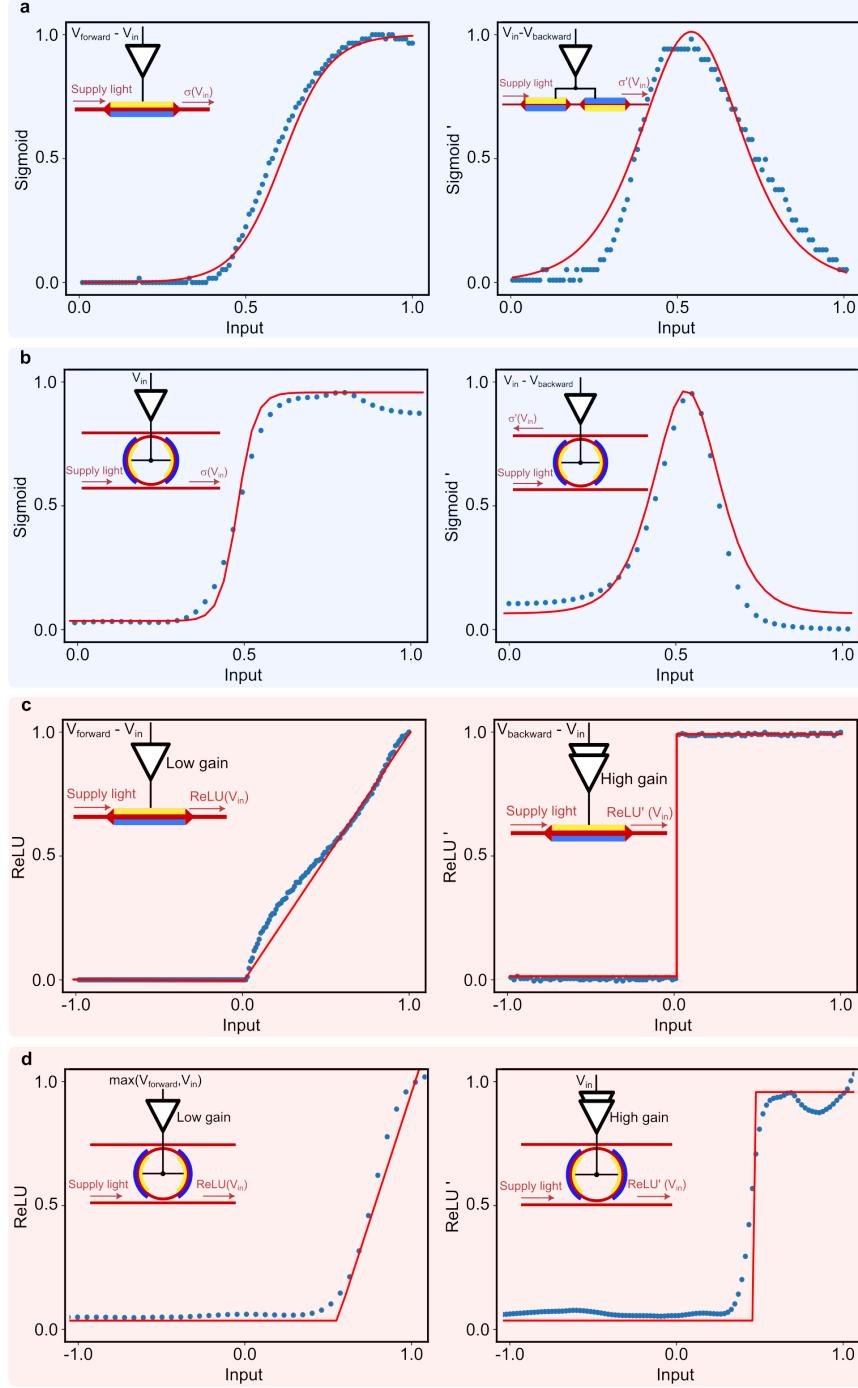
$$\delta^{(i-1)} = ((\delta^{(i)})^T w^{(i)})^T \odot \sigma'^{(i-1)}. \quad (7)$$

Therefore, to compute $\delta^{(i-1)}$, the transpose of the output of modified weight block should be multiplied by the gradient of the nonlinear activation of the previous layer ($\sigma'^{(i-1)}$). This is performed in the Hadamard product block which is an array of parallel IMs whose optical input is $\sigma'^{(i-1)}$ and electrical input is $((\delta^{(i)})^T w^{(i)})^T$.

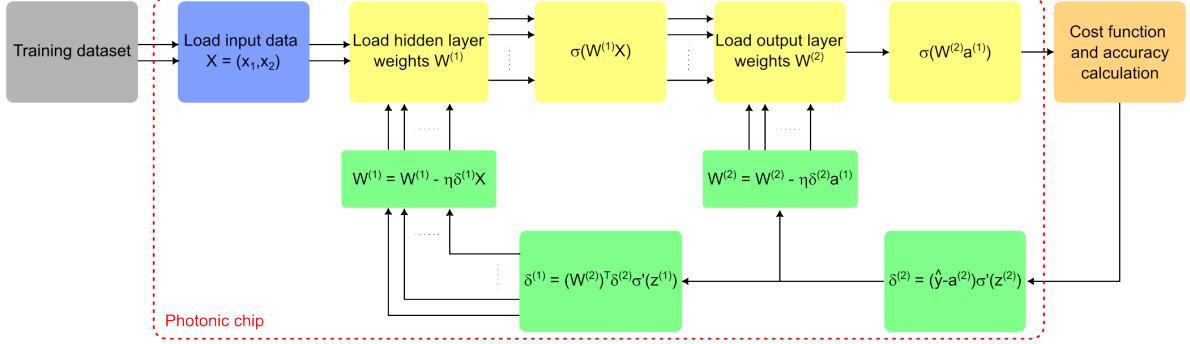
The nonlinear activation block is also modified to a mode switching activation that generates the desired output based on the mode of operation (inference or training). Depending on the type of nonlinear function (Fig. 2), the activation block can be designed. For IM-based sigmoid activation, the electrical connection of one of the IMs can be switched to change between sigmoid and its gradient. The switch is open for inference and closed for training. In the MRM-based implementation, an optical switch can be used to take the output either from the through port (inference) or from the drop port (training). In the case of ReLU activation, a programmable gain amplifier can be utilized in both IM- and MRM-based architectures where low (high) gain is set for inference (training). All of the proposed mode switching

activation circuits are schematically shown in Supplementary Fig. 5.

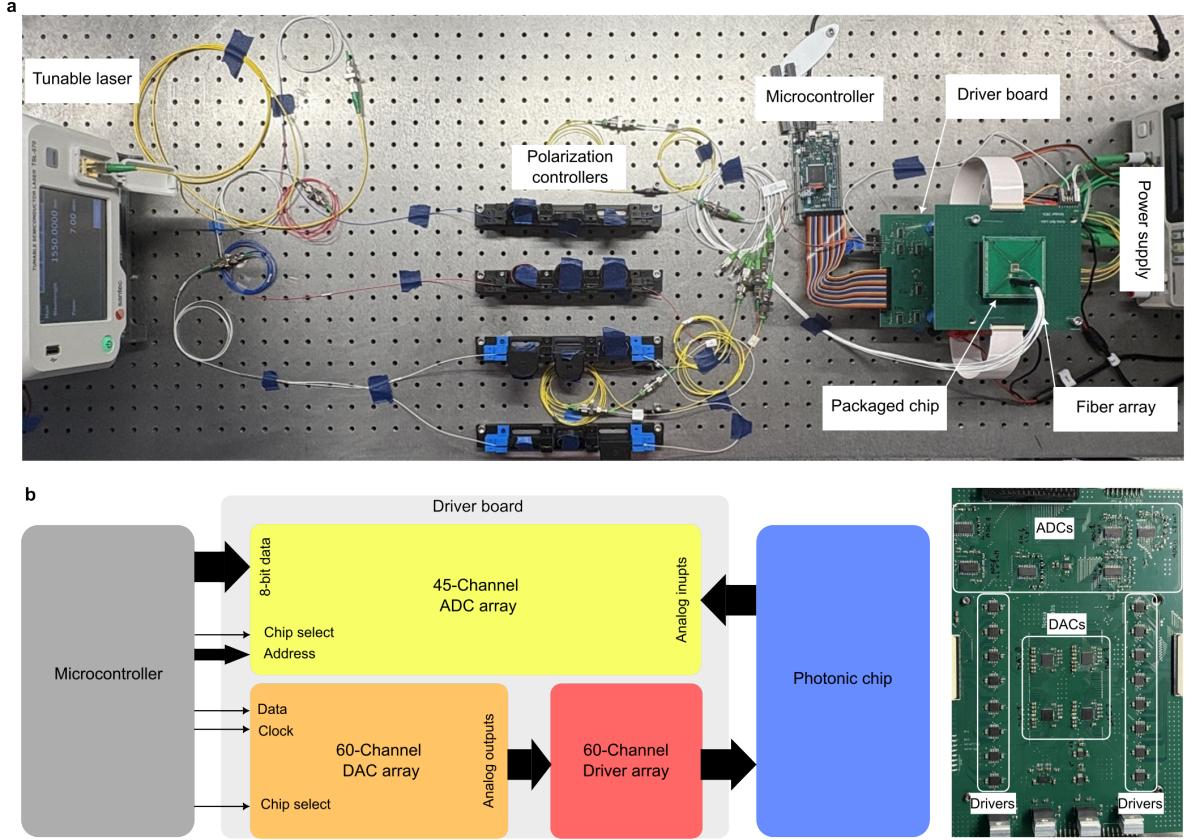
In addition to reducing the number of optical inputs by a factor of two, the number of nonlinear blocks is also half of the original design, further reducing the chip area and the number of components. Moreover, the proposed approach reduces the number of electronic components controlling the reused nonlinear blocks which in turn simplifies the system design.



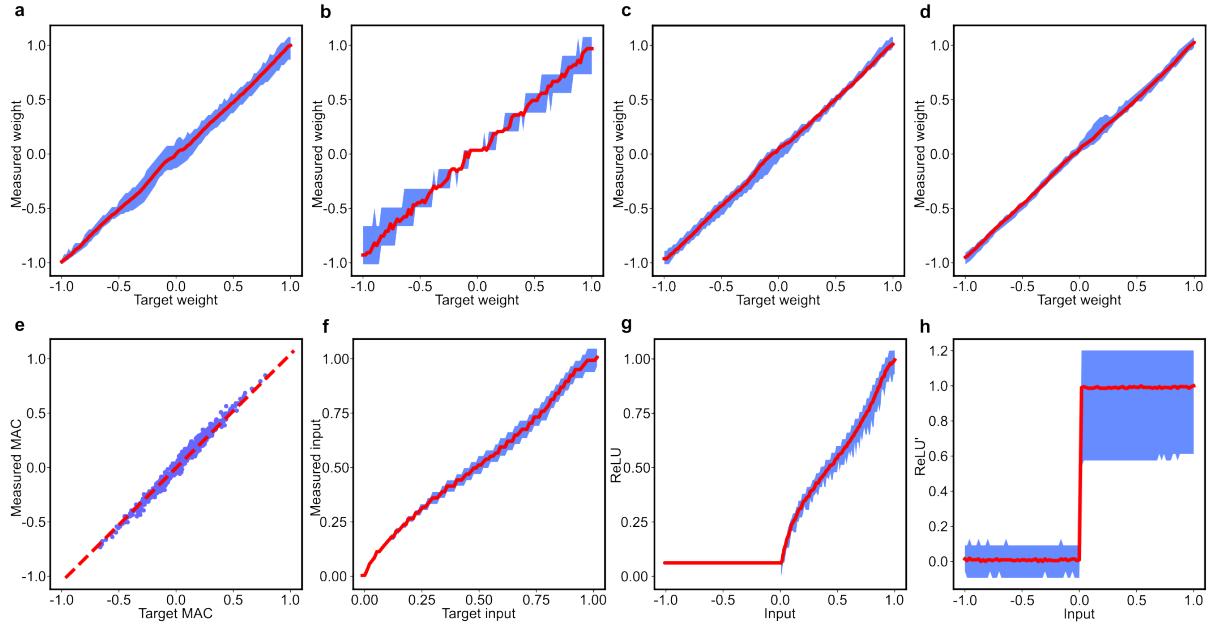
Supplementary Fig. 1: **Photonic approximation of sigmoid and ReLU using IM and MRM.** Normalized experimental (blue dots) and theoretical (red lines) graphs of sigmoid and ReLU nonlinear activations using the architectures shown in Fig. 2. Sigmoid and its gradient using **a**, IM and **b**, MRM. ReLU and its gradient using **c**, IM and **d**, MRM.



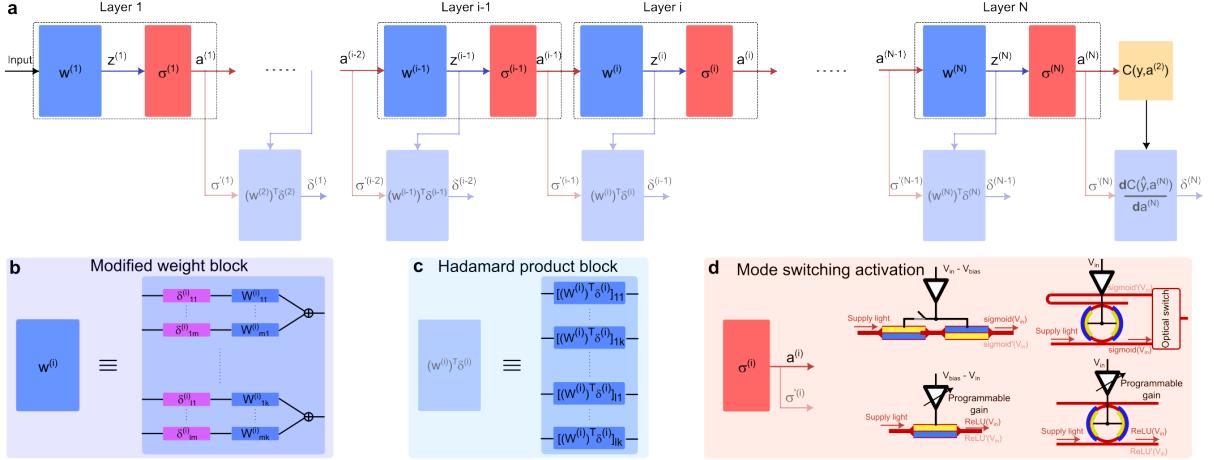
Supplementary Fig. 2: **On-chip BP training process.** Training data and hidden layer weights are loaded their corresponding modulators. Weighted-sum output of the hidden layer ($z^{(1)} = w^{(1)}X$) is read to drive its ReLU nonlinearity and generate $a^{(1)} = \sigma(w^{(1)}X)$ that is multiplied by the output layer weight matrix. All acquired data are stored in a memory for training. Output nonlinearity and cost function are applied to the result in the microcontroller. In the backward path, weighted-sum (z) and neural output (a) signals are recalled from the memory and loaded to the corresponding modulators to calculate output and hidden layer errors ($\delta^{(1)}$ and $\delta^{(2)}$) and update the weights accordingly.



Supplementary Fig. 3: **Experimental setup and control electronics.** **a**, Picture of the experimental setup. The output of a tunable laser is split into four signals using fiber splitters. After polarization adjustment, the four optical signals are vertically coupled to the chip using a single-mode fiber array. A microcontroller together with a custom designed electronic circuit board control the photonic chip. **b**, Block diagram and picture of the control electronic circuit consisting of an array of ADCs to read the output signals, and an array of DACs followed by drivers to write the data to the photonic chip.



Supplementary Fig. 4: **On-chip device variations.** Measured variations of various neural network layer blocks. **a**, Hidden layer weights. **b**, Output layer weights. **c**, Output layer error calculation weights. **d**, Hidden layer error calculation weights. **e**, Accuracy of MAC operation used in weight blocks. **f**, Input layer data mapping. **g**, ReLU nonlinear activation and **h**, its gradient.



Supplementary Fig. 5: **On-chip BP training via hardware reuse for improved scaling.** **a**, Block diagram of an N-layer neural network with N reused nonlinear blocks. **b**, Linear weight blocks are modified to include modulators for layer error values (*i.e.*, δ^i). These modulators are transparent (full transmission mode) during inference and are used in training to calculate $(\delta^i)^T w^i$. **c**, Hadamard product block consisting of an array of weights similar to that of Fig. 3d to calculate $((w^i)^T \delta^i) \odot \sigma'(i)$. **d**, Mode switching nonlinear activation. Depending on the type of nonlinear activation, a single block operates in training and inference modes by switching electrical connection, gain, and output port.

Supplementary Table 1: **On-chip device specifications**

Component	Microphotograph	Specification
Grating coupler		Coupling loss = 5 dB
1x2 MMI		Excess loss = 0.1 dB
PIN attenuator		Insertion loss = 0.2 dB
Silicon-Germanium photodiode		Responsivity = 1.1 A/W

Supplementary Table 2: **Experimental setup equipment list**

Component	Model
Tunale laser	Santec TSL-570
Microcontroller	ATMEL AT91SAM3X8E
Analog-to-digital converter (ADC)	Analog Devices ADC7829
Digital-to-analog converter (DAC)	Texas Instruments DAC81416
Driver op-amp	Texas Instruments OPA4991
DAC voltage regulator	Analog Devices LT3097, LT3042
Driver voltage regulator	Texas Instruments LM337, LM338
ADC voltage regulator	Analog Devices LT3042
DC power supply	SIGLENT SPD3303X-E