Digital Design and Computer Architecture LU

Lab Protocol

Exercise I

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Vienna, April 7, 2022

Task 1: Introduction and Preparations

Subtask 1

Create a screenshot of the RTL netlist viewer, showing how the outputs of the PLL are connected to the rest of the system!

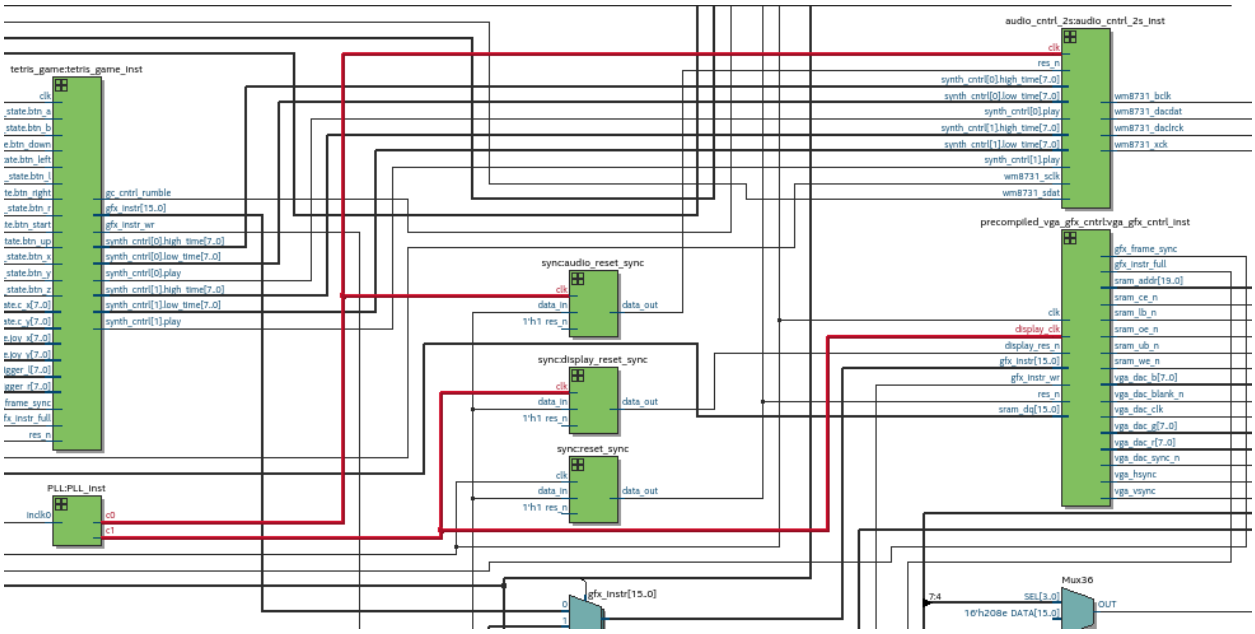

Figure 1: RTL netlist viewer screenshot

END Subtask 1

Task 2: GameCube Controller

Subtask 2

Analyse the resource usage of your gc_cntrl! You can find this information in the compilation report under the entry "Analysis&Synthesis".

	Combinational ALUTs	Dedicated Logic Registers
Absolute number	177	215
% of whole design	4.22%	7.69%
% of whole FPGA resources	0.15%	0.18%

END Subtask 2

Task 3: Decimal Printer

Subtask 3

Include the state graph of the state machine you designed and briefly explain how it works.

The FSM gets initialized to WAIT_START, when the signal start gets set to high the state machine transissions to START_GFX_INSTR, where it stays for one cycle and sends the move_gp instruction. Afterwards it stays for one clock cycle in SEND_X and SEND_Y each where it sends x and y respectively. Then it transitions into SEND_BLIT_INIT which sets up the environment for the next run of SEND_BLIT_DATA. This state subtracts from the current number 10 to the power of digit_counter and the FSM stays in this state until the number is smaller than 10**digit_counter number. In that case it sends the information for what digit to write to the gfx controller, decreases the digit_counter by one and in most cases returns to the previous state: SEND_BLIT_DATA. If digit_counter equals -1 though, the conversion is finished and the FSM will transition to the inital WAIT_START state.

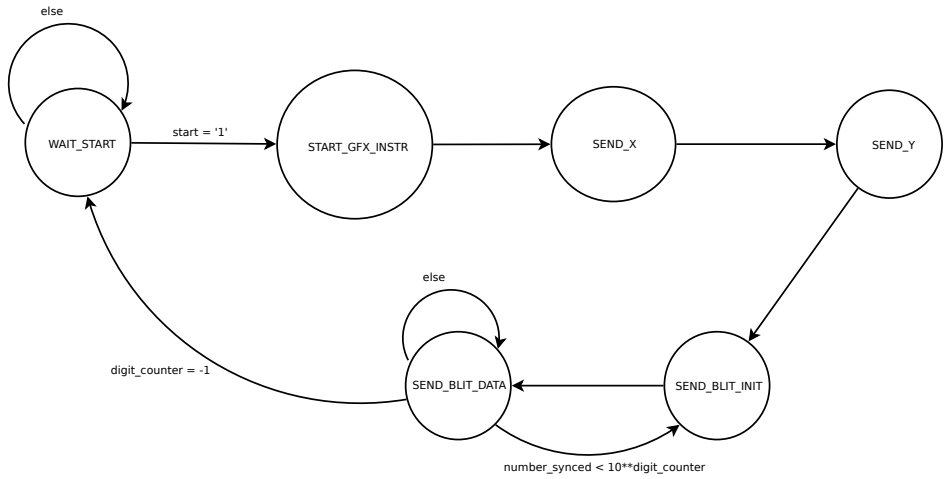

Figure 2: FSM state graph

END Subtask 3