PROL16: Scan Test

Übungsprotokoll zur Übung 3

Metrikorientierter Hardwareentwurf

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1 Einbau der Scan-Kette

1.1 Design Rule Check vor dem Einbau der Scan-Kette

Der Design Rule Check vor dem Einbau der Scan-Kette lief fehlerfrei durch.

cpu.pre_scan.drc:

```
In mode: all_dft...
  Pre-DFT DRC enabled

Information: Starting test design rule checking. (TEST-222)
  Loading test protocol
  ...basic checks...
  ...basic sequential cell checks...
          ...checking for scan equivalents...
  ...checking vector rules...
  ...checking pre-dft rules...

---------------------------------------------------------------
  DRC Report
  Total violations: 0
---------------------------------------------------------------
Test Design rule checking did not find violations
---------------------------------------------------------------
  Sequential Cell Report
  0 out of 199 sequential cells have violations
---------------------------------------------------------------
SEQUENTIAL CELLS WITHOUT VIOLATIONS
    * 199 cells are valid scan cells

Information: Test design rule checking completed. (TEST-123)
Current design is 'cpu'.
Current design is 'cpu'.
```

1.2 Design Rule Check nach dem Einbau der Scan-Kette

Der Design Rule Check nach dem Einbau der Scan-Kette lief fehlerfrei durch.

cpu.drc:

```
In mode: Internal_scan...
  Design has scan chains in this mode
  Design is scan routed
  Post-DFT DRC enabled

Information: Starting test design rule checking. (TEST-222)
  Loading test protocol
  ...basic checks...
  ...basic sequential cell checks...
  ...checking vector rules...
  ...checking clock rules...
  ...checking scan chain rules...
  ...checking scan compression rules...
  ...checking X-state rules...
  ...checking tristate rules...
  ...extracting scan details...

---------------------------------------------------------------
  DRC Report
  Total violations: 0
---------------------------------------------------------------
Test Design rule checking did not find violations
---------------------------------------------------------------
  Sequential Cell Report
  0 out of 199 sequential cells have violations
---------------------------------------------------------------

SEQUENTIAL CELLS WITHOUT VIOLATIONS
     * 199 cells are valid scan cells

Information: Test design rule checking completed. (TEST-123)
```

cpu.scan_report:

```
****************************************
Report : Scan path
Design : cpu
Version: B-2008.09-SP3
Date   : Wed Nov 25 08:48:25 2015
****************************************

========================================
TEST MODE: Internal_scan
VIEW     : Existing DFT
========================================

========================================
AS SPECIFIED BY USER
========================================

========================================
AS BUILT BY insert_dft
========================================

Scan_path    Len   ScanDataIn  ScanDataOut ScanEnable  MasterClock SlaveClock
-----------  ----- ----------- ----------- ----------- ----------- -----------
I 1          199   mem_data_i[0] mem_data_o[0] scan_enable_i clk_i -

****************************************
Report : DFT signals
Design : cpu
Version: B-2008.09-SP3
Date   : Wed Nov 25 08:48:25 2015
****************************************

========================================
TEST MODE: all_dft_user
VIEW     : Existing DFT
========================================
Port           SignalType        Active    Hookup    Timing    Usage
----------     ----------        ------    ------    ------    -----
test_mode_i    Constant          1         -
mem_data_o[0]  ScanDataOut       -         -
mem_data_i[0]  ScanDataIn        -         -
scan_enable_i  ScanEnable        1         -
clk_i          ScanMasterClock   1         -         P 100.0 R 45.0 F 55.0
clk_i          MasterClock       1         -         P 100.0 R 45.0 F 55.0
res_i          Reset             0         -         P 100.0 R 55.0 F 45.0
========================================
TEST MODE: all_dft_protocol
VIEW     : Existing DFT
```

```
=======================================
Port          SignalType       Active   Hookup   Timing   Usage
----------    ----------       ------   ------   ------   -----
test_mode_i     Constant         1      -
mem_data_o[0]    ScanDataOut      -      -
mem_data_i[0]    ScanDataIn       -      -
scan_enable_i    ScanEnable       1      -
clk_i          ScanMasterClock    1      -      P 100.0 R 45.0 F 55.0
clk_i          MasterClock        1      -      P 100.0 R 45.0 F 55.0
res_i          Reset              0      -      P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: all_dft
VIEW    : Existing DFT
=======================================
Port          SignalType       Active   Hookup   Timing   Usage
----------    ----------       ------   ------   ------   -----
test_mode_i     Constant         1      -
mem_data_o[0]    ScanDataOut      -      -
mem_data_i[0]    ScanDataIn       -      -
scan_enable_i    ScanEnable       1      -
clk_i          ScanMasterClock    1      -      P 100.0 R 45.0 F 55.0
clk_i          MasterClock        1      -      P 100.0 R 45.0 F 55.0
res_i          Reset              0      -      P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: Internal_scan_user
VIEW    : Existing DFT
=======================================
Port          SignalType       Active   Hookup   Timing   Usage
----------    ----------       ------   ------   ------   -----
test_mode_i     Constant         1      -
mem_data_o[0]    ScanDataOut      -      -
mem_data_i[0]    ScanDataIn       -      -
scan_enable_i    ScanEnable       1      -
clk_i          ScanMasterClock    1      -      P 100.0 R 45.0 F 55.0
clk_i          MasterClock        1      -      P 100.0 R 45.0 F 55.0
res_i          Reset              0      -      P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: Internal_scan_protocol
VIEW    : Existing DFT
=======================================
Port          SignalType       Active   Hookup   Timing   Usage
----------    ----------       ------   ------   ------   -----
test_mode_i     Constant         1      -
mem_data_o[0]    ScanDataOut      -      -
mem_data_i[0]    ScanDataIn       -      -
scan_enable_i    ScanEnable       1      -
clk_i          ScanMasterClock    1      -      P 100.0 R 45.0 F 55.0
clk_i          MasterClock        1      -      P 100.0 R 45.0 F 55.0
res_i          Reset              0      -      P 100.0 R 55.0 F 45.0
```

```
=======================================
TEST MODE: Internal_scan
VIEW    : Existing DFT
=======================================
Port           SignalType       Active   Hookup   Timing   Usage
----------     ----------       ------   ------   ------   -----
test_mode_i    Constant         1        -
mem_data_o[0]  ScanDataOut      -        -
mem_data_i[0]  ScanDataIn       -        -
scan_enable_i  ScanEnable       1        -
clk_i          ScanMasterClock  1        -        P 100.0 R 45.0 F 55.0
clk_i          MasterClock      1        -        P 100.0 R 45.0 F 55.0
res_i          Reset            0        -        P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: Mission_mode_user
VIEW    : Existing DFT
=======================================
Port           SignalType       Active   Hookup   Timing   Usage
----------     ----------       ------   ------   ------   -----
test_mode_i    Constant         1        -
mem_data_o[0]  ScanDataOut      -        -
mem_data_i[0]  ScanDataIn       -        -
scan_enable_i  ScanEnable       1        -
clk_i          ScanMasterClock  1        -        P 100.0 R 45.0 F 55.0
clk_i          MasterClock      1        -        P 100.0 R 45.0 F 55.0
res_i          Reset            0        -        P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: Mission_mode_protocol
VIEW    : Existing DFT
=======================================
Port           SignalType       Active   Hookup   Timing   Usage
----------     ----------       ------   ------   ------   -----
test_mode_i    Constant         1        -
mem_data_o[0]  ScanDataOut      -        -
mem_data_i[0]  ScanDataIn       -        -
scan_enable_i  ScanEnable       1        -
clk_i          ScanMasterClock  1        -        P 100.0 R 45.0 F 55.0
clk_i          MasterClock      1        -        P 100.0 R 45.0 F 55.0
res_i          Reset            0        -        P 100.0 R 55.0 F 45.0
=======================================
TEST MODE: Mission_mode
VIEW    : Existing DFT
=======================================
Port           SignalType       Active   Hookup   Timing   Usage
----------     ----------       ------   ------   ------   -----
test_mode_i    Constant         1        -
mem_data_o[0]  ScanDataOut      -        -
mem_data_i[0]  ScanDataIn       -        -
scan_enable_i  ScanEnable       1        -
```

```
clk_i          ScanMasterClock    1       -       P 100.0 R 45.0 F 55.0
clk_i          MasterClock        1       -       P 100.0 R 45.0 F 55.0
res_i          Reset              0       -       P 100.0 R 55.0 F 45.0

****************************************
Report : DFT configuration
Design : cpu
Version: B-2008.09-SP3
Date   : Wed Nov 25 08:48:25 2015
****************************************

DFT Structures                  Status
--------------                  --------
Scan:                           Enable
Fix Sets:                       Disable
Fix Resets:                     Disable
Fix Clocks:                     Disable
Fix Busses:                     Enable
Fix Bdirectional Ports:         Enable
Fix X Propagation:              Disable
Control Points:                 Disable
Observe Points:                 Disable
Logic BIST:                     Disable
Wrapper:                        Disable
Boundary scan:                  Disable
Scan Compression:               Disable
Pipeline Scan Data:             Disable
Clock Controller:               Disable
ConnectClockGating:             Enable
Mode Decoding Style:            Binary
```

2 Golden Simulation

Die Simulation lief ohne Fehler durch. Zum Testen wurde das Assemblerprogramm einer früheren Übung verwendet. Unten befindet sich die Ausgabe der Simulation.

```
# Loading timing data from ../syn/netlist/cpu.sdf
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#    Time: 0 ps  Iteration: 0  Instance: /cpu_tb File: ../src/cpu_tb.vhd
run –all
#
#  Assembling 0308 lines complete, code & data size 00579 words
# Write Memory Dump File: from address 8000h size 00512 words
```