PROL16: Scan Test

Übungsprotokoll zur Übung 3

Metrikorientierter Hardwareentwurf

Bernhard Selymes, Reinhard Penn, Robert Zeugswetter

01.12.2015

# 1 Einbau der Scan-Kette

## 1.1 Design Rule Check vor dem Einbau der Scan-Kette

Der Design Rule Check vor dem Einbau der Scan-Kette lief fehlerfrei durch.

**cpu.pre\_scan.drc:**

In mode: all\_dft...  
 Pre-DFT DRC enabled  
  
Information: Starting test design rule checking. (TEST-222)  
 Loading test protocol  
 ...basic checks...  
 ...basic sequential cell checks...  
 ...checking for scan equivalents...  
 ...checking vector rules...  
 ...checking pre-dft rules...  
  
-----------------------------------------------------------------  
 DRC Report  
 Total violations: 0  
-----------------------------------------------------------------  
Test Design rule checking did not find violations  
-----------------------------------------------------------------  
 Sequential Cell Report  
 0 out of 199 sequential cells have violations  
-----------------------------------------------------------------  
SEQUENTIAL CELLS WITHOUT VIOLATIONS  
 \* 199 cells are valid scan cells  
  
Information: Test design rule checking completed. (TEST-123)  
Current design is 'cpu'.  
Current design is 'cpu'.

## 1.2 Design Rule Check nach dem Einbau der Scan-Kette

Der Design Rule Check nach dem Einbau der Scan-Kette lief fehlerfrei durch.

**cpu.drc:**

In mode: Internal\_scan...  
 Design has scan chains in this mode  
 Design is scan routed  
 Post-DFT DRC enabled  
  
Information: Starting test design rule checking. (TEST-222)  
 Loading test protocol  
 ...basic checks...  
 ...basic sequential cell checks...  
 ...checking vector rules...  
 ...checking clock rules...  
 ...checking scan chain rules...  
 ...checking scan compression rules...  
 ...checking X-state rules...  
 ...checking tristate rules...  
 ...extracting scan details...  
  
-----------------------------------------------------------------  
 DRC Report  
 Total violations: 0  
-----------------------------------------------------------------  
Test Design rule checking did not find violations  
-----------------------------------------------------------------  
 Sequential Cell Report  
 0 out of 199 sequential cells have violations  
-----------------------------------------------------------------  
  
SEQUENTIAL CELLS WITHOUT VIOLATIONS  
 \* 199 cells are valid scan cells  
  
Information: Test design rule checking completed. (TEST-123)

**cpu.scan\_report:**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
Report : Scan path  
Design : cpu  
Version: B-2008.09-SP3  
Date : Wed Nov 25 08:48:25 2015  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
  
========================================  
TEST MODE: Internal\_scan  
VIEW : Existing DFT  
========================================  
  
========================================  
AS SPECIFIED BY USER  
========================================  
  
========================================  
AS BUILT BY insert\_dft  
========================================  
  
Scan\_path Len ScanDataIn ScanDataOut ScanEnable MasterClock SlaveClock  
----------- ----- ----------- ----------- ----------- ----------- -----------  
I 1 199 mem\_data\_i[0] mem\_data\_o[0] scan\_enable\_i clk\_i -  
  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
Report : DFT signals  
Design : cpu  
Version: B-2008.09-SP3  
Date : Wed Nov 25 08:48:25 2015  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
  
========================================  
TEST MODE: all\_dft\_user  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: all\_dft\_protocol  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: all\_dft  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Internal\_scan\_user  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Internal\_scan\_protocol  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Internal\_scan  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Mission\_mode\_user  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Mission\_mode\_protocol  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
========================================  
TEST MODE: Mission\_mode  
VIEW : Existing DFT  
========================================  
Port SignalType Active Hookup Timing Usage  
---------- ---------- ------ ------ ------ -----  
test\_mode\_i Constant 1 -  
mem\_data\_o[0] ScanDataOut - -  
mem\_data\_i[0] ScanDataIn - -  
scan\_enable\_i ScanEnable 1 -  
clk\_i ScanMasterClock 1 - P 100.0 R 45.0 F 55.0  
clk\_i MasterClock 1 - P 100.0 R 45.0 F 55.0  
res\_i Reset 0 - P 100.0 R 55.0 F 45.0  
  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
Report : DFT configuration  
Design : cpu  
Version: B-2008.09-SP3  
Date : Wed Nov 25 08:48:25 2015  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
  
DFT Structures Status  
-------------- --------  
Scan: Enable  
Fix Sets: Disable  
Fix Resets: Disable  
Fix Clocks: Disable  
Fix Busses: Enable  
Fix Bdirectional Ports: Enable  
Fix X Propagation: Disable  
Control Points: Disable  
Observe Points: Disable  
Logic BIST: Disable  
Wrapper: Disable  
Boundary scan: Disable  
Scan Compression: Disable  
Pipeline Scan Data: Disable  
Clock Controller: Disable  
ConnectClockGating: Enable  
Mode Decoding Style: Binary

# 2 Golden Simulation

Die Simulation lief ohne Fehler durch. Zum Testen wurde das Assemblerprogramm einer früheren Übung verwendet. Unten befindet sich die Ausgabe der Simulation.

# Loading timing data from ../syn/netlist/cpu.sdf  
# \*\* Note: (vsim-3587) SDF Backannotation Successfully Completed.  
# Time: 0 ps Iteration: 0 Instance: /cpu\_tb File: ../src/cpu\_tb.vhd  
run –all  
#   
# Assembling 0308 lines complete, code & data size 00579 words  
# Write Memory Dump File: from address 8000h size 00512 words