TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4021BP, TC4021BF, TC4021BFN

TC4021B 8 - STAGE STATIC SHIFT REGISTER (ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT)

TC4021B is 8 stage parallel in/serial out shift register, which can be used also for serial in/serial out operations. In the case of parallel operation, the data of PARALLEL IN is input to each F/F asynchronously with CLOCK and the output is obtained. In the case of serial operations, each F/F is triggered by rising edge of CLOCK. (ASYNCHRONOUS PARALLEL OR SYNCHRONOUS SERIAL INPUT) Switching of PARALLEL operation and SERIAL operation is achieved by P/\overline{S} CONTROL input. When P/\overline{S} CONTROL input is "H", PARALLEL operation is designated and when it is "L", SERIAL operation is designated.

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	٧
Input Voltage	V _{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	>
Output Voltage	V _{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	٧
DC Input Current	I _{IN}	± 10	mA
Power Dissipation	P _D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T _{opr}	- 40~85	°C
Storage Temperature Range	T _{stg}	- 65~150	°C

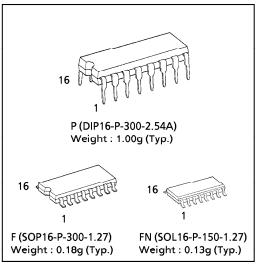
TRUTH TABLE

		OUTPUTS△				
CLOCK △△	P/S	PI1	Pln	SI	Q1	Qn
\Box	L	*	*	L	L	Qn - 1
	L	*	*	Н	Н	Qn - 1
	L	*	*	*	No Change	
*	Н	L	L	*	L	L
*	Н	L	Н	*	L	Н
*	Н	Η	L	*	Н	L
*	Н	Ι	Н	*	Н	Н

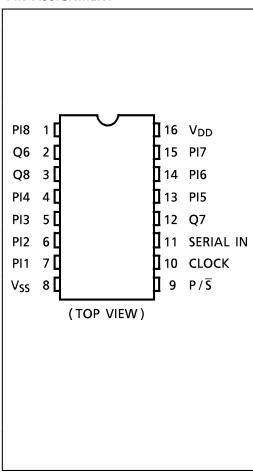
: 2~8

: Q1 ~ Q5 Internal Δ $\triangle \triangle$: Level Change : Don't Care

(Note) The JEDEC SOP (FN) is not available in

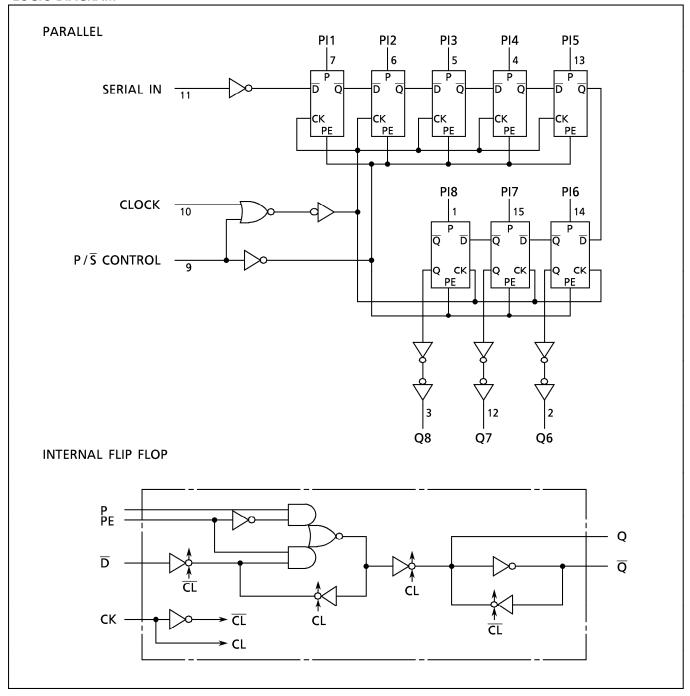


PIN ASSIGNMENT



TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V _{DD}		3	_	18	V
Input Voltage	V _{IN}		0	_	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

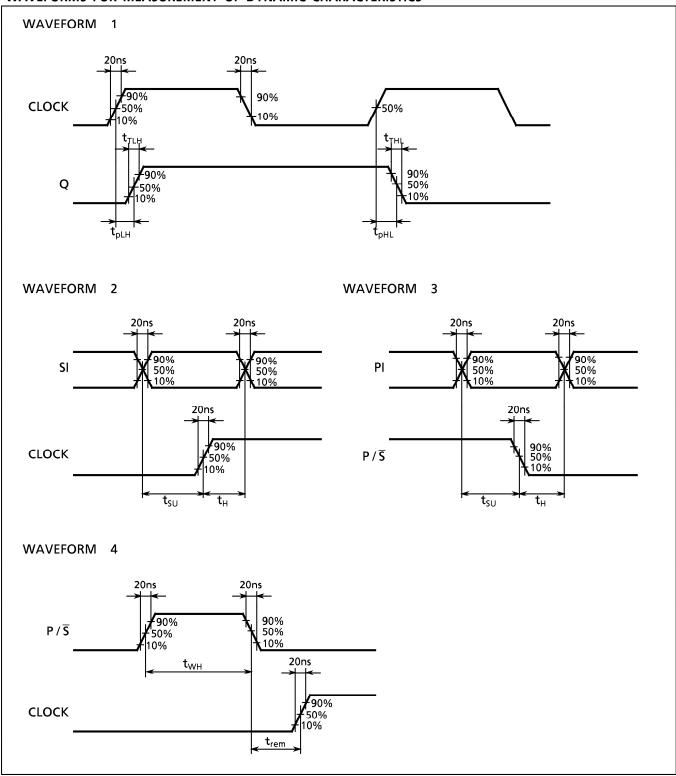
CHARACTERISTIC	SYM-	TEST CONDITION	V_{DD}	– 40°C		25°C			85°C		UNIT
CHARACTERISTIC	BOL	TEST CONDITION	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	OINII
High-Level Output Voltage	V _{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.00 10.00 15.00	_ _ _	4.95 9.95 14.95	-	.,
Low-Level Output Voltage	V _{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15		0.05 0.05 0.05	_ 	0.00 0.00 0.00	0.05 0.05 0.05		0.05 0.05 0.05	V
Output High Current	І _{ОН}	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5 5 10 15	- 0.61 - 2.50 - 1.50 - 4.00	_	- 0.51 - 2.10 - 1.30 - 3.40	- 1.0 - 4.0 - 2.2 - 9.0	_ _ _ _	- 0.42 - 1.70 - 1.10 - 2.80		- mA
Output Low Current	I _{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	0.61 1.50 4.00	_	0.51 1.30 3.40	1.5 3.8 15.0	_ _ _	0.42 1.10 2.80		IIIA
Input High Voltage	V _{IH}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5 10 15	3.5 7.0 11.0	111	3.5 7.0 11.0	2.75 5.50 8.25	l	3.5 7.0 11.0	111	v
Input Low Voltage	V _{IL}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5 10 15		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
Input "H" Leve Current "L" Leve		$V_{IH} = 18V$ $V_{IL} = 0V$	18 18		0.1 -0.1	_	10 ⁻⁵ - 10 ⁻⁵	0.1 -0.1	_	1.0 - 1.0	μΑ
Quiescent Supply Current	I _{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5 10 15	111	5 10 20	_ _ _	0.005 0.010 0.020	5 10 20		150 300 600	μΑ

^{*} All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS ($Ta = 25^{\circ}C$, Vss = 0V, $C_L = 50pF$)

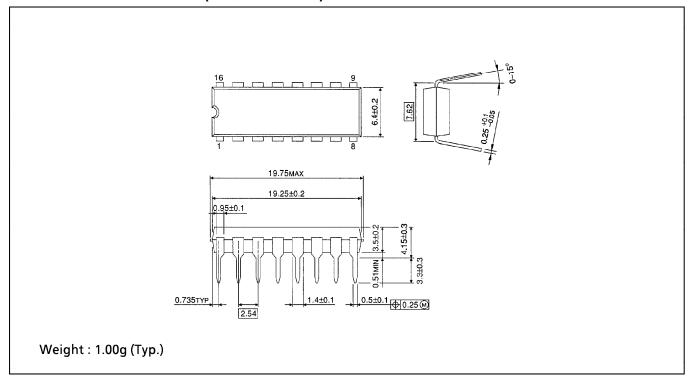
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time			5	_	80	200	
(Low to High)	t _{TLH}		10	_	50	100	
(2011 to 111911)			15	_	40	80	ns
Output Transition Time			5	_	80	200	'''
(High to Low)	t _{THL}		10	_	50	100	
(riigii to Lovv)			15	_	40	80	
Propagation Delay Time	₊		5	_	150	320	
(CLOCK - Q)	t _{pLH}		10	_	65	160	ns
(CLOCK - Q)	t _{pHL}		15	<u> </u>	45	120	
Dranagation Daloy Time			5	_	230	460	
Propagation Delay Time $(P/\overline{S} - Q)$	t _{pLH}		10	_	90	180	ns
(P/3-Q)	t _{pHL}		15	_	60	120	
			5	3.0	6.5	_	
Max. Clock Frequency	f _{CL}		10	6.0	18.0	_	MHz
			15	8.5	24.0	_	
			5	_	80	180	
Min. Clock Pulse Width	t _w		10	_	30	80	ns
			15	_	20	50	
			5	20.0	_	_	
Max. Clock Rise Time	t _{rCL}		10	2.5	<u> </u>	_	μs
Max. Clock Fall Time	t_{fCL}		15	1.0	l —	_	'
NA: 6 . T			5	_	40	120	
Min. Set – up Time	t _{sU}		10	_	20	80	ns
(SI - CLOCK)			15	_	15	60	
			5	_	25	50	
Min. Set – up Time	t _{sU}		10	_	15	30	ns
(PI - P / S)			15		10	20	
Na: 11 1 7:			5	_	35	70	
Min. Hold Time	t _H		10	l <u> </u>	20	40	ns
(SI - CLOCK), (PI - P \overline{S})	"		15	l <u> </u>	15	30	
Min. Pulse Width $(P/\overline{S} - CONTROL)$			5	_	90	180	
	t _{wh}		10	_	30	80	ns
	******		15	_	10	50	
Min. Removal Time (P/ \overline{S} - CLOCK)			5	_	45	280	
	t _{rem}		10	_	20	140	ns
	-iem		15	_	15	100	
Input Capacitance	C _{IN}			_	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



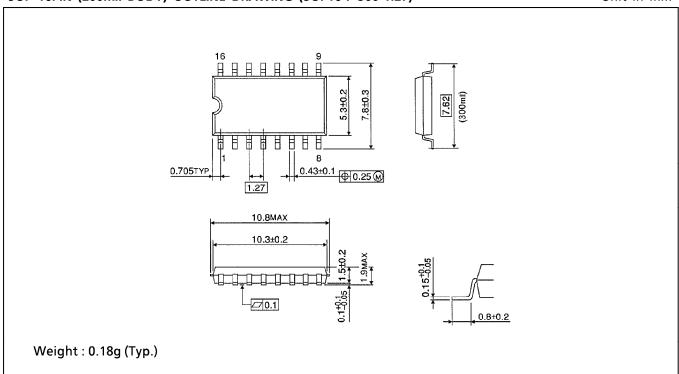
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

