CHECK YOUR PROGRESS 4

11. A flip-flop is basically a
    (a) mono-stable multi-vibrator
    (b) a stable multi-vibrator
    (c) bi-stable multi-vibrator
    (d) none of these.
12. JK flip-flop has the specialty in
    (a) fast response time
    (b) toggle property
    (c) spike shaped clock input
    (d) preset input
13. In MS flip-flop the master changes state
    (a) after the slave
    (b) with the slave at the same time
    (c) before the slave
    (d) never

1.6 COUNTER

A counter is one of the most useful sequential circuits in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulse has a definite time period, the counter can be used to measure time, the time period or frequency.

There are basically two types of counter: ***Synchronous counter*** and ***asynchronous counter***.

Counters are constructed by using flip-flops and other logic gates. If the flip-flops are connected serially then the output of one flip-flop is applied as input to the next flip-flop. Therefore, this type of counter has a cumulative settings time due to propagation delay. Counters of this type are called serial or asynchronous counter. These counters have speed limitation.

Speed can be increased by using parallel or synchronous counter.

Here, flip-flops are triggered by a clock at a time and thus setting time is equal to the propagation delay of a single flip-flop. But this type of synchronous counters require more hardware and hence they are costly.

Combination of serial or parallel counter is also done to get an optimum solution of speed and hardware/cost. If each clock pulse advances the contents of the counter by one, it is called ***up counter***. If the content of the counter goes down at each clock pulse, it is called ***down counter***.

Before operation, some time it is required to reset all the flip-flops to zero. It is called “Clear”. Some time, it is required to set the flip-flops. It is called ***preset***. To do these, two extra inputs are there in every flip-flop called CLR and PR.

1.6.1 Asynchronous Counter

When the output of a flip-flop is used as the clock input for the next flip-flop it is called asynchronous counter.

Asynchronous counters are also called ripple counter because flip-flop transitions ripple through from one flip-flop to the next in a sequence until all flip-flops reach a new state.

A binary ripple counter can be constructed by using clocked JK flip-flop. Fig 1.22(a) shows three MS JK flip-flops connected in series. The clock drives flip-flop A. The output of A drives B and the output of B drives C. J and K inputs of all the flip-flops are connected to positive to make them equal to 1. Under this condition each flip-flop will change state (toggle) with a negative transition at its clock point.

In the counter shown in Fig 1.22 (a), the flip-flop A changes its state at the negative edges of the clock pulses. Its output is applied to the B flip-flop as its clock input.

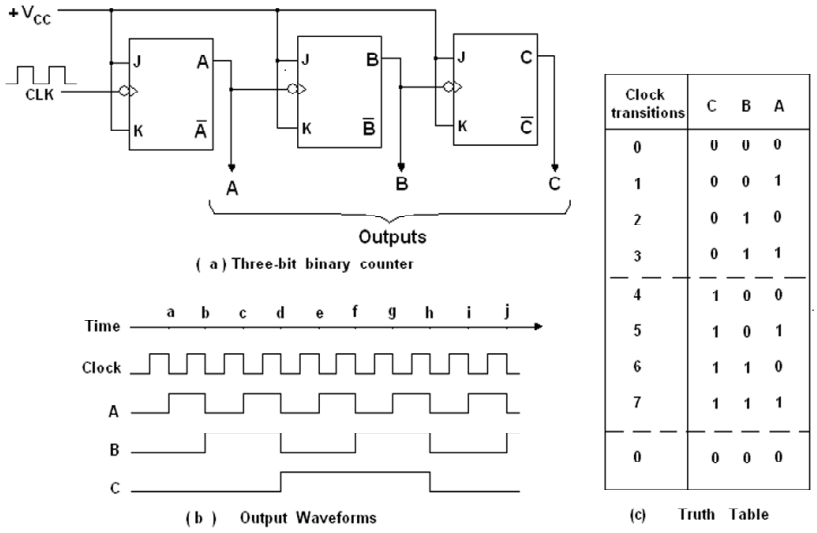


Fig. 1.22 : Three Bit Binary Counter

The output of B flip-flop toggles at the negative edges of the output of A flip-flop. Similarly, the output of B flip-flop is used as clock input of the C flip-flop and therefore C toggles at the negative edges of the output of B flip-flop. We can see that triggering pulses move through the flip-flops like a ripple in water.

The wave form of the ripple counter is shown in fig 1.22(b). It shows the action of the counter as the clock runs. To understand the wave form let us assume that the counter is cleared before the operation. The A output is assumed the list significant bit(LSB) and C is the most-significant-bit (MSB). Hence, at the very beginning the contents of the counter is CBA=000.

Flip-flop A changes its state to 1 after the negative pulse transition. Thus, at point A on the time line , A goes high. At point b it goes low, at C it goes back to high and so on.

Now, output of A acts as clock input of B. So, each time the output of A goes low, flip-flop B will toggle. Thus, at point B on the time line, B goes high at point b and it goes low at point d, and toggles back high again at point f and so on.

Since B acts as the clock input for C, each time the output of B goes low, the C flip-flop toggles. Thus C goes high at point d on the time line, it goes back to low again at point h.

We can see, at the output, wave form of A has half the frequency than the clock input wave. B has half the frequency than that of A and C has half the frequency than that of B.

We can further see that since the counter has 3 flip-flops cascaded together , it progresses through 000---- 001----010---011---100---101---110---111 as its CBA output. After CBA= 111,it starts the cycle again from CBA=000. One cycle from 000---111 takes 8 clock pulses, as it is evident from the wave form as well as from the truth table.

1.6.2 Synchronous Counter

An asynchronous counter or ripple counter has limitation in its operating frequency. Each flip-flop has a delay time which is additive in asynchronous counter.

In synchronous counter the delay of asynchronous counter is overcome by the use of simultaneous applications of clock pulse to all the flip-flops. Hence, in synchronous counter, the common clock pulse triggers all the flip-flops simultaneously and therefore the individual delay of flip-flop does not add together. This feature increases the speed of synchronous counter. The clock pulse applied can be counted by the output of the counter.

To build a synchronous counter, flip-flops and some additional logic gates are required. Fig 1.23 shows a three stage synchronous or parallel binary counter along with its output wave forms and truth table. Here the J and K inputs of each flip-flop is kept high and therefore the flip-flops toggle at the negative clock transition at its clock input. From figure we can see that the output of A is ANDed with CLK to drive the 2nd flip-flop and the outputs of A, B are ANDed with CLK to drive the third flip-flop. This logic configuration is often referred to as “steering logic” since the clock pulses are steered to each individual flip-flop.

In the figure , the clock pulse is directly applied to the first flip-flop. Its J and K are both high, so the first flip-flop toggles state at the negative transition of the input clock pulses. This can be seen at points a,b,c,d,e,f,g,h,i on the time line.

The AND gate X is enabled when A is high, and it allows a clock pulse to reach the 2nd flip-flop. So the 2nd flip-flop toggles with every other negative clock transition at points b, d, f and h on the time line.

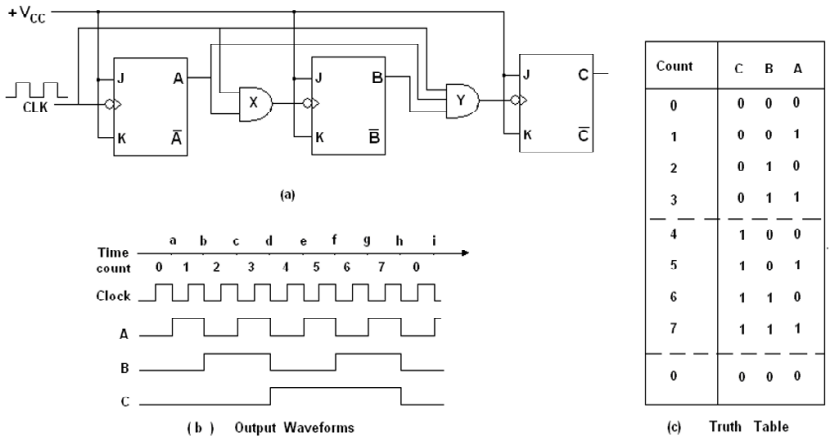


Fig. 1.23 : Parallel Binary Counter

The AND gate Y is enabled only when both A and B are high and it transmits the clock pulses to the clock input of the 3rd flip-flop. The 3rd flip-flop toggles state with every fourth negative clock transition at d and h on the time line.

The wave form and the truth table shows that the synchronous counter progresses upward in a natural binary sequence from 000 to 111. The total count from 000 to 111 is 8 and hence this counter can also be called MOD-8 counter, in count up mode.

CHECK YOUR PROGRESS

14. State *True or False*
    (a) Counters are non sequential digital circuits.
    (b) Asynchronous counters are fast in operation than synchronous counters.
    (c) The natural progression of a counter is called MODE.
    (d) Counters can be used to build digital clock.

1.7 REGISTER

A number of flip-flops connected to store binary number is called a register. The number to be stored is entered or shifted into the register and also taken out or shifted out as per necessity. Hence, registers are also known as shift register.

Registers are used to store data temporarily. Registers can be used to perform some important arithmetic operations like complementation, multiplication, division etc. It can be connected to form counters, to convert serial data to parallel and parallel to serial data.

Types of registers: According to shifting of binary number also called shift registers, different types of registers are:

- Serial In—Serial Out (SISO)
- Serial In –Parallel Out (SIPO)
- Parallel In –Serial Out (PISO)
- Parallel In –Parallel Out (PIPO)

1.7.1 Serial In - Serial Out (SIPO)

Fig 1.24 shows a typical 4 bit SISO register using flip-flops. Here the content of the register is named as QRST. Let us consider that all flip-flops are initially reset. Hence, at the beginning QRST= 0000. Let us consider a binary number 1011 which we want to store in the SISO register.

At time A : A 1 is applied at the D input at the first flip-flop. At the negative edge of the CLK pulse, this 1 is shifted into Q. The O of Q is shifted into R, O of R is shifted into S and O of S is shifted into T. The output of flip-flop just after time A are QRST=1000.

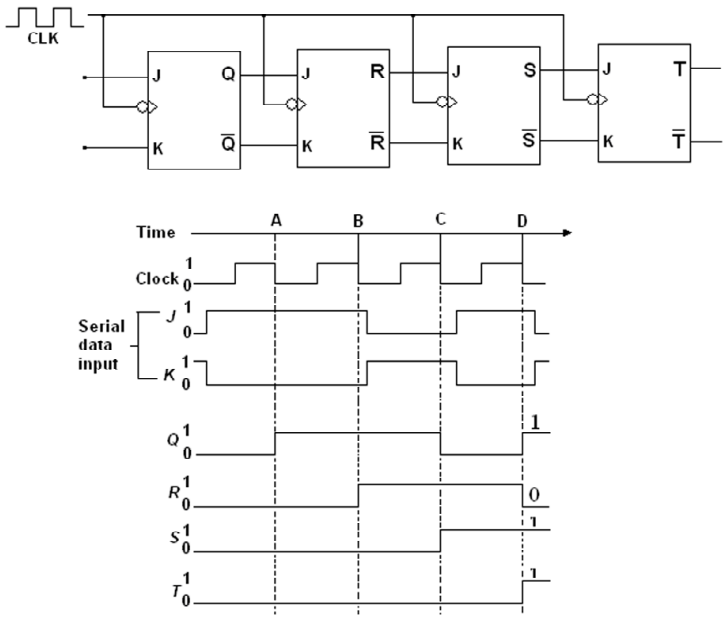


Fig. 1.24 : 4 Bit Serial In-Serial Out Shift Register

At time B: Another 1 is applied in the data input of the first flip-flop. So at the negative CLK edge , this 1 is shifted to Q. The 1 of Q is shifted in R.,O of R shifted in S, O of S is shifted into T. so, at the end of time B the output of all the flip-flops are QRST=1100.

At time C: A O(zero) is applied in the D input of the 1st first flip-flop. At the negative CLK edge , this O shifts to Q. The 1 of Q shifts into R.,1 of R shifts into S, 1 of R shifts into S, O of S shifts into T. Hence the output becomes QRST=0110.

At time D: 1 is applied to D input of the first flip-flop. So this 1 shifts into Q at the negative transmission of CLK. The previous O of Q shifts into R, the 1 of R shifts into S, the 1 of S shifts into T. Hence at the end of time D, the registers contains QRST=1011.

In the above steps, using 4 CLK pulses, we have shifted a 4 bit binary number 1011 in the register in a serial fashion.

To take out this binary number serially, we need another 4 CLK pulses and 4 O inputs into D pin of the first flip-flop. The binary

number leave the register serially through the T pin of the last flip-flop.

1.7.2 Serial In - Parallel Out (SIPO)

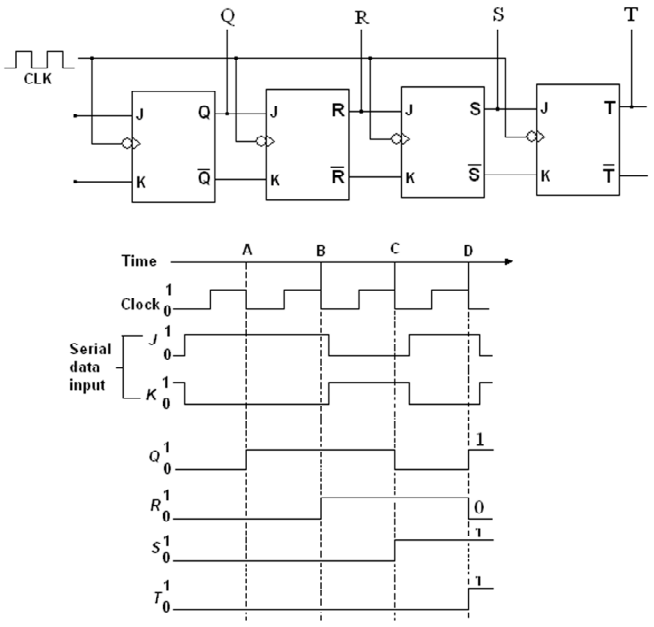


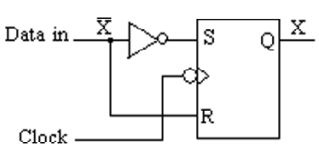
Fig. 1.25 : Bit Serial In - Parallel Out Shift Register

In this type of shifts register, data is entered serially into the register and once data entry completed it can be taken out parallelly. To take the data parallelly, it is simply required to have the output of each flip-flop to an output pin. All other constructional features are same as Serial In—Serial Out (SISO) register.

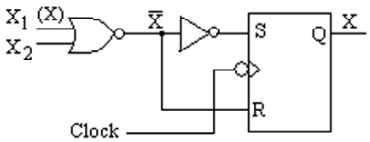
The shifting of data into SIPO is same as SISO registers. In the SIPO of Fig 1.25 , a binary number, say 1011 would be shifted just like the manner as described in the previous section. It would take 4 CLK pulses to complete the shifting. As soon as shifting is completed, the stored binary number becomes available in the output pins QRST. SIPO register is useful to convert serial data into parallel data.

1.7.3 Palallel In-Serial Out (PISO)

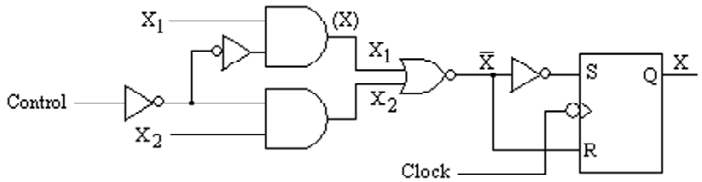
PISO registers take data parallelly and shifts data serially. Commercially available TTL IC for PISO is 54/74166. To understand the functional block diagram of 54/74166 we should first understand the following Fig 1.26(a) is a clocked RS flip-flop, which is converted to a D flip-flop by a NOT gate. The output of the flip-flop is 1 if Data IN ($\overline{X}$) is 0. Next add a NOR gate as in Fig 1.26(b). Here, if X_2 is at ground level, X_1 will be inverted by the NOR gate. As for example, if X_1 =1, then output of the NOR gate will be $\overline{X}$ =0, thereby a 1 will be clocked into the flip-flop. This NOR gate allows entering data from two sources, either from X_1 or X_2. To shift X_1 into the flip-flop, X_2 is kept at ground level and to shift X_2 into the flip-flop, X_1 is kept at ground level.



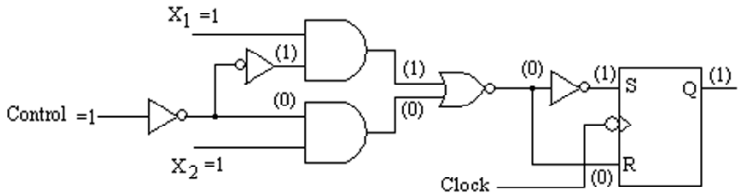
(a) D Type Flip-Flop



(b) D Type Flip-Flop with NOR gate



(c) D Flip-Flop with control logic

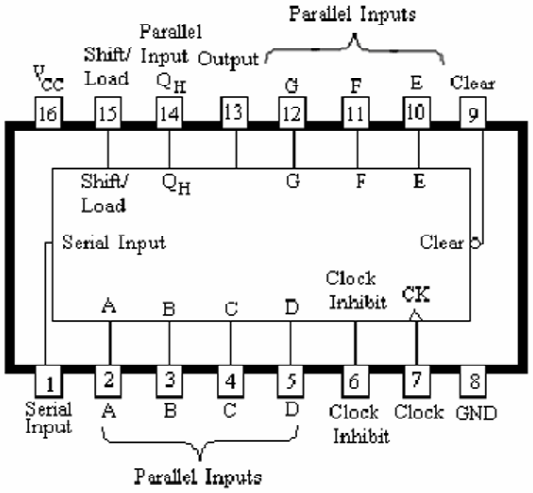


(d) Example of Data Transmision

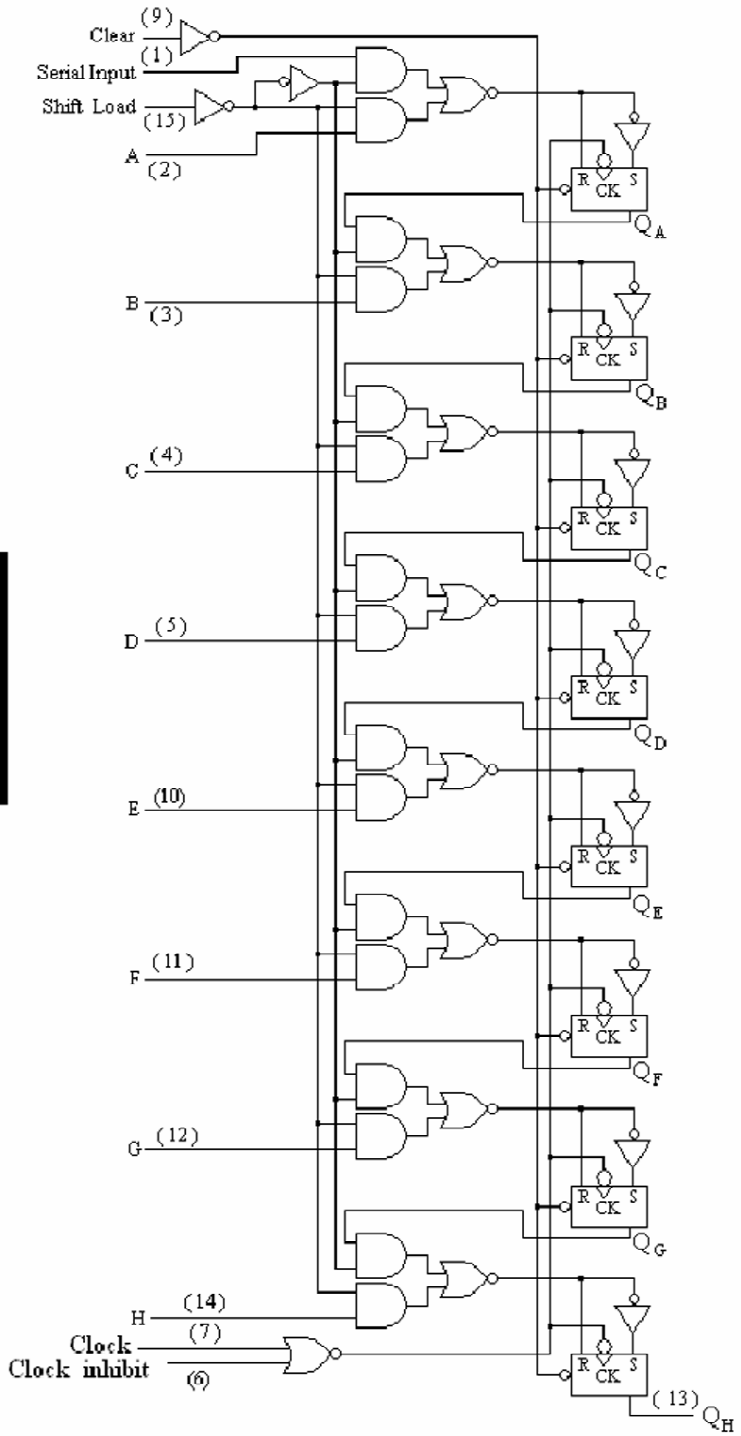
Fig. 1.26 : Building Block of Parallel In-Serial Out Register

Now in Fig 1.26 (c) two AND gates and two NOT gates are added. These will allow the selection of data X_1 or data X_2. If the control line is high, the upper AND gate is enabled and the lower AND gate is disabled. Thus, the data X_1 will enter at the upper leg of the NOR gate and at the same time the lower leg of the

NOR gate is kept at ground. Opposite to this, if the control is low, the upper AND gate is disabled and the lower AND gate is enabled. So X_2 will appear at the lower leg of the NOR gate and during this time the upper leg of the NOR leg gate is kept at ground level.



(a) Pin Out Diagram of Serial In- Parallel out Register



(b) Logic Diagram of Serial In - Parallel Out Register

Fig 1.27 Circuit of 54/74166

If we study Fig 1.27 of PISO we see that circuit of Fig 1.26 (c) is repeated 8 times to form the 54/74/66 shift register. These 8 circuits are connected in such a style that it allows two operations: (1) The parallel data entry and (2) shifting of data serially through the flip-flop Q_A from Q_B toward

If Fig 1.27 the X_2 input of Fig 1.26(c) is taken out from each flip-flop to form 8 inputs named as ABCDEFGH to enter 8 bit data parallelly to the register. The control is named here as SHIFT/LOAD which is kept low to load 8 bit data into the flip-flops with a single clock pulse parallelly. If the SHIFT/LOAD is kept high it will enable the upper AND gate for each flip-flop. If any input is given to this upper AND gate then a clock pulse will shift a data bit from one flip-flop to the next flip-flop. That means data will be shifted serially.

1.7.4 Palallel In - Palallel Out Register (PIPO)

The register of Fig 1.27 can be converted to PIPO register simply by adding an output line from each flip-flop.
The 54/74198 is an 8 bits such PIPO and 54/7459A is a 4 bit PIPO register. Here the basic circuit is same as Fig 1.26(C). The parallel data outputs are simply taken out from the Q sides of each flip-flop. In Fig 1.28 the internal structure of 54/7459A is shown.

When the MODE CONTROL line is high, the data bits ABCD will be loaded into the register parallely at the negative clock pulse. At the same time the output is available $Q_AQ_BQ_CQ_D$. When the MODE CONTROL is low, then the left AND gate of the NOR gate is enabled. Under this situation, data can be entered to the register serially through SERIAL INPUT. In each negative transition, a data bit shifted serially from Q_A to Q_B, from Q_B to Q_c and so on. This operation is called right-shift operation.

With a little modification of the connection, the same circuit can be used for shift-left operation. To operate in shift-left mode, the input data is to be entered through D input pin. It is also necessary

to connect Q_D to C, Q_C to B, Q_B to A as shown in Fig 1.28. MODE CONTROL line is high to enter data through the D input pin and each stored data bits of flip-flops will be shifted to left flip-flop on each negative clock transition. This is serial data and left shift operation.

To clock inputs—clock1 and clock2 is used here to perform shift right and shift left operation..

Hence 54/7495A can be used as Parallel In – Parallel Out shift register as well as shift right and shift left register.

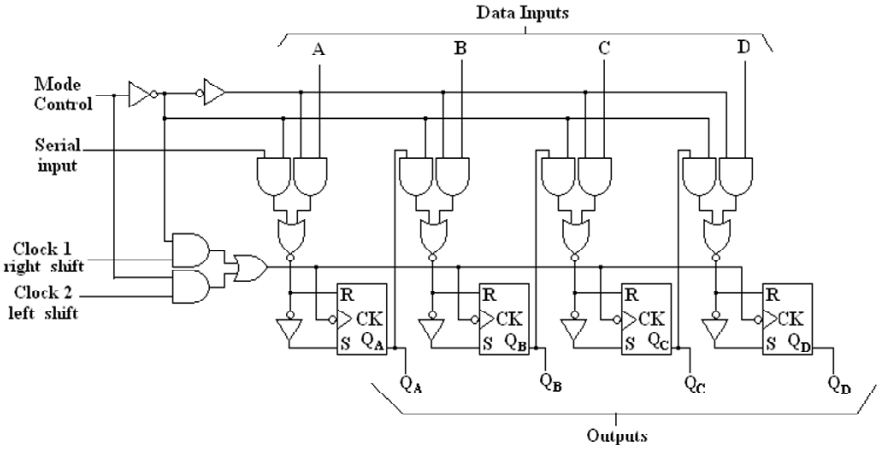


Fig. 1.28 : Parallel In - Parallel Out Shift Register

CHECK YOUR PROGRESS 6

15. Shift registers are
    (a) basically a synchronous circuit
    (b) an asynchronous circuit
    (c) permanent memory
    (d) none of these
16. In SIPO
    (a) data enters parallely and leaves serially
    (b) data enters serially and leaves serially
    (c) data enters serially and leaves parallely
    (d) data enters parallely and leaves parallely

1.8 LET US SUM UP

- Digital circuits are of two categories - combinational and sequential
- A combinational circuit is some combinations of logic gates as per specific relationship between inputs and outputs.
- Adder and subtractor circuits can perform binary addition and subtraction.
- A multiplexer is a combinational circuit which selects one of many inputs.
- Demultiplexer is opposite to a multiplexer.
- An encoder generates a binary code for input variables.
- A decoder decodes an information receives from n input lines and transmits the decoded information to maximum outputs.
- A sequential circuit's output depends on past output and present inputs.
- A flip-flop is basically a single cell of memory which can store either 1 or 0.
- Sequential circuits use flip-flop as their building block.
- There are many types of flip-flop viz RS, D, JK, MS flip-flop.
- A counter is a sequential circuit that can count square waves give as clock input. There are two types of counters- asynchronous and synchronous counter.
- Shift registers are also sequential circuit which are used to store binary bits. They are of four different types - Serial In- Serial Out, Serial In- Parallel Out, Parallel In- Parallel Out and Parallel In-Serial Out register.

1.9 ANSWERS TO CHECK YOUR PROGRESS

1. (b) 2. (c) 3. (a) 4. (b)

5. (c) 6. (d) 7. (b)

8. (a) 9. (b) 10. (b)

11. (c) 12. (b) 13. (c)

14. (a) False (b) False (c) True (d) True

15. (a) 16 (c)

1.10 FURTHER READINGS

1. Mano, M. M., Digital Logic and Computer Design, PHI.
2. Mano, M. M., Computer System Architecture, PHI.
3. Malvino, Albert Paul & Leach, Donald P., Digital Principles and Applications, Mcgraw-Hill International.
4. Lee, Samual C, Digital Circuits and Logic Design, PHI.
5. Talukdar, Dr. Pranhari, Digital Techniques, N. L. Publications.

1.11 MODEL QUESTIONS

1. Distinguish between combinational circuit and sequential circuit.

2. With truth table and logic diagram explain the working of a full-adder circuit.

3. With truth table and logic diagram explain the working of a Full-subtractor circuit.

4. What do you mean by multiplexer ? With diagram explain the working of a 8-to-1 multiplexer.

5. Explain the principle of an encoder. Draw a decimal-to-BCD encoder.

6. What are the differences between asynchronous and synchronous counter ? Draw a MODE-8 counter and explain its working principle.

7. Draw a logic diagram with output wave form of a 4-bit Serial In- Parallel Out shift register for an input of 1101. Explain its operation.

8. Why is square wave clock pulse converted to a narrow spike to be used for flip-flops ? Draw a RC differentiator circuit to convert a square wave into a narrow spike.

9. What is called racing ? To get rid of racing what techniques are used ?

10. What do you mean by magnitude comparator? Draw a block diagram and the function table of the magnitude comparator SN 7485.

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