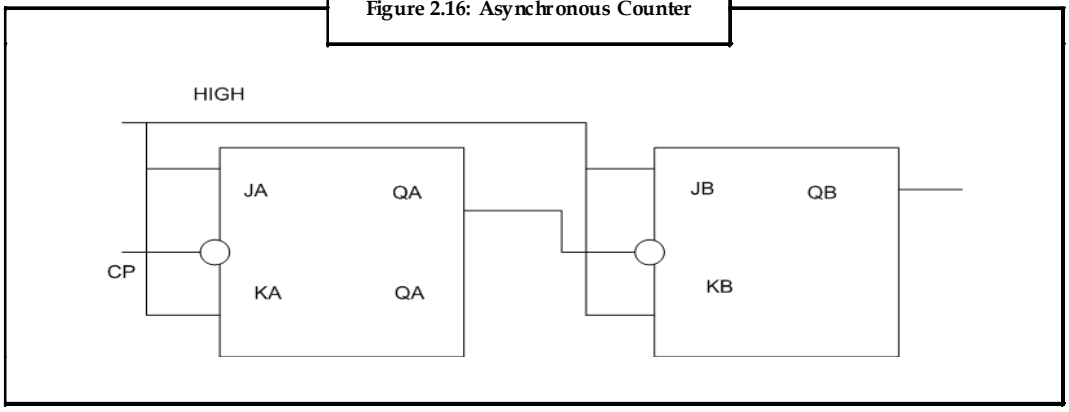
Notes

QA = 1 and QB = 0. After second clock pulse, QA = 0 and QB = 1. After the fourth clock pulse the counter recycles back to its original state.

2.4.2 Asynchronous Counters

An asynchronous counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of the next higher order flip-flop. To obtain a complementing flip-flop a JK flip flop can be used by connecting the J and K inputs together. The figure 2.16 shows a 2-bit asynchronous counter using JK flip-flops.

Figure 2.16: Asynchronous Counter

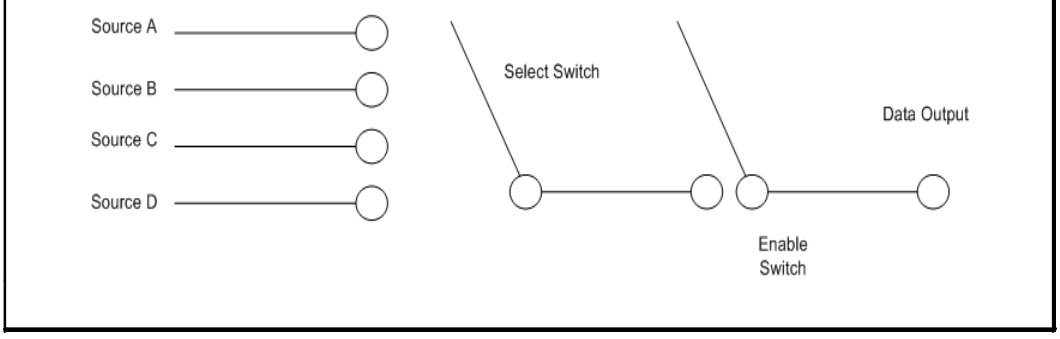


2.5 Multiplexer

A multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. A set of selection lines control the selection of a particular input line. Therefore, a multiplexer is a multiple-input and single-output switch. It provides the digital equivalent of an analog selector switch.

A multiplexer is also called as data selector as it accepts many digital data inputs and selects one of them at any given time to pass onto the output. In some cases, two or more multiplexers are enclosed within an IC package. Figure 2.17 depicts the switching concept of a multiplexer.

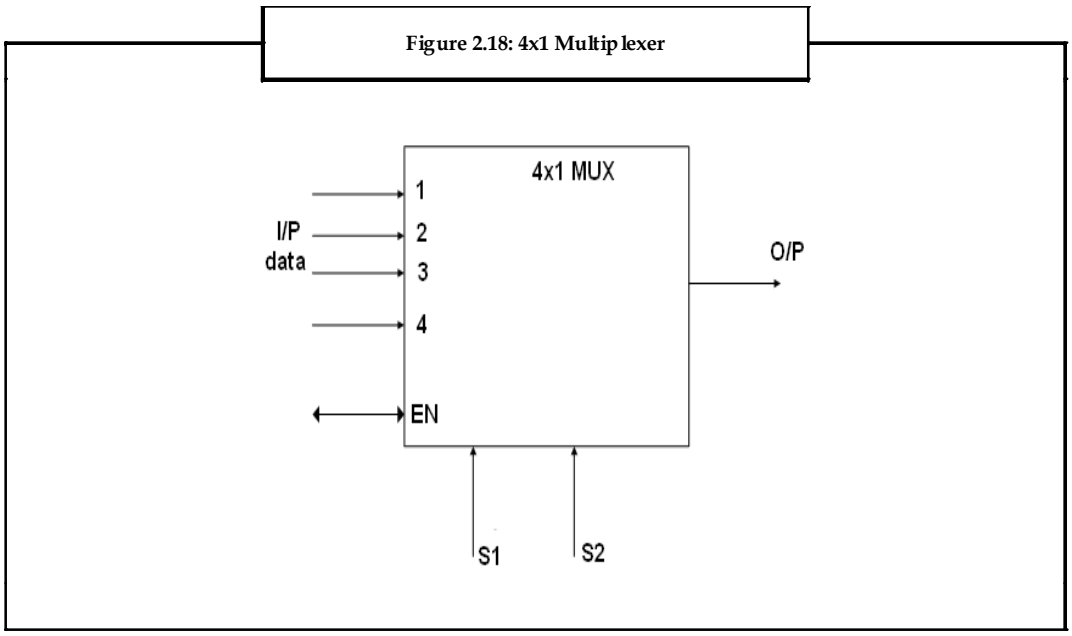
Figure 2.17: Switching Concept of a Multiplexer



Notes

Figure 2.18 depicts a 4 to 1 line multiplexer.

Figure 2.18: 4x1 Multiplexer



The truth table of a multiplexer circuit is shown in table 2.7.

Table 2.7: Truth Table of Multiplexer

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Example: 74xx151 is an 8 to 1 multiplexer which has 8 inputs and two outputs. One of the outputs is an active high output and the other is an active low output. These circuits are used mostly in digital systems of all types, such as data selection, data routing, operation sequencing, parallel-to-serial conversion, waveform generation, and logic-function generation.

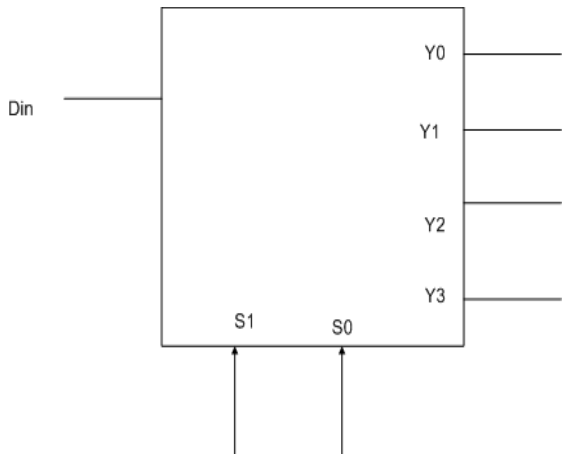
Notes

2.6 Demultiplexer

A circuit that receives information on a single line and transmits the information on any of the 2^n possible output lines is called as a demultiplexer. Therefore, a demultiplexer is called a single-input multiple-output switch. The values of n selection lines control the selection of specific output line.

A demultiplexer is shown in figure 2.19.

Figure 2.19: 1x4 Demultiplexer



The truth table of a demultiplexer circuit is shown in table 2.8.

Table 2.8: Truth Table of Demultiplexer

Enable	S1	S0	Din	Y0	Y1	Y2	Y3
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1

A demultiplexer is used extensively in clock demultiplexer, security monitoring system, synchronous data transmission system, and so on.

2.7 Decoder and Encoder

A decoder is a multiple input, multiple output logic circuit. A decoder converts coded inputs into coded outputs, where the input and output codes are different. Often, the input code has fewer bits than the output code. Each input code word produces a different output code word. The following figure shows the general structure of the decoder circuit which shows that n inputs produce 2^n possible outputs. The 2^n output values are from 0 through 2^{n-1}. Usually, a decoder is provided with enabled inputs to activate decoded output based on data inputs. When any one enabled input is unasserted, all outputs of decoder are disabled.

Notes

2.7.1 Binary Decoder

A binary decoder is a decoder which has an n-bit binary input code and one activated output which is selected from 2^n output codes. This decoder is applicable in instances where it is necessary to activate exactly one of 2^n outputs based on an n-bit input value.

In a 2 to 4 decoder, 2 inputs are decoded into four outputs, each output representing one of the minterms of the 2 input variables. The two inverters provide the complement of the inputs and each one of the four AND gates generate one of the minterms.

The figure 2.20 illustrates the circuit diagram of a 2 to 4 decoder.

Figure 2.20: 2 to 4 Decoder Circuit Diagram

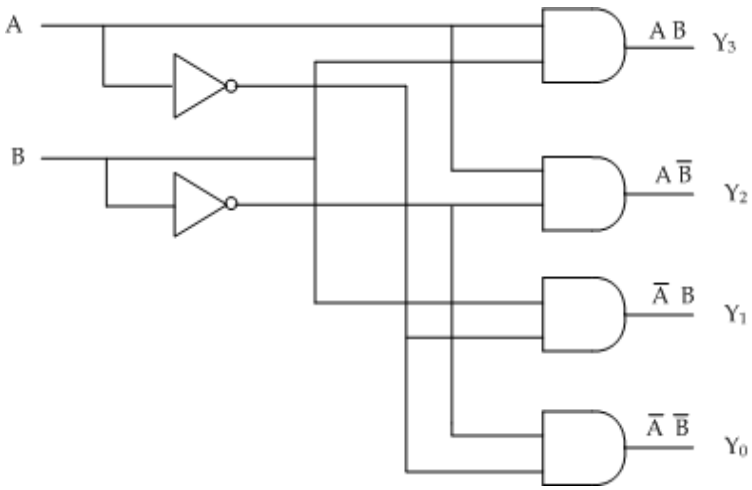


Table 2.9 shows the truth table for a 2 to 4 decoder.

Table 2.9: Truth Table of a 2 to 4 Decoder

Inputs			Outputs			
EN	A	B	Y3	Y2	Y1	Y0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

2.7.2 3 to 8 Decoder

The 74x138 is a 3 to 8 decoder. It accepts three binary inputs, namely A, B, and C and it provides eight individual active low outputs (Y0-Y7) when enabled. The device has three enable inputs, that is, two active low and one active high.

Notes

The figure 2.21 depicts a 3 to 8 decoder.

Figure 2.21: A 3 to 8 Decoder

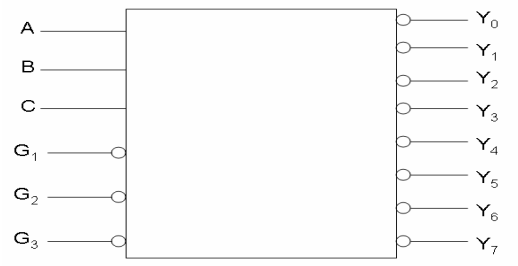


Figure 2.22 depicts the circuit diagram of a 3 to 8 decoder.

Figure 2.22: A 3 to 8 Decoder Circuit Diagram

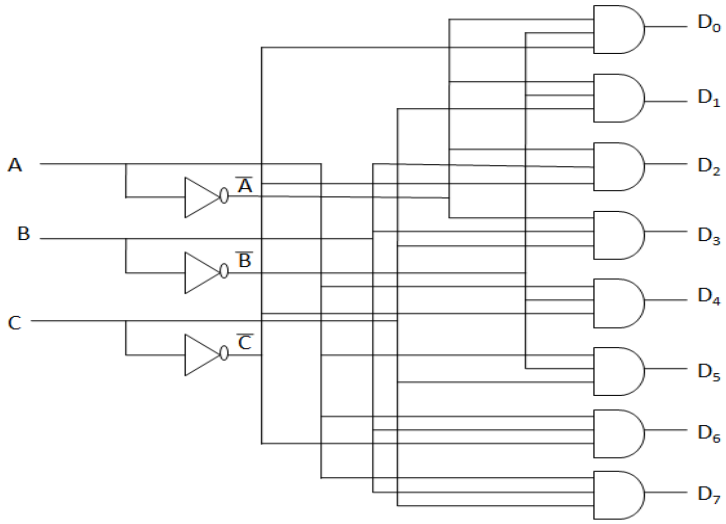


Table 2.10 shows the truth table of a 3 to 8 decoder.

Table 2.10: Truth Table of a 3 to 8 Decoder

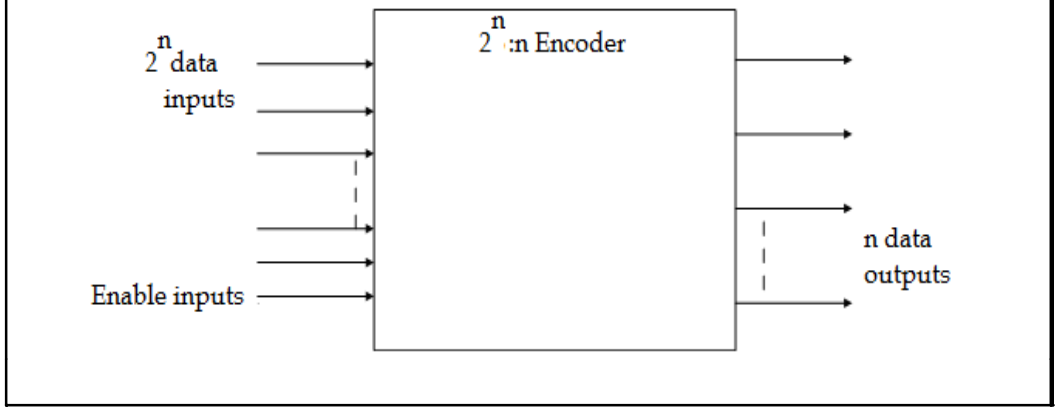
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Notes

2.7.3 Encoder

A digital circuit that performs the inverse operation of a decoder is called as an encoder. It has 2^n input lines and n output lines. In an encoder, the output lines generate the binary code corresponding to the input value. The figure 2.23 depicts the general structure of an encoder circuit.

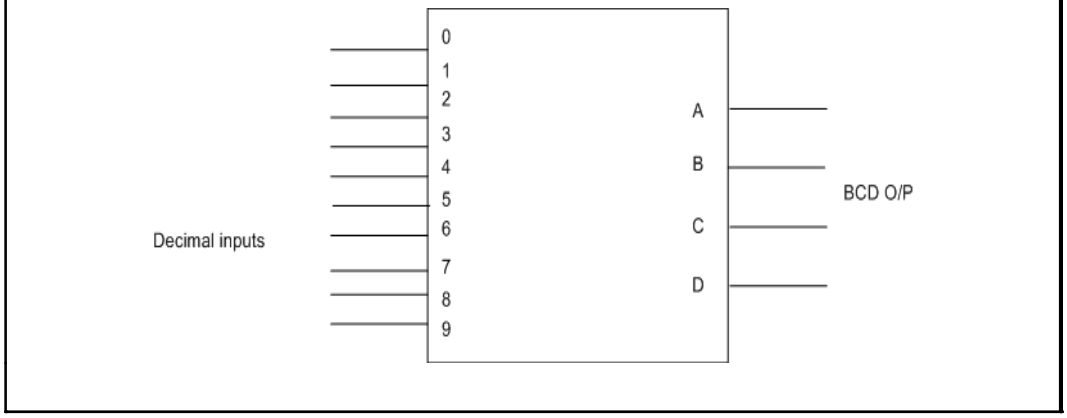
Figure 2.23: An Encoder Circuit



Decimal to BCD Encoder

The decimal to BCD encoder has ten input lines and four output lines. The input for the encoder is the decoded decimal data and encoded BCD is the output available on the four output lines. The figure 2.24 shows the logic symbol for decimal to BCD encoder IC.

Figure 2.24: Decimal to BCD Encoder



Notes

Figure 2.25 depicts the decimal to BCD encoder circuit diagram.

Figure 2.25: Decimal to BCD Encoder Circuit Diagram

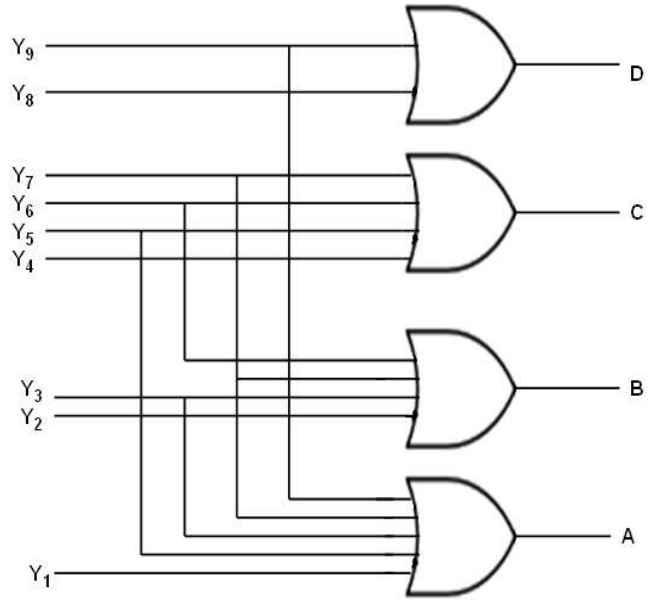


Table 2.11 shows the truth table for a BCD encoder.

Table 2.11: Truth Table of a BCD Encoder

Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	D	C	B	A	BCD
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	0	0	1	0	2
0	0	1	0	0	0	0	0	0	0	0	1	1	3
0	0	0	1	0	0	0	0	0	0	1	0	0	4
0	0	0	0	1	0	0	0	0	0	1	0	1	5
0	0	0	0	0	1	0	0	0	0	1	1	0	6
0	0	0	0	0	0	1	0	0	0	1	1	1	7
0	0	0	0	0	0	0	1	0	1	0	0	0	8
0	0	0	0	0	0	0	0	1	1	0	0	1	9

2.8 Summary

- Binary codes are classified into many forms like weighted codes, reflective codes, sequential codes, alphanumeric codes, and so on.
- There are various logic gates in digital electronics like AND gate, OR gate, NOT gate, NAND gate, NOR gate, and so on which have their own significance.
- The output of latches and flip-flops depends not only on the current inputs but also on previous inputs and outputs.
- The group of flip-flops can be used to store a word which is called a register.

Notes

- A counter is a register which is capable of counting the number of clock pulses arriving at its clock input.
- A multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line.
- A demultiplexer is a circuit that receives information on a single line and transmits the same information on any of the 2^n possible output lines.
- A multiple input, multiple output logic circuit is called as a decoder. It converts coded inputs into coded outputs.
- An encoder has 2^n input lines and n output lines.

2.9 Keywords

Clock Pulse: A circuit in a processor that generates a regular sequence of electronic pulses used to synchronize operations of the electronic system.

Register: An electronic component that offers a known resistance to the flow of electricity.

Switch: A device that directs incoming data from any of multiple input ports to the specific output port.

2.10 Self Assessment

1. State whether the following statements are true or false:
   (a) A decoder has 2^n input lines and n output lines.
   (b) In a 2 to 4 decoder, 2 inputs are decoded into four outputs, each output representing one of the minterms of the 2 input variables.
   (c) A demultiplexer is used extensively in clock multiplexer, security monitoring system, synchronous data transmission system, and so on.
2. Fill in the blanks:
   (a) The decimal to BCD encoder has ten input lines and _____ output lines.
   (b) A multiplexer is also called as _____ as it accepts many digital data inputs and selects one of them at any given time to pass onto the output.
   (c) A counter is a _____ which is capable of counting the number of clock pulses arriving at its clock input.
3. Select a suitable choice for every question:
   (a) Apart from the states of its inputs, the output of _____ is determined by its present output state as well.
      (i) JK flip-flop
      (ii) S-R flip-flop
      (iii) D flip-flop
      (iv) T flip-flop
   (b) _____ is a multiple input, multiple output logic circuit.
      (i) Decoder
      (ii) Encoder
      (iii) Multiplexer
      (iv) Demultiplexer