EELE 475
HARDWARE AND SOFTWARE ENGINEERING
FOR EMBEDDED SYSTEMS

Lab #1
Quartus II Introduction

Assignment Date: 9/01/2015

Due Date: 9/8/2015

Lab Description

Note: Software version numbers will be slightly different. Also note that if you target the DE2 board in the Digital Lab, you will need to use the "University Edition" of Quartus II (version 13.0sp1). Later version don't support the Cyclone II device found on the DE2 board.

Today's lab will introduce you to Altera's Quartus II Software (v15.0). For most of you, this will be a review as you have done this in previous classes such as EELE 367. However, if this is a new version of Quartus for you, it will still be worthwhile going through the tutorial. An important fairly recent change is the method of specifying timing constraints. *It is possible that you have not used the TimeQuest Timing Analyzer to create Synopsys Design Constraints (.sdc files), so pay particular attention to section 6: Specifying Timing Constraints.* The only requirement for this lab is to get the instructor sheet signed off and turned in. You will also need to submit your commented VHDL code to the D2L dropbox site.

Open Quartus II (v15.0) and on the top menu bar go to: *Help→PDF Tutorials→PDF Tutorial for VHDL Users*. The other location where you can find this tutorial is in the Altera Quartus II install directory (e.g. c:/altera/13.0/quartus/common/help/tutorial_quartusii_intro_vhdl.pdf).

Go through the tutorial titled ***Quartus II Introduction for VHDL Users***.

Tutorial Comments & Notes

Here are specific comments that you will want to know about when you read the tutorial.

Section 2.2 : Create your own directory on the lab computer. You can create a directory such as C:\EELE475\your_initials\lab1\ on the lab computer since running the design locally will be *much faster* than running it using your Z or flash drive when it comes to compile times.

Section 2.4 : You can select the Stratix III device as the tutorial says since we won't be downloading and targeting a FPGA board (The DE2 board has a cyclone II part, the Helio View board has a cyclone V).

Section 3, Figure 12 (and in entity): The code addersubtractor.vhd can be found on the D2L site. Notice that the output signal Z is defined as a buffer type. Buffer types are not commonly used in VHDL designs because they can cause problems during synthesis. To reduce the amount of buffer coding in hierarchical designs, create an internal signal and declare port Z as an out type.
(See http://www.velocityreviews.com/forums/t23330-buffer-mode-ports.html)

Section 4.1.1 (Under Errors Section) **:** The line is ~66 instead of line 47 if you downloaded the file from D2L.

Your Lab #1 Assignment:

Change the signal type in section 3 from *buffer* to *out* and recompile (without any compiler errors).

Deliverables

- No lab report this week
- Hand in the Instructor Verification Sheet
- Upload to D2L:
    - Your VHDL code you modified.
    - The .sdc file you created.

Instructor Verification Sheet
Turn in this page in to get credit for Lab #1

Lab #1
Quartus II Introduction Using VHDL Design

EELE 475
HARDWARE AND SOFTWARE ENGINEERING
FOR EMBEDDED SYSTEMS

Name : _____

Sign-off #1 : The signal Z in the addersubtractor has been changed from the *buffer* type to an *out* type and the file can be compiled with no errors.

Verified: _____ Date:_____