DB08
Binary Adder-Subtracter

Product Tutorial

Ver.1.1

Designed & Manufactured in India by-
An ISO 9001:2008 company
Scientech Technologies Pvt. Ltd.
94, Electronic Complex, Pardesipura, Indore - 452 010 India,
+ 91-731 4211100, : info@scientech.bz , : www.ScientechWorld.com

Binary Adder-Subtracter
DB08

Table of Contents

Introduction

DB08 is a compact, ready to use **Binary Adder-Subtracter** experiment board. This experiment board has been designed to study binary adder and Subtracter circuits. It can be used as stand alone unit with external Power Supply or can be used with **Scientech Digital Lab Scientech 2611** which has built in Power Supply, Pulse Generator, Pulser Switches, 8 bits data switches, logic probe, digital display, 8 bits LED display.

List of boards:

Model	Name
DB01	Logic Gates
DB02	Universal Gate- NAND/NOR
DB03	EX-OR Gate Implementation
DB04	Demorgan's Theorem
DB05	EX-OR Gate Application
DB06	Code Conversion (Binary to Gray & Gray to Binary)
DB07	Code Conversion (BCD to Excess-3 code)
DB09	Encoder – Decoder
DB10	Multiplexer – Demultiplexer
DB11	Flip-Flops (R-S, D, J-K, T)
DB12	Shift Register (4 bit SIPO)
DB13	4 Bit Synchronous Binary Counter
DB16	Digital to Analog Converter (R-2R ladder)
DB15	BCD to 7- Segment Decoder
DB17	Event Counter
DB21	Fiber Optic Digital Link
DB22	Analog to digital converter (Counter Type)
DB27	Digital to Analog Converter (R-2R ladder)
DB28	Monostable Multivibrator
DB29	CMOS and Crystal Oscillator
DB31	Decoder/Demultiplexer
DB32	Modulo-N programmable counter
DB35	4 BIT Shift Register

………and many more

Theory

Half Adder:

The combinational circuit that performs the addition of two bits is called a Half Adder. This circuit has two binary inputs and two binary outputs. The input variable X, Y designate the augends and addend bits, the output variables S_h, C_h produces the sum and carry. The logic diagram and Truth Table are shown in experiment section. The Boolean equation is

$$S_h = X'.Y + X.Y' = X \oplus Y$$

$$C_h = X.Y$$

Full Adder:

The circuit that performs the addition of three bits (two significant bits and a previous carry) is called a full adder. It consists of three inputs X, Y, Z. Two of the input variable, denoted by X and Y, represents the two significant bits to be added. The third input, Z, represents the carry from the previous lower significant position. The output S_f gives the value of the least significant bit of sum and C_f gives the output carry. The logic diagram for 3-bit full adder is shown in experiment section. The Boolean equation is

$$S_f = X'Y'Z + X'YZ' + XY'Z' + XYZ$$

$$C_f = X.Y + X.Z + Y.Z$$

The full adder introduced above forms the sum of two bits and a previous carry. Two binary number of n bits each can be added in parallel by means of binary parallel adder. Consider two 2 bit numbers Y0 X0, Y1 X1

$$\begin{array}{rcr} \text{Y0 X0} & & \text{Y0 X0} \\ + \underline{\text{Y1 X1}} & = & \underline{\text{Y1 X1}} \\ \text{SUM} & & \text{C0 S1 S0} \end{array}$$

It can also be constructed with two full adder in cascade, with the output carry from one full adder connected to the input carry of the next full adder. An n bit parallel adder requires n full adder. The Truth Table and logic diagram for 2 bit binary parallel adder is shown in experiment section.

Half Subtracter:

A Half Subtracter is a combinational circuit that subtracts two bits and produces their difference. It has two inputs X, Y. X is minuend and Y is subtrahend. The output bits are designated by B_h, D_h. D_h is difference bit and B_h is borrow bit (generates the binary signal that informs the next stage that a 1 has been borrowed). The logic diagram and Truth Table for 2 bit Half Subtracter is shown in experiment section.

The Logic equation is

DB08

$$D_h = X'Y + XY' = X \oplus Y$$

$$B_h = \overline{X}.Y$$

DB08

Experiment

Objective:

Verification of Truth Table for the following Digital Circuits

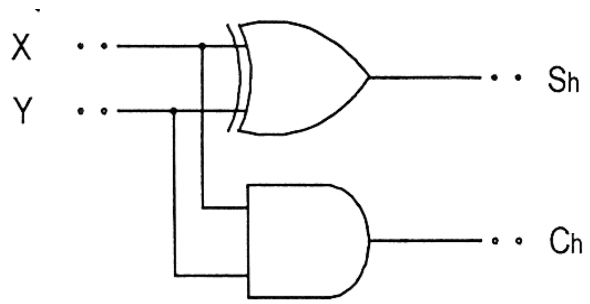
1. 2 Bit Binary Half Adder.
2. 3 Bit Binary Full Adder.
3. 2 Bit Binary Parallel Adder.
4. 2 Bit Binary Half Subtracter.

Equipment Needed:

1. Digital board **DB08**
2. DC Power Supply +5 V from external source or **ST2611 Digital lab.**
3. Digital Multimeter or **Digital Lab ST2611**.

Logic Diagram & Truth Table:

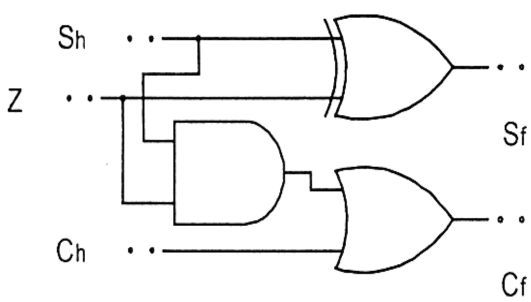
(Logic 1 = +5 V & Logic 0=GND)



2 Bit Binary Half Adder

X	Y	Ch	Sh
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Figure 1

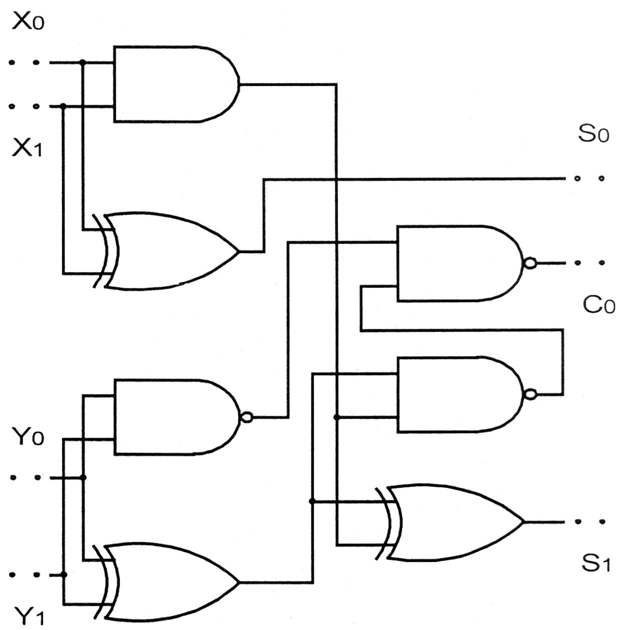


3 Bit Binary Half Adder

X	Y	Z	Cf	Sf
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 2

DB08



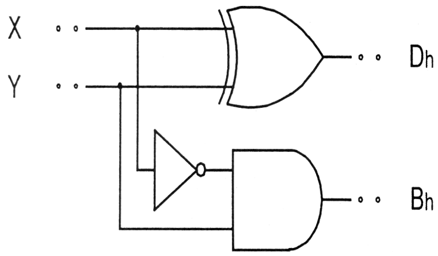
2 Bit Binary Parallel Adder

Figure 3

Y0	X0	Y1	X1	C0	S1	S0
0	0	0	1	0	0	1
0	1	0	1	0	1	0
0	1	1	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	1

Truth Table

DB08



X	Y	Bh	Dh
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

2 Bit Binary Half Subtracter

Figure 4

Procedure:

1. Connect +5 V and ground to their indicated position on **DB08** from external DC Power Supply or from DC power block of **Digital Lab ST -2611.**

2. Switch on the Power Supply.

3. Connect inputs X, Y as per Truth Table to 2 bit binary Half Adder.

4. Observe output S_h, C_h on multimeter or on LED display of **Digital Lab ST2611** and prove Truth Table.

5. Switch Off the Power Supply.

6. Connect output Sh, CH of 2 bit binary Half Adder to input Sh, Ch of 3 bit binary Full Adder.

7. Connect input X, Y, Z to 3 bit binary Full Adder as per Truth Table shown.

8. Observe output S_f, C_f on multimeter or on LED display of **Digital Lab ST2611** and prove Truth Table.

9. Repeat above steps and prove Truth Table for 2 bit binary parallel Adder and 2 bit binary Half Subtracter.

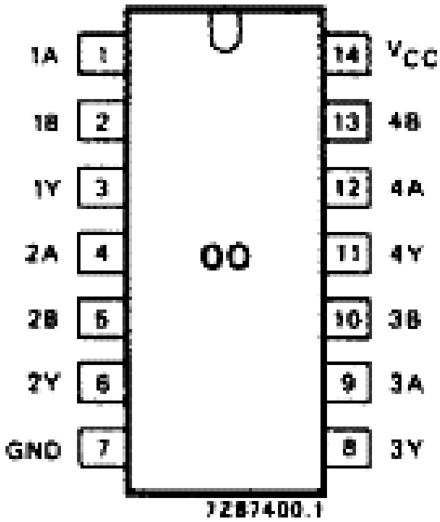
Quad 2-input NAND gate	74HC/HCT00

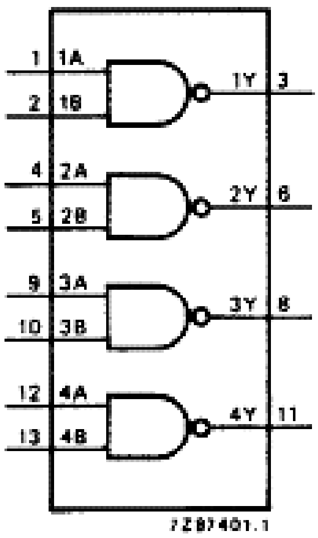
Pinout diagrams: (Pin 14 = Vcc = +5 V)

General Description:

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard number 7A.

The 74HC/HCT00 provide the 2-input NAND function.





DB08

FUNCTION TABLE

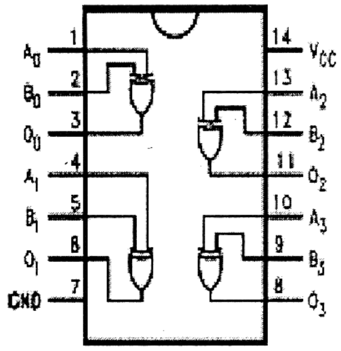
INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level

Quad 2- Input Exclusive-OR **Gate 54LS/74S136**

Pinout Diagram: (Pin 14 = Vcc = + 5 V)



H = High voltage level
L = Low voltage level

Function Table

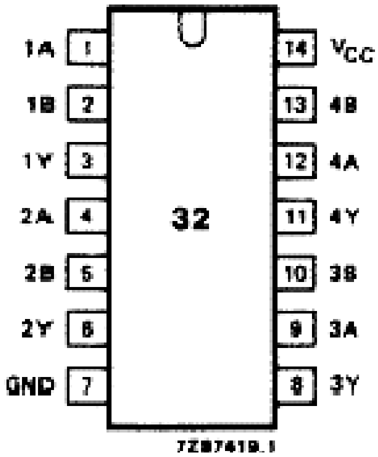
INPUTS		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

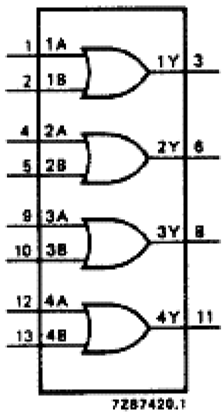
Quad 2-input OR gate 74HC/HCT32

General Description:

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard number 7A.

The 74HC/HCT32 provide the 2-input OR function.





FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

Notes

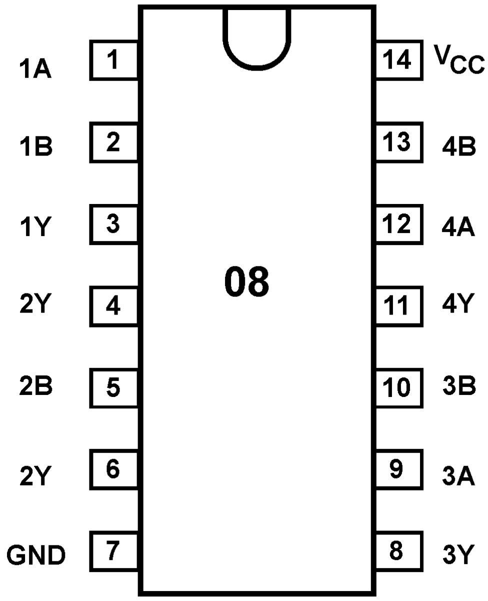
1. H = HIGH voltage level
   L = LOW voltage level

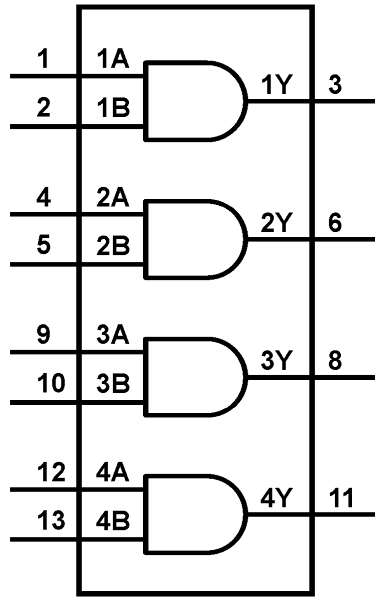
Quad 2-input AND gate 74HC/HCT08

General Description:

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard number 7A.

The 74HC/HCT08 provide the 2-input AND function.





FUNCTION TABLE

INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	L
L	H	L
H	L	L
H	H	H

Note

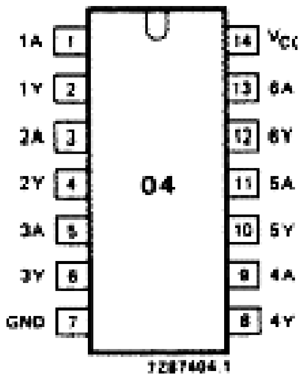
1. H = HIGH voltage level
   L = LOW voltage level

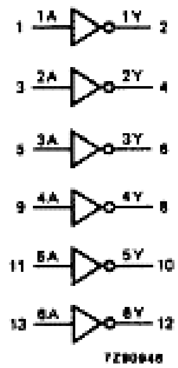
Hex inverter 74HC/HCT04

General Description:

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard number 7A.

The 74HC/HCT04 provides six inverting buffers.





FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level

Note: Pull up resistance of 1 K is required in open collector ICs to get output

Warranty

1. We guarantee this product against all manufacturing defects for **12 months** from the date of sale by us or through our dealers.
2. The guarantee will become void, if
   a. The product is not operated as per the instruction given in the Learning Material.
   b. The agreed payment terms and other conditions of sale are not followed.
   c. The customer resells the instrument to another party.
   d. Any attempt is made to service and modify the instrument.
3. The non-working of the product is to be communicated to us immediately giving full details of the complaints and defects noticed specifically mentioning the type, serial number of the product and date of purchase etc.
4. The repair work will be carried out, provided the product is dispatched securely packed and insured. The transportation charges shall be borne by the customer.

Hope you enjoyed the Scientech Experience.

List of Accessories

1. 2 mm Patch Cord (Red) 16” .... 1 No.
2. 2 mm Patch Cord (Black) 16”... 1 No.
3. 2 mm Patch Cord (Blue) 16” .... 7 Nos.