DB11
Flip-Flops

Product Tutorial

Ver.1.1

Designed & Manufactured in India by:
An ISO 9001:2008 company
Scientech Technologies Pvt. Ltd.
94, Electronic Complex, Pardesipura, Indore - 452 010 India,
✆ + 91-731 4211100, ✉: info@scientech.bz , : www.ScientechWorld.com

DB11
Flip-Flops

Table of Contents

DB11

Introduction

DB11 is a compact, ready to use **Flip-Flops** experiment board. All Flip-flops are incorporated on a single board for verification of their Truth Table and comparison. This experiment board has been designed to study R-S, J-K, D, T flip-flops. It can be used as stand alone unit with external Power Supply or can be used with **Scientech Digital Lab Scientech 2611** which has built in Power Supply, Pulse Generator, Pulser Switches, 8 Bits Data Switches, Logic Probe, Digital Display, 8 bits LED display.

List of boards:

Model	Name
DB01	Logic Gates
DB02	Universal Gate- NAND/NOR
DB03	EX-OR Gate Implementation
DB04	Demorgan's Theorem
DB05	EX-OR Gate Application
DB06	Code Conversion (Binary to Gray & Gray to Binary)
DB07	Demorgan's Theorem
DB08	Binary Adder -Subtractor
DB09	Encoder – Decoder
DB10	Multiplexer – Demultiplexer
DB12	Shift register (4 bit SIPO)
DB13	4 Bit Synchronous Binary Counter
DB16	Digital to Analog Converter (R-2R ladder)
DB15	BCD to 7- Segment Decoder
DB17	Event Counter
DB21	Fiber Optic Digital Link
DB22	Analog to digital converter (Counter Type)
DB27	Digital to Analog Converter (R-2R ladder)
DB28	Monostable Multivibrator
DB29	CMOS and Crystal Oscillator
DB30	Adder/ Subtracter (4-Bit/8-Bit)
DB31	Decoder/Demultiplexer
DB32	Modulo-N programmable counter
DB35	4 BIT Shift Register

……and many more

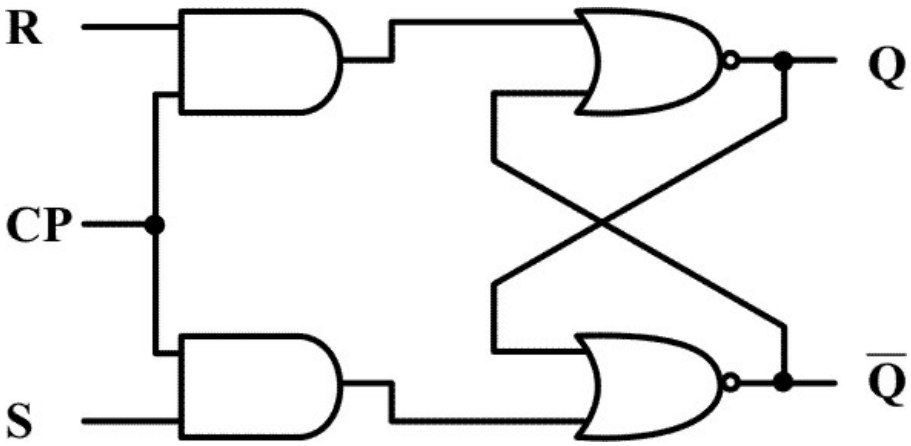
Theory

Flip-flops are binary cells capable of storing one bit of information. A Flip-flop has two outputs, one for the normal value and one for complement value of the bit stored in it. A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

Clocked RS Flip-flop:

Clocked RS Flip-flop shown in figure 1 consists of two NOR Gates and two AND Gates. The input S and R are set and reset input and output Q and Q' are normal and complement output. The input CP is input for giving clock pulse. Flip-flop will change state only when CP goes from 0 to 1.

The output of two AND Gates remain at 0 as long as the clock pulse CP is 0, regardless of the S and R input values. When the clock pulse goes to logic high level i.e. 1, information from the S and R is allowed to reach the basic flip-flop. The set state is reached with S = 1, R = 0, and CP = 1. (for set state, Q = 1 and for reset state, Q = O) To change to the clear state, the inputs must be S = 0, R = 1, CP = 1. With both S = 1 and R = 1, the occurrence of a clock pulse causes both outputs to momentarily go to 0. When the pulse is removed, the state of flip-flop is indeterminate, i.e., either state may result, depending on whether the set or the reset input of the basic flip-flop remains a 1 longer before the transition to 0 at the end of the pulse. The characteristics table is shown in experiment section along with logic diagram.



R-S Flip-flop

Figure 1

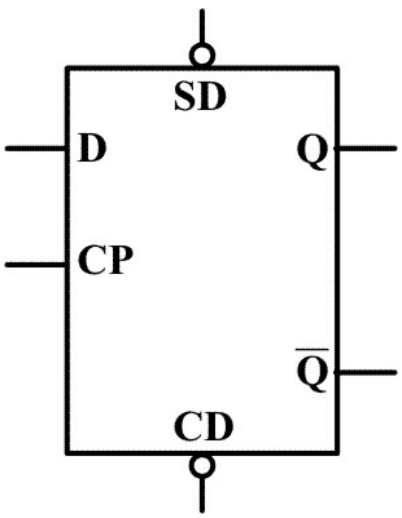
(Q=Present State, Q (t+1) = Next state)

Truth Table for R-S Flip-flop

CP Transition	Q	S	R	Q (t +1)
0 →1	0	0	0	0
0 →1	0	0	1	0
0 →1	0	1	0	1
0 →1	0	1	1	Indeterminate
0 →1	1	0	0	1
0 →1	1	0	1	0
0 →1	1	1	0	1
0 →1	1	1	1	Indeterminate

D Flip-flop:

The logic symbol and characteristics table for D flip-flop is shown in figure 2. It has only one data input (D) and clock input (CP). The outputs are labeled Q and Q'. The data (0 or 1) at the input 0 is delayed one clock pulse from getting to output Q. SD and CD are active low input (Negative edge trigger) to set and reset the flip-flop i.e these inputs will be effective when logic 0 is applied. A D Flipflop is a bistable circuit whose 0 input is transferred to the output after a clock pulse is received.



CP Transition	Q	D	Q(t + 1)
1→ 0	0	0	0
1→ 0	0	1	1
1→ 0	1	0	0
1→ 0	1	1	1

D Flip-flop

Figure 2

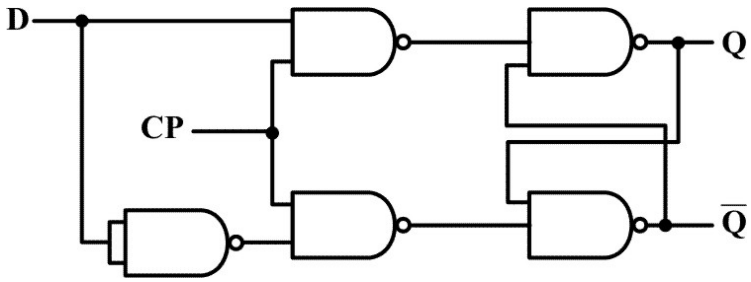


Figure 3

As long as the clock input is at 0, Gates 3, 4 have a 1 in their outputs, regardless of the value of the other inputs. The D input is sampled during the occurrence of a clock pulse (CP=1). If it is 1, the output of Gate 3 goes to 0, switching the flip-flop to the set state (unless it was already set). If it is a 0 the output of Gate 4 goes to 0, switching the flip-flop to the clear state.

J-K Flip-flop:

A J-K flip-flop is refinement of R-S flip-flop in that the indeterminate state of the RS type is defined in the JK type. Inputs J, K is used to set and clear the flip-flop. When both J, K are high simultaneously, the flip-flop switches to its complement state, that is, if Q = 1, it switches to Q= 0, and vice versa. A CP signal which remains a 1 (While J=K = 1) after the outputs have been complemented once will cause repeated and continuous transitions of the output. To avoid this undesirable operation, the clock pulse must have a time duration which is shorter than the propagation through the flip-flop.

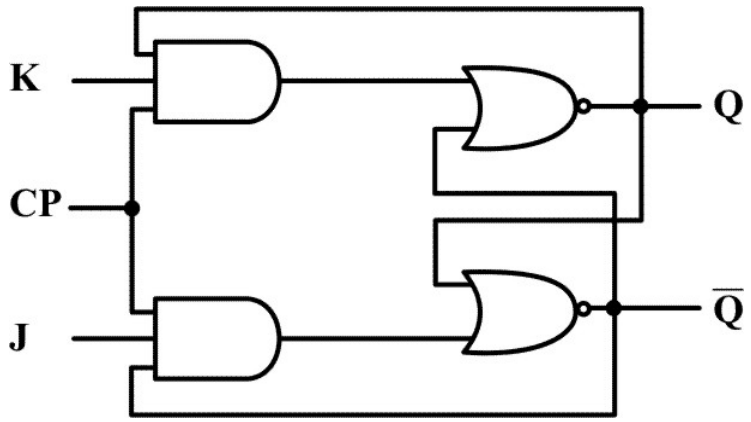
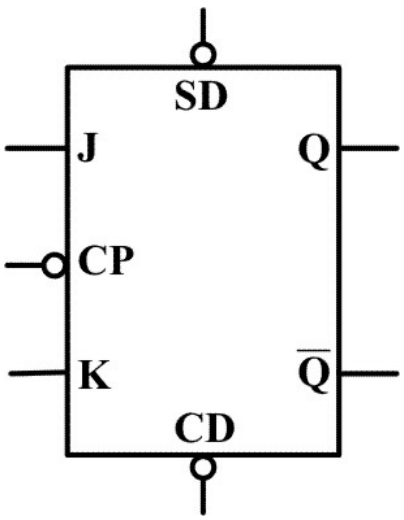


Figure 4

The JK flip-flop shown above behaves like an R-S flip-flop, except when both J and K are 1, the clock pulse is transmitted through one AND Gates only- the one whose input is connected to the flip-flop output which is presently 1. Thus, if Q = 1, the output of the upper AND Gate become 1 upon application of a clock pulse, and the flip-flop is cleared. If Q = 0, the output of lower AND Gate becomes a 1 and the flip-flop is set. In either case, the output state of the flip-flop is complemented.



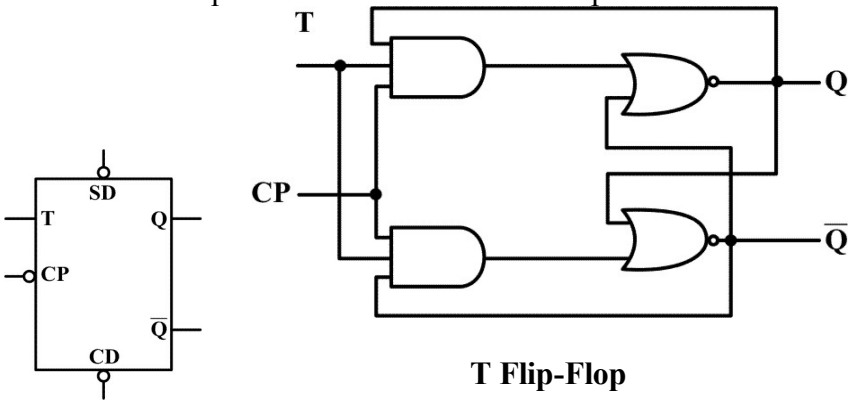
CP Transition	Q	J	K	Q (t +1)
1→ 0	0	0	0	0
1→ 0	0	0	1	0
1→ 0	0	1	0	1
1→ 0	0	1	1	1
1→ 0	1	0	0	1
1→ 0	1	0	1	0
1→ 0	1	1	0	1
1→ 0	1	1	1	0

J-K Flip-flop

Figure 5

T Flip-flop:

The flip-flop is a single input version of the JK flip-flop .As shown below; the T flip-flop is obtained from a JK type if both inputs are tied together. The designation T shows ability of flip-flop to toggle. Regardless of the present state of the flip-flop, it assumes the complement state when the clock pulse occurs while input T is logic1



T Flip-Flop

Figure 6

CP Transition	Q	T	Q(t +1)
1→ 0	0	0	0
1→ 0	0	1	1
1→ 0	1	0	1
1→ 0	1	1	0

DB11

Experiment

Objective:

To study following Flip-flops and prove Truth Tables

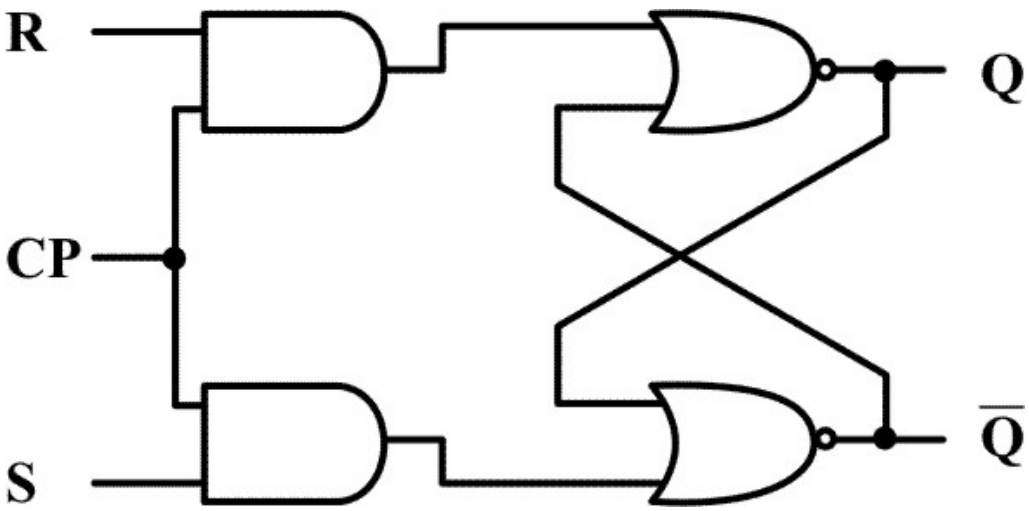
1. R-S
2. D
3. J-K
4. T

Equipments Needed:

1. Digital board, **DB11**
2. DC Power Supply +5 V
3. Digital Multimeter or **Digital Lab Scientech 2611**.
4. TTL Clock Generator of 2 KHz

Logic diagram & Truth Table:

(Logic 1 = +5V & Logic 0= GND)



R-S Flip-flop

Figure 7

DB11

(Q=Present State, Q (t+1) = Next state)

CP Transition	Q	S	R	Q (t +1)
0 →1	0	0	0	0
0 →1	0	0	1	0
0 →1	0	1	0	1
0 →1	0	1	1	Indeterminate
0 →1	1	0	0	1
0 →1	1	0	1	0
0 →1	1	1	0	1
0 →1	1	1	1	Indeterminate

Truth Table for R-S Flip-flop

Procedure:

1. Connect +5V and ground to their indicated position on **DB11** experiment board from external DC power supply or from DC power block of **Digital Lab Scientech 2611**.
2. Switch on the power supply.
3. Connect inputs 0, 0, 0 to S, R, CP pins of R-S flip-flop.
4. Measure output Q (Present state).
5. Connect input 1 to CP.
6. Measure output Q. It is next state Q (t + l) for input 0, 0.
7. Repeat above steps for remaining inputs. (Before transition of clock pulse from 0 to 1, output is present state and after transition output is next state)
8. Connect 1, 0 to pins SD and CD of D flip-flop to clear the output Q.
9. Connect 1, 1 to pins SD and CD of D flip-flop.
10. Connect inputs as per Truth Table for D flip-flop and prove Truth Table.
11. Connect output Q to Input D of D Flip-flop.
12. Connect a TIL clock pulse of 2 KHz to CP input.
13. Observe output Q on Osci1loscope. It win be 1 KHz.
14. Connect 1, 0 to pins SD and CD of JK flip-flop to clear the Output Q.
15. Connect inputs as per Truth Table of JK Flip Flop and prove it.
16. Connect input 1, 1 to J, K pins of JK flip-flop and 1, 1 to SD, CD.
17. Connect a TIL clock pulse of 2 KHz to CP input.
18. Observe output Q on Oscilloscope. It will be 1 KHz.
19. Repeat above steps to prove Truth Table for T flip-flop.

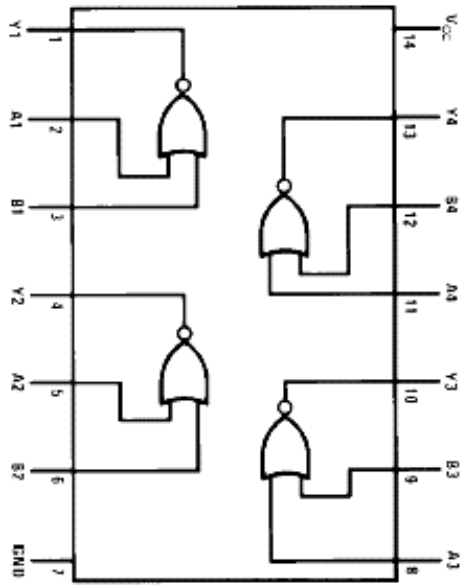
Result:

Indeterminate state of RS flip-flop is determined in JK Flip-flop but problem of toggling occurs which is useful for making divide by 2 circuit.

Data Sheet

Quad 2- Input NOR Gate — DM7402

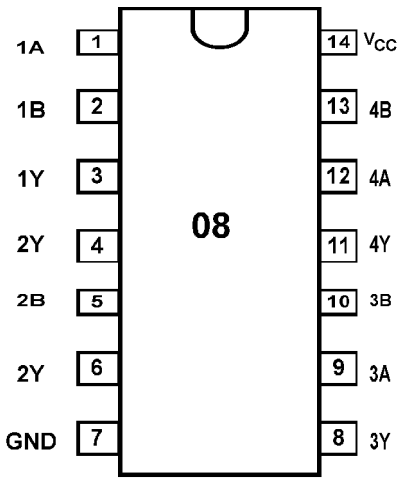
Pinout Diagram (Pin 14 = Vcc= + 5 V)



Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

Function Table

Quad 2-input AND gate — 74HC/HCT08



INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

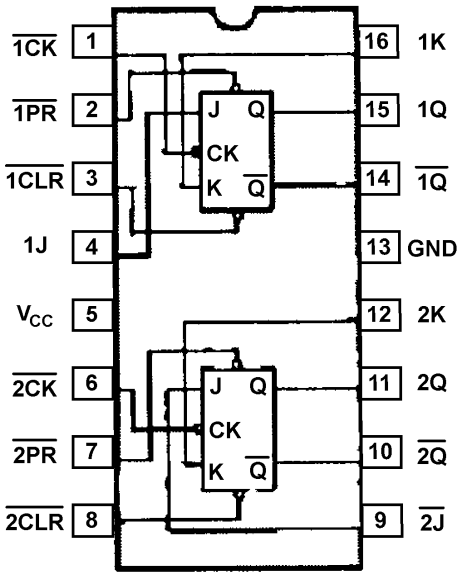
Note

1. H = HIGH voltage level
   L = LOW voltage level

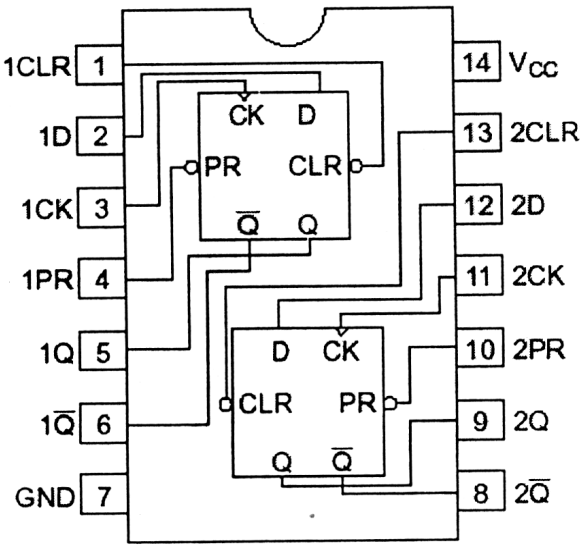
Function Table

DB11

Dual J-K Flip Flop **7476**



Dual D Flip Flop **7474**



Note: Pull up resistance of 1 k is required in open collector ICs to get output.

Warranty

1. We guarantee this product against all manufacturing defects for **12 months** from the date of sale by us or through our dealers.
2. The guarantee will become void, if
   a. The product is not operated as per the instruction given in the Learning Material.
   b. The agreed payment terms and other conditions of sale are not followed.
   c. The customer resells the instrument to another party.
   d. Any attempt is made to service and modify the instrument.
3. The non-working of the product is to be communicated to us immediately giving full details of the complaints and defects noticed specifically mentioning the type, serial number of the product and date of purchase etc.
4. The repair work will be carried out, provided the product is dispatched securely packed and insured. The transportation charges shall be borne by the customer.

Hope you enjoyed the Scientech Experience.

List of Contents