F2018 MTE220 Assignment 8

userid: _____

(1) supply a transistor level circuit diagram for the logic functions $\overline{(A+B)}.\overline{(C+D)}$

(2) Design a current mirror network which supplies

3 different sourcing currents (pmos)
3 different sinking currents (nmos)

and supply the $\frac{W}{L}$ ratios for

source current 1: 1x $I_{ref}$
source current 2: 4x $I_{ref}$
source current 3: 7x $I_{ref}$
sink current 1: 2x $I_{ref}$
sink current 2: 3x $I_{ref}$
sink current 3: 5x $I_{ref}$