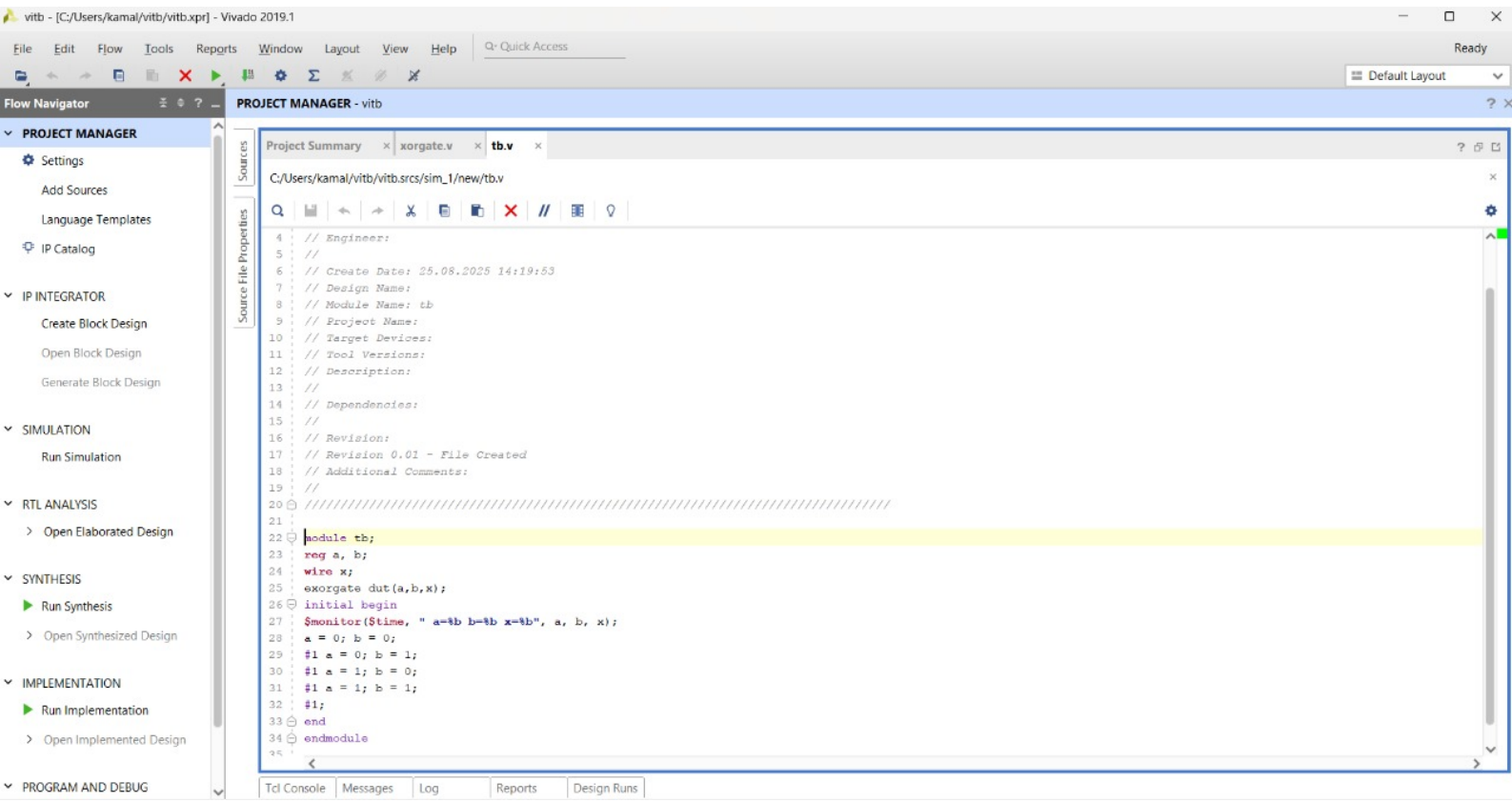
vitb - [C:/Users/kamal/vitb/vitb.xpr] - Vivado 2019.1
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tb.v
C:/Users/kamal/vitb/vitb.srcs/sim_1/new/tb.v
// Engineer:
//
// Create Date: 25.08.2025 14:19:53
// Design Name:
// Module Name: tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module tb;
reg a, b;
wire x;
exorgate dut(a,b,x);
initial begin
$monitor($time, " a=%b b=%b x=%b", a, b, x);
a = 0; b = 0;
#1 a = 0; b = 1;
#1 a = 1; b = 0;
#1 a = 1; b = 1;
#1;
end
endmodule
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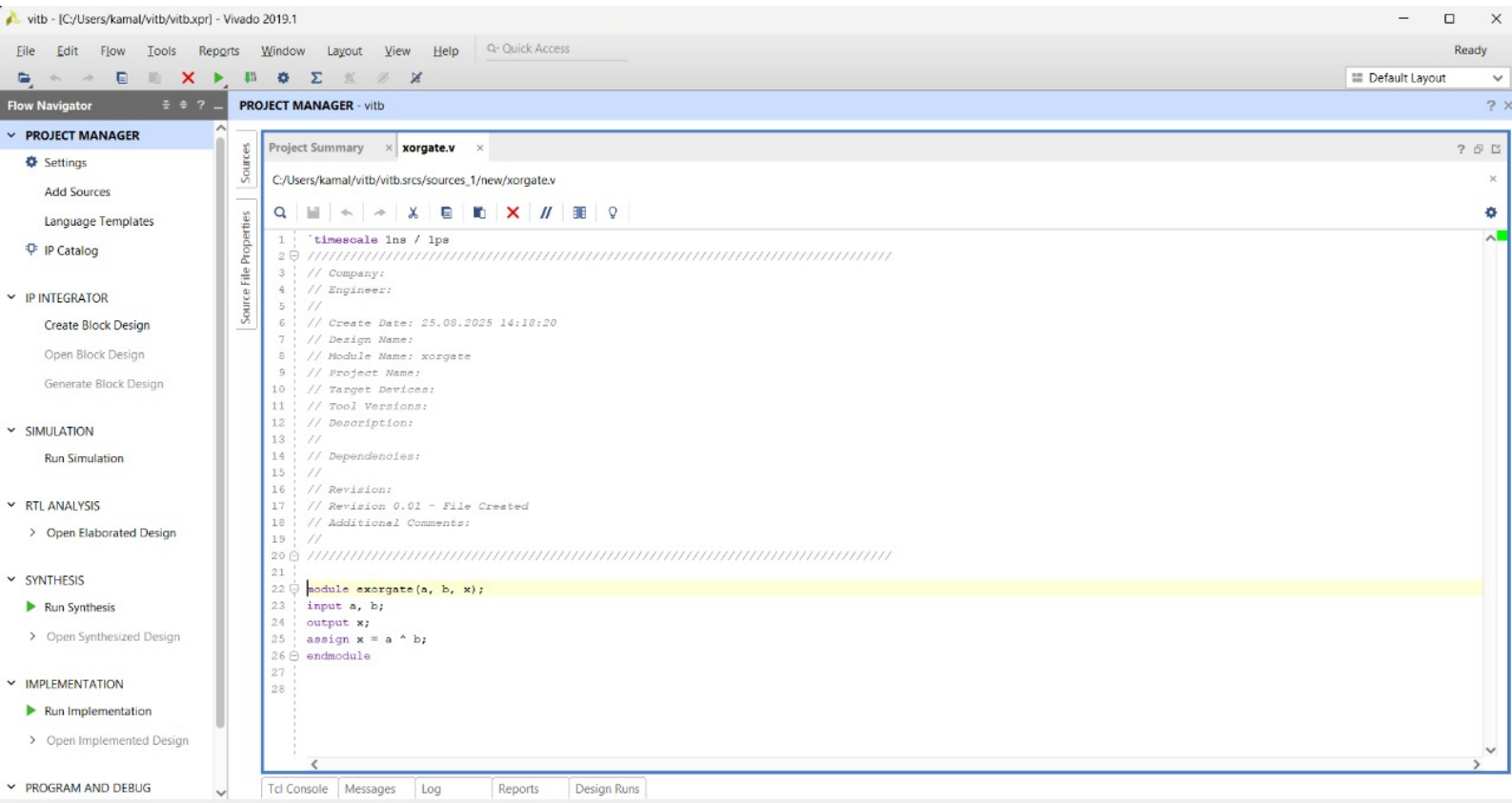
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xorgate.v
C:/Users/kamal/vitb/vitb.srcs/sources_1/new/xorgate.v
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 25.08.2025 14:18:20
// Design Name:
// Module Name: xorgate
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module xorgate(a, b, x);
input a, b;
output x;
assign x = a ^ b;
endmodule
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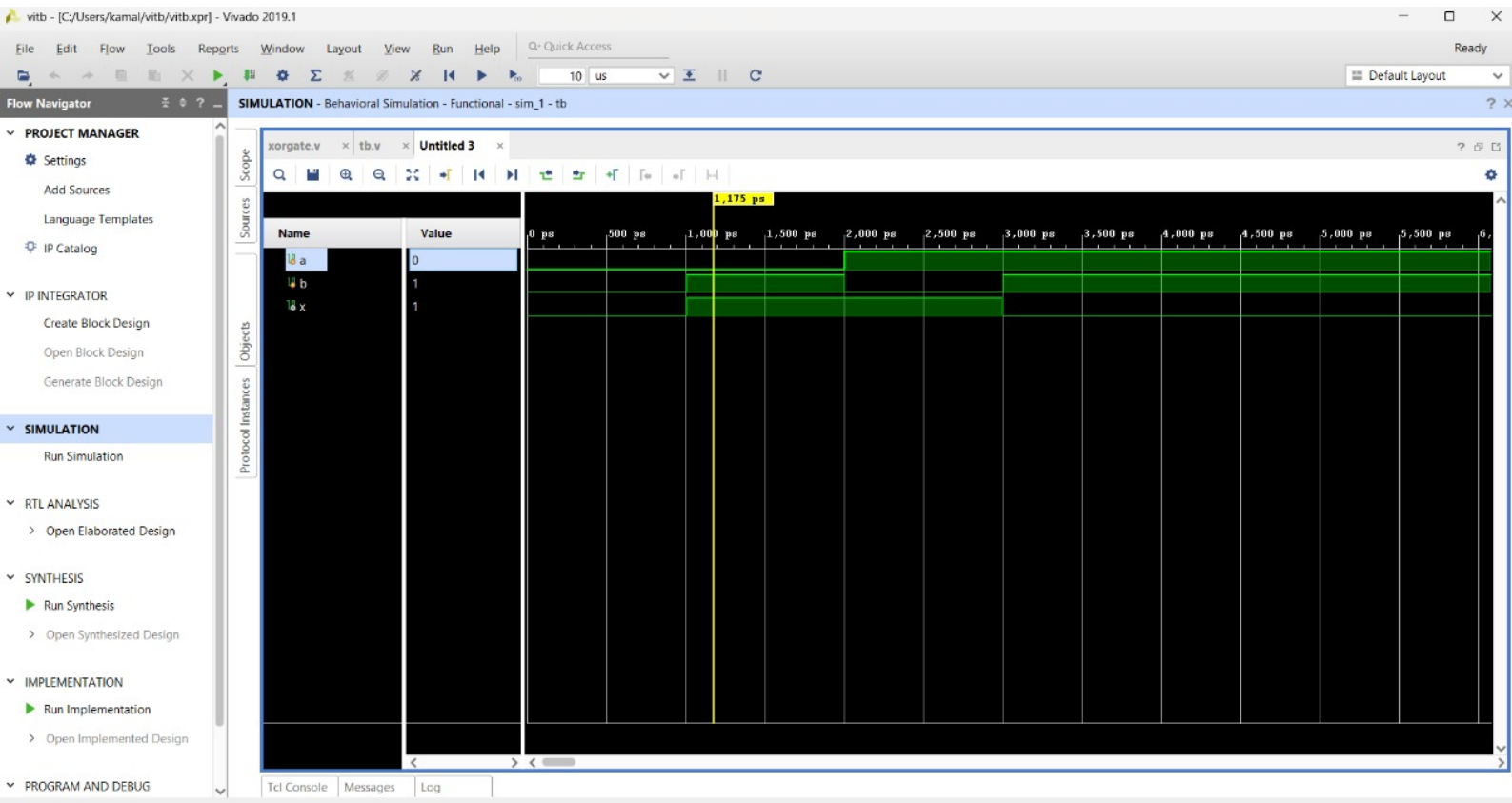
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Value
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b
x
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1,175 ps
0 ps
500 ps
1,000 ps
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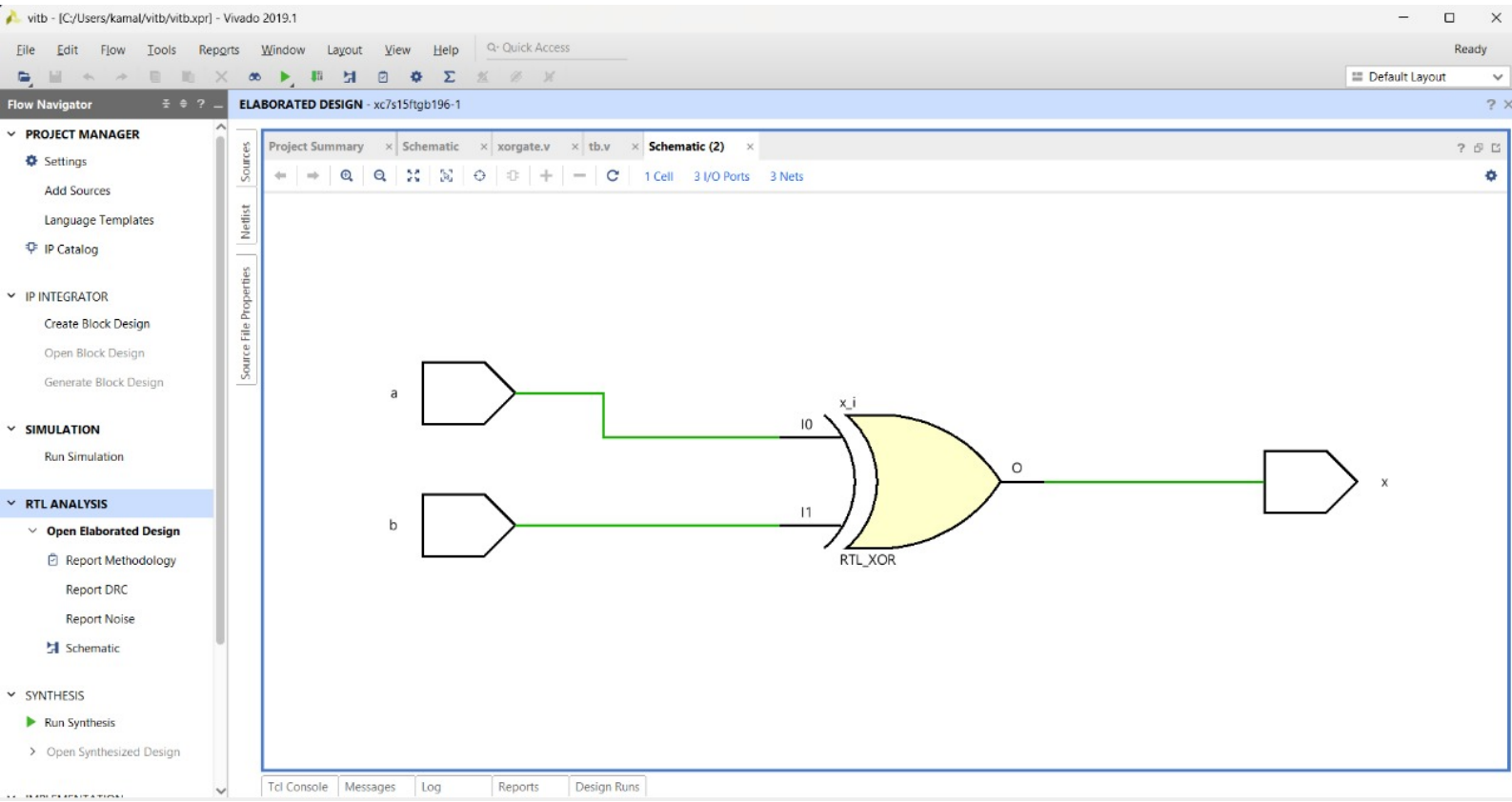
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I0
I1
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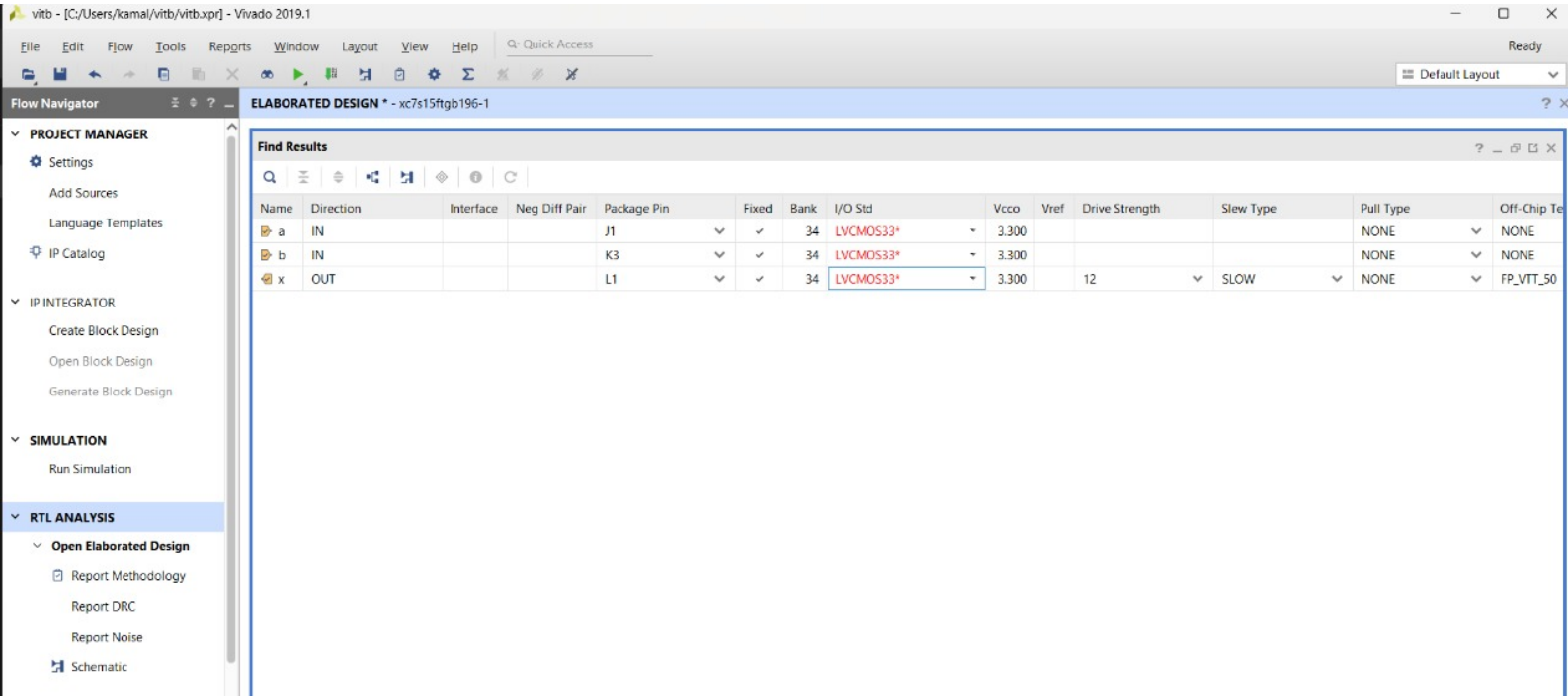
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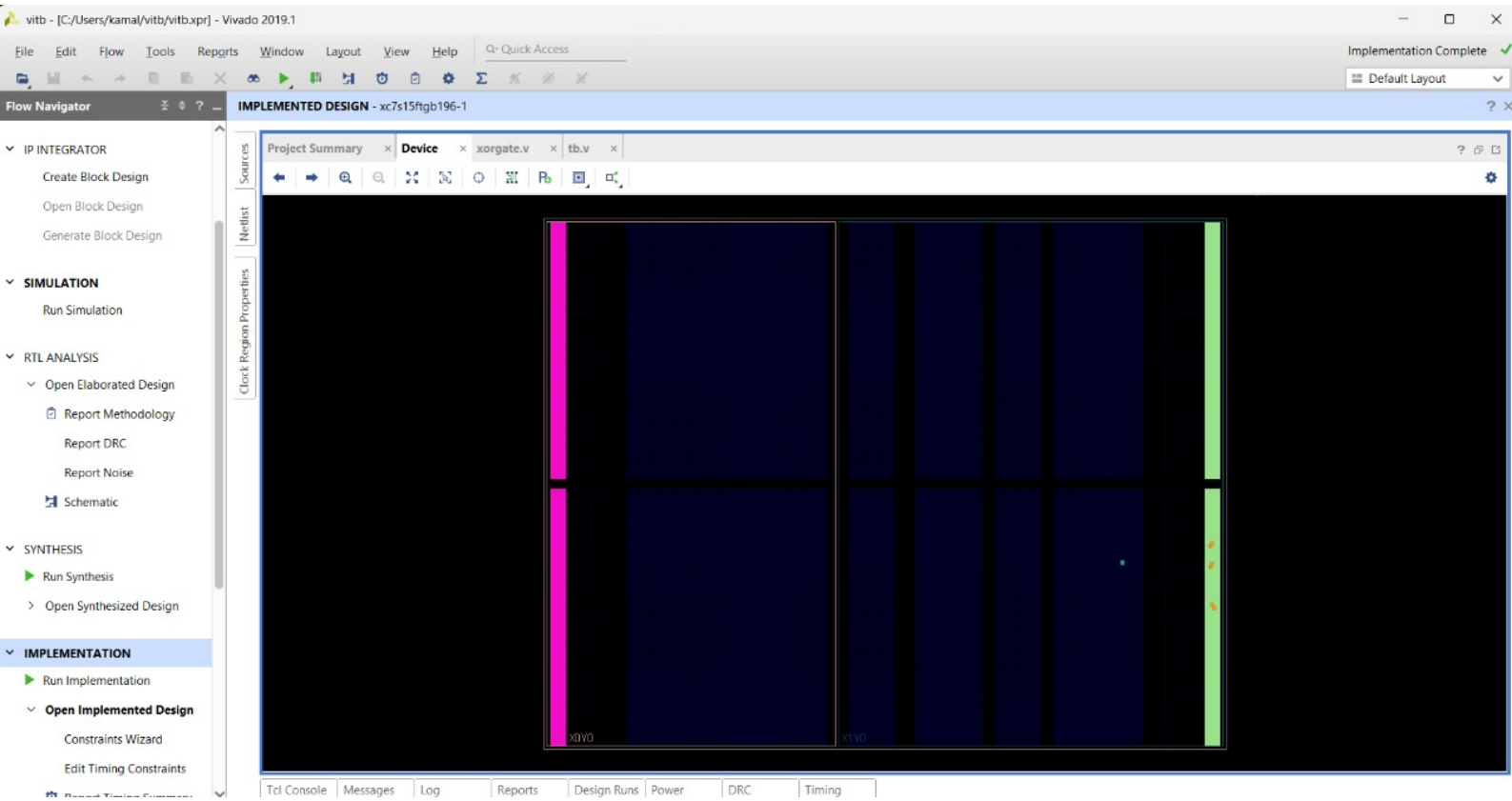
ELABORATED DESIGN * - xc7s15ftgb196-1
Find Results
Name Direction Interface Neg Diff Pair Package Pin Fixed Bank I/O Std Vcco Vref Drive Strength Slew Type Pull Type Off-Chip Te
a IN J1 34 LVCMOS33* 3.300 NONE NONE
b IN K3 34 LVCMOS33* 3.300 NONE NONE
x OUT L1 34 LVCMOS33* 3.300 12 SLOW NONE FP_VTT_50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