Department of Electrical,
Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor	Dr. Fei Yuan

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Assignment/Lab title	Design Project

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1. Introduction:

In this project, I will design a BJT amplifier circuit that accommodates the required specifications mentioned in the objectives section. This report contains 5 sections each with its respective purpose. To help explain why the chosen design was used.

2. Objectives:

The objective of this Design Project was to build a BJT amplifier circuit that meets the following specifications:

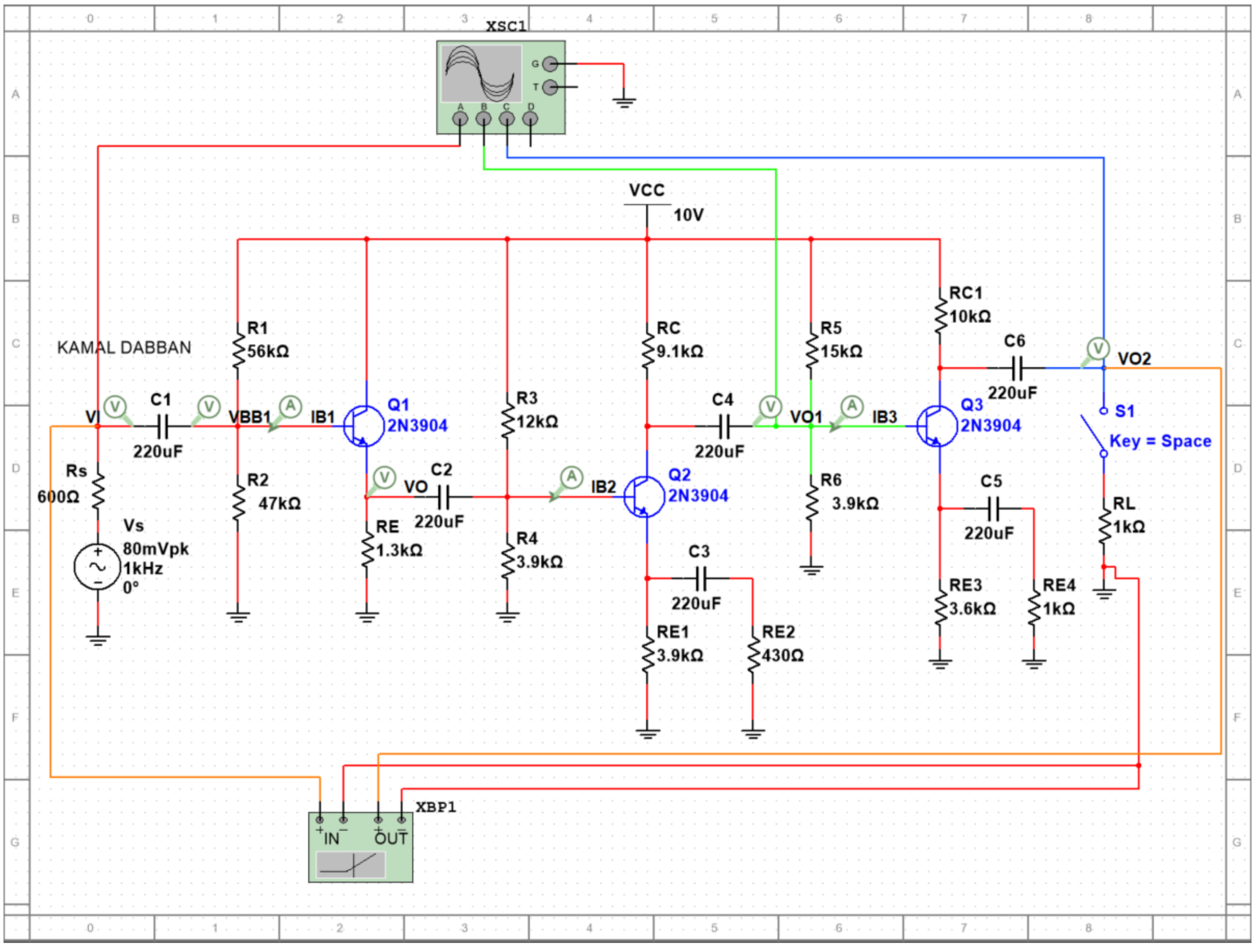
1) Power Supply: +10V relative to the ground.
2) Quiescent current drawn from the power supply: no larger than 10mA.
3) No-load voltage gain (at 1kHz): IAvol = 50(±10%).
4) Maximum no-load output voltage swing (at 1kHz): no smaller than 8V peak to peak.
5) Loaded voltage gain (at 1kHz and with RL = 1kΩ): no smaller than 90% of the no-load voltage gain.
6) Maximum loaded output voltage swing (at 1kHz and RL = 1kΩ): no smaller than 4V peak to peak.
7) Input resistance (at 1kHz): no smaller than 20kΩ.
8) Amplifier type: inverting or non-inverting.
9) Type of transistors: BJT.
10) Number of transistors (stages): no more than 3.
11) Resistances permitted: values smaller than 220kΩ from the E24 series.
12) Capacitors permitted: 0.1μF, 1μF, 2.2μF, 4.7μF, 10μF, 47μF, 100μF, 220μF.
13) Other components (BJTs, diodes, Zener diodes etc.): only from your ELE404 lab kit.
14) Source resistance must be 600Ω for all tests.

3. Circuit Under Test:

The Configuration:

From **Schematic 1**, I chose the following configuration to meet the requirements for this project:
Stage 1: CC amplifier
Stage 2: CE amplifier
Stage 3: CE amplifier
These amplifiers were chosen to acquire the desired gain that was specified easily. The reason why I chose a CC amplifier as my initial stage (Stage 1) was to achieve the required input resistance (greater than 20kΩ), where the output resistance is small in a CC amplifier, unlike the

input resistance. As for my 2nd and 3rd stages, I chose a CE amplifier to reach a high voltage gain of 50. (check specifications) Where the 2nd stage amplified the signal by roughly 5. Then, this gain was further amplified by about 10, from the 3rd stage CE amplifier. This brings a total gain of around 50.



Schematic 1: shows the full circuit containing a CC to CE to CE amplifiers.

Analysis:

Ele 404 Design Project: 5/04/2024

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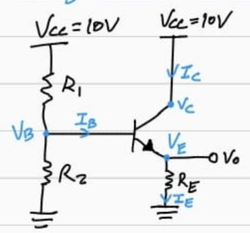
Analysis:

(Break the original circuit into 3 part for easy analysis)

Stage 1:

Analysing CC-Amp @ DC: (C_1 and C_2 are open circuit)



$$V_B = \frac{R_2}{R_2+R_1}(10)$$

For BJT to be in active mode ($V_{BE} = 0.7V$):

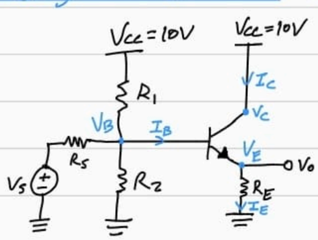
$\therefore V_{BE} = V_B - V_E = 0.7V$

$\therefore V_E = V_B - 0.7V = V_o$

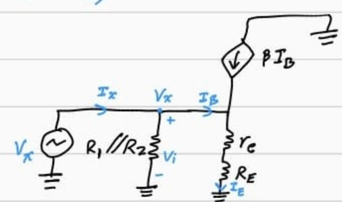
$\therefore V_C = 10V$

Note: $I_E = I_C + I_B$ and $I_C = \beta I_B$

Analysing CC-Amp @ AC: (C_1 and C_2 are short circuit)



Small-signal Equivalent circuit



$$I_B + \beta I_B = \frac{V_x}{r_e + R_E}$$

$$I_B(1+\beta) = \frac{V_x}{r_e + R_E}$$

$$I_B = \frac{V_x}{r_e + R_E}\left(\frac{1}{1+\beta}\right)$$

Plug in

KCL @ V_x:

$$I_x + \beta I_B = \frac{V_x}{r_e + R_E} + \frac{V_x}{R_1 // R_2}$$

$$V_x\left(\frac{1}{r_e + R_E} + \frac{1}{R_1 // R_2}\right) = \beta I_B + I_x$$

$$V_x\left(\frac{1}{r_e + R_E} + \frac{1}{R_1 // R_2}\right) = \frac{V_x}{r_e + R_E}\left(\frac{\beta}{1+\beta}\right) + I_x$$

$$V_x\left(\frac{1}{r_e + R_E} + \frac{1}{R_1 // R_2}\right) - \frac{V_x}{r_e + R_E}\left(\frac{\beta}{1+\beta}\right) = I_x$$

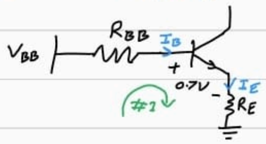
$$V_x\left(\frac{1 - \frac{\beta}{\beta+1}}{r_e + R_E}\right) + \frac{V_x}{R_1 // R_2} = I_x$$

$$V_x\left[\frac{1 - \frac{\beta}{\beta+1}}{r_e + R_E} + \frac{1}{R_1 // R_2}\right] = I_x$$

$$\therefore \frac{V_x}{I_x} = R_{in} = \frac{1}{\left[\frac{1 - \frac{\beta}{\beta+1}}{r_e + R_E} + \frac{1}{R_1 // R_2}\right]}$$

$$r_e = \frac{V_T}{I_B(1+\beta)}$$

$$V_{BB} = V_{cc}\left(\frac{R_2}{R_1+R_2}\right)$$



KVL @ #1:

$$V_{BB} = R_{BB}I_B + 0.7 + (1+\beta)R_E I_B$$

$$V_{BB} = 0.7 + I_B\left[R_{BB} + (1+\beta)(R_E)\right]$$

$$\therefore I_B = \frac{V_{BB} - 0.7V}{R_{BB} + (1+\beta)(R_E)}$$

Note:

By picking values for R_1 and R_2 in $k\Omega$ ranges. What our DC bias is since it will change I_B by a tiny bit. So as long as the chosen DC Voltage bias is greater than 0, we should be ok.

Let $R_1 = 56k\Omega$ and $R_2 = 47k\Omega$.

$$V_{BB} = V_{cc}\left(\frac{47k}{56k+47k}\right) = 4.563V$$

$$\therefore R_{BB} = \left(\frac{1}{56k} + \frac{1}{47k}\right)^{-1} \approx 25.6k\Omega$$

$$\therefore I_B = \frac{V_{BB} - 0.7}{25.6k + (151)(1.3k)} = 1.741\times10^{-5}A$$

I chose this value for R_E because when we cascade the multiple stage, the equation of I_B becomes: $I_B = \dfrac{V_{BB} - 0.7}{R_{BB} + 151(R_E // R_C)}$

$\therefore$ if R_E is small, I_B is small which doesn't affect r_e.

$$\therefore r_e = \frac{V_T}{I_B(\beta+1)} = \frac{26\times10^{-3}}{1.741\times10^{-5}(151)} = 9.89\Omega$$

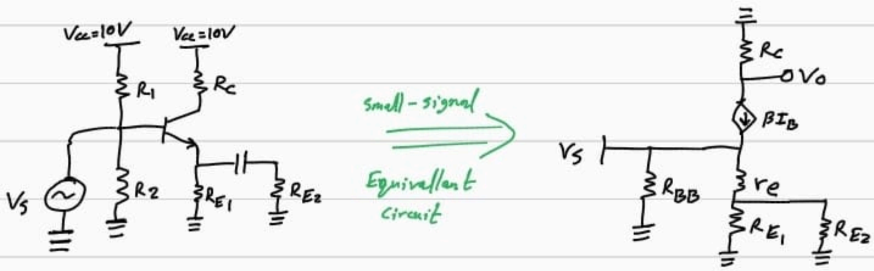
$$\therefore R_{in} = \frac{1}{\left[\frac{1-\frac{\beta}{\beta+1}}{r_e+R_E} + \frac{1}{R_1//R_2}\right]} = \frac{1}{\frac{1-\frac{150}{151}}{9.89+1.3k} + \frac{1}{56k//47k}} \approx 22.63k\Omega$$

The gain of CC Amp:

KCL @ V_o: $\dfrac{V_o}{R_E} + \dfrac{V_o - V_x}{r_e} = 0 \rightarrow V_o\left(\dfrac{1}{R_E} + \dfrac{1}{r_e}\right) = \dfrac{V_x}{r_e}$

$$\therefore \frac{V_o}{V_x} = \frac{1}{r_e\left(\frac{1}{R_E} + \frac{1}{r_e}\right)} = \frac{1}{\frac{r_e}{R_E}+1} = 0.992 \approx 1$$

Stage 2:



$$V_{BB} = V_{cc}\left(\frac{R_2}{R_2+R_1}\right)$$

$$R_{BB} = R_1 \,//\, R_2$$

$$R_E = R_{E_1} \,//\, R_{E_2}$$

KCL @ V_o:

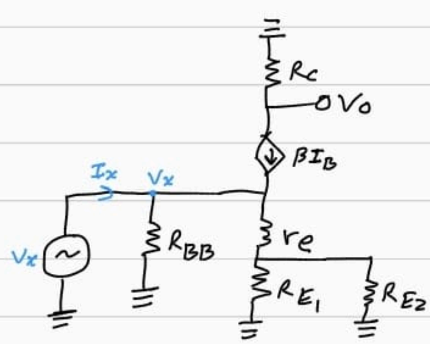
$$\frac{V_S}{R_C} = \beta I_B = \frac{\beta}{\beta+1} I_E = \alpha \frac{V_S}{r_e + R_E}$$

$$\therefore V_S = \frac{\alpha V_S R_C}{r_e + R_C}$$

No-load gain: $\dfrac{V_o}{V_S} = \dfrac{\alpha R_C}{r_e + R_E}$

Loaded gain: $\dfrac{V_o}{V_S} = \dfrac{\alpha (R_C // R_L)}{r_e + R_E}$

Input resistance: $R_{in} = \dfrac{V_x}{I_x}$



KCL @ V_x:

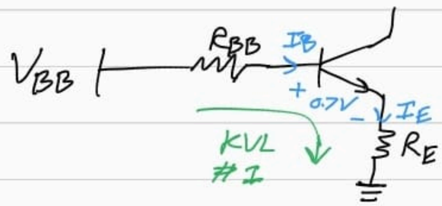
$$I_x = \frac{V_x}{R_{BB}} + I_E(1-\alpha)$$

$$= \frac{V_x}{R_{BB}} + \frac{V_x}{r_e + R_E(1-\alpha)}$$

$$= \frac{V_x}{R_{BB}} + \frac{V_x}{r_e + R_E\left(1-\frac{\beta}{\beta+1}\right)}$$

$$= \frac{V_x}{R_{BB}} + \frac{V_x}{r_e + R_E}\left(\frac{1}{\beta+1}\right)$$

$$\therefore \frac{V_x}{I_x} = R_{in} = R_{BB} \,//\, (\beta+1)(r_e + R_E)$$



KVL @ #1:

$$V_{BB} = R_{BB} I_B + 0.7 + R_E(1+\beta) I_B$$

$$V_{BB} = 0.7 + I_B\left[R_{BB} + R_E(1+\beta)\right]$$

$$\therefore I_B = \frac{V_{BB} - 0.7}{R_{BB} + R_E(1+\beta)}$$

Since we need I_B to be large, we need to use a small R_{E_1} in the kΩ range. This is to properly DC bias the CE Amplifier.

Let $R_{E_1} = 3.9\,k\Omega$

Since we already met the requirement for the Rin to be greater than 20kΩ. I will not be concerned about Rin unless it affects the gain.

$\therefore$ Let $R_1 = 12\,k\Omega$ and $R_2 = 3.9\,k\Omega$

$$\therefore R_{BB} = \left(\frac{1}{12k} + \frac{1}{3.9k}\right)^{-1} \approx 2.94\,k\Omega$$

Since we need a big I_B to decrease our r_e. This could be use to increase our gain. To do that, we will use a small R_{E_2} with respect to R_C.

$\therefore R_{E_2} = 430\,\Omega$

$$V_{BB} = 10\left(\frac{3.9k}{12k + 3.9k}\right) = 2.453V$$

$$I_B = \frac{2.453 - 0.7}{2.94k + 151(3.9k // 0.43k)} = 2.854 \times 10^{-5} A$$

$$r_e = \frac{V_T}{I_B(\beta+1)} = \frac{26 \times 10^{-3}}{2.854 \times 10^{-5}(151)} = 6.033\,\Omega$$

$$A_{vo} = \frac{\alpha R_C}{r_e + R_E} = \frac{\alpha R_C}{393.33} \longrightarrow A_V = \frac{\alpha (R_C // R_L)}{393.33}$$

To Avoid distortions we will take $R_C = 9.1\,k\Omega$.

$\therefore A_{vo} = 22.98$ (will calculate AV Later after the 3rd stage.)

Stage 3:

$V_{BB} = V_{cc}\left(\frac{R_2}{R_2+R_1}\right)$

Let $R_1 = 15k\Omega$ and $R_2 = 3.9k\Omega$

$\therefore V_{BB} = 10\left(\frac{3.9k}{15k+3.9k}\right) = 2.063\,V$

$\therefore R_{BB} = R_1 // R_2 \approx 3.1\,k\Omega$

$\therefore I_B = \frac{V_{BB}-0.7}{R_{BB}+(\beta+1)R_E} = \frac{2.063-0.7}{3.1k+151(782.6)} = 1.124\times10^{-5}A$

$\therefore r_e = \frac{V_T}{I_B(\beta+1)} = \frac{26\times10^{-3}}{1.124\times10^{-5}(151)} = 15.32\,\Omega$

$\therefore A_{vo} = \frac{\alpha R_c}{r_e+R_E} = \frac{\alpha R_c}{782.61}$ (Let $R_c = 10k\Omega$)

$\therefore A_{vo} = 12.69$

Mostly used the same resistors as stage 2, but some were changed to prevent distortions and because of the $R_L = 1k\Omega$ in the circuit.

Note: $R_E = R_{E3} // R_{E4}$

where $R_{E_3} = 3.6k\Omega$, $R_{E_4} = 1k\Omega$

$\therefore R_E = 782.61\,\Omega$

Rin of 3rd stage CE Amp:

$R_{in} = R_{BB} // (\beta+1)(r_e+R_E)$

$R_{in} = 3.1k // 151(782.61)$

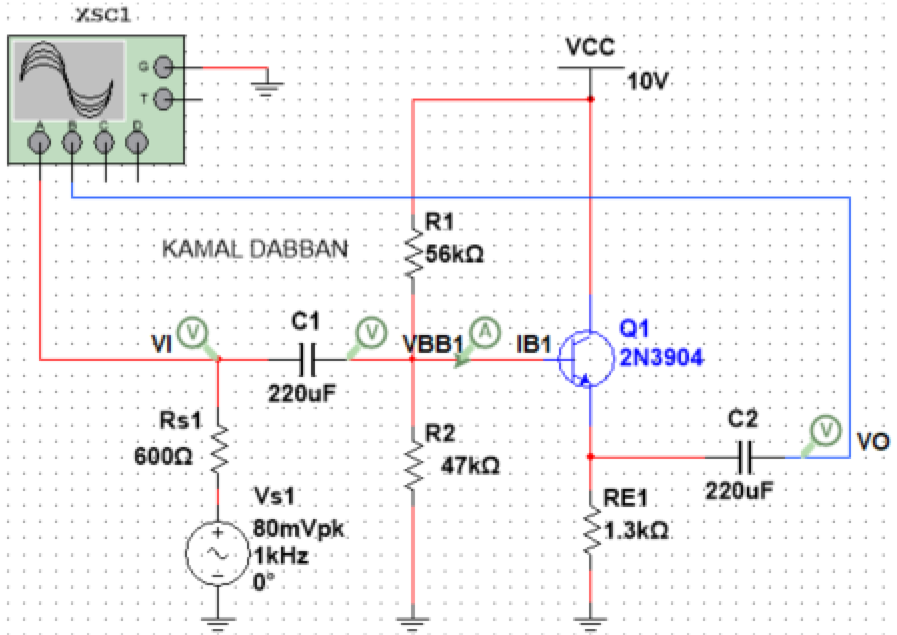
$R_{in} = \left(\frac{1}{3.1k}+\frac{1}{118.174k}\right)^{-1}$

$\therefore R_{in} = 3.021\,k\Omega$

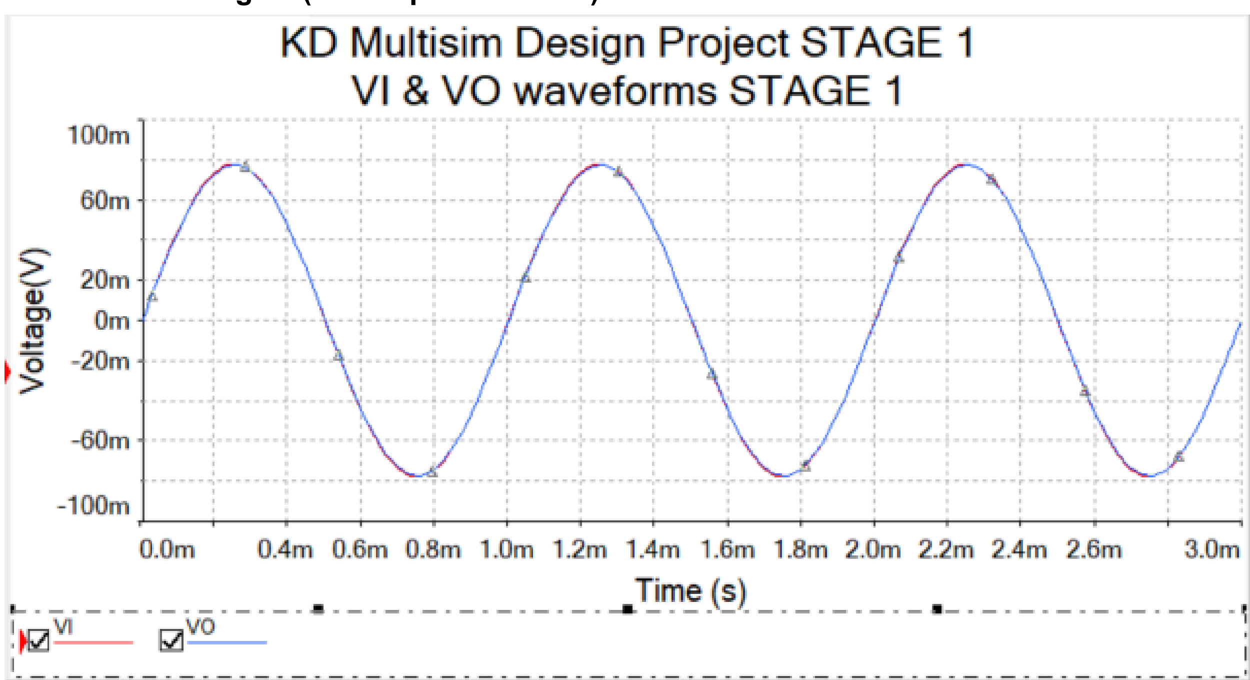
$\therefore$ Av of stage 2:

$A_v = \frac{\alpha(9.1k // 3.021k)}{393.33} \approx 5.73$

4. Experimental Results:



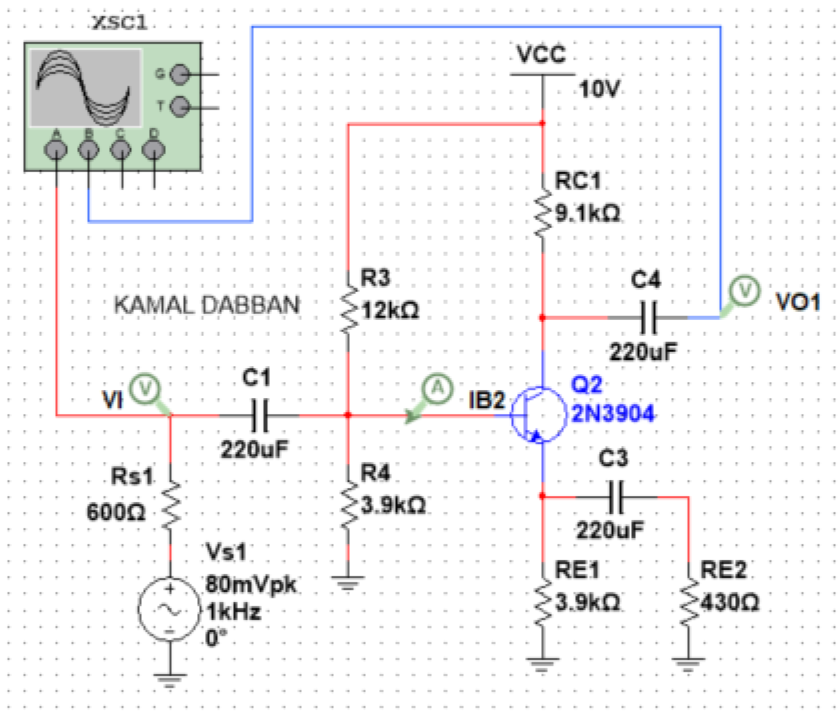
Schematic 2: Stage 1 (CC Amplifier Circuit)



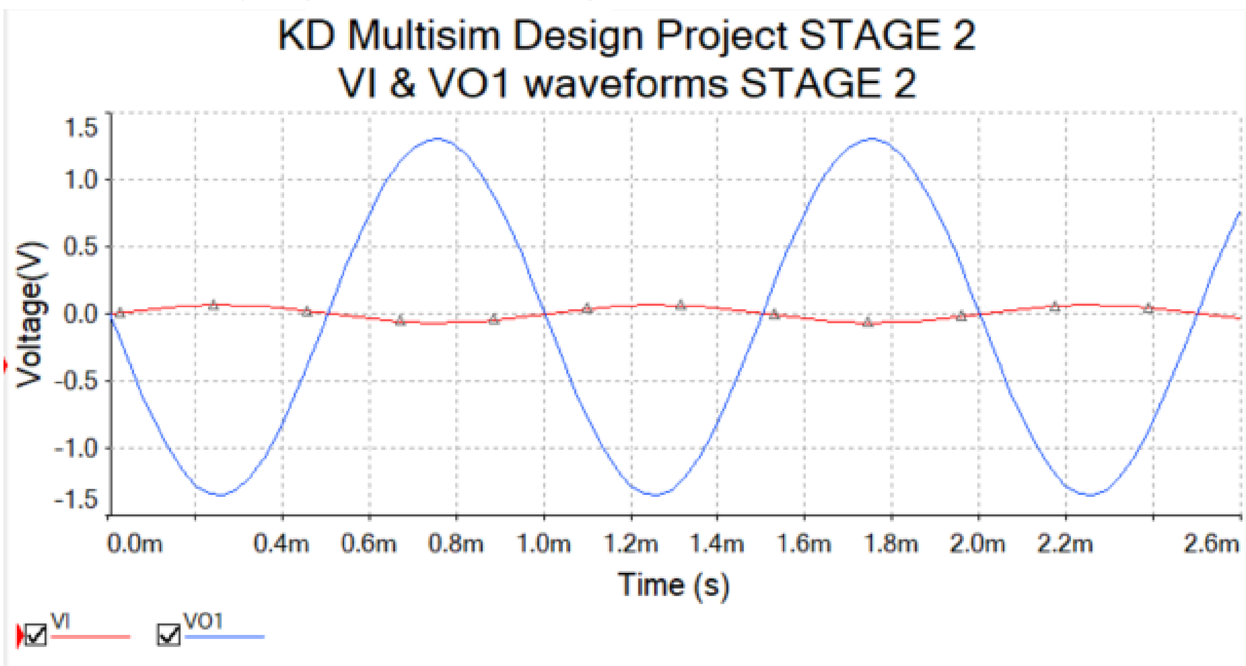
Graph 1: VI and VO waveforms of Stage 1 amplifier for schematic 2.

Comments:

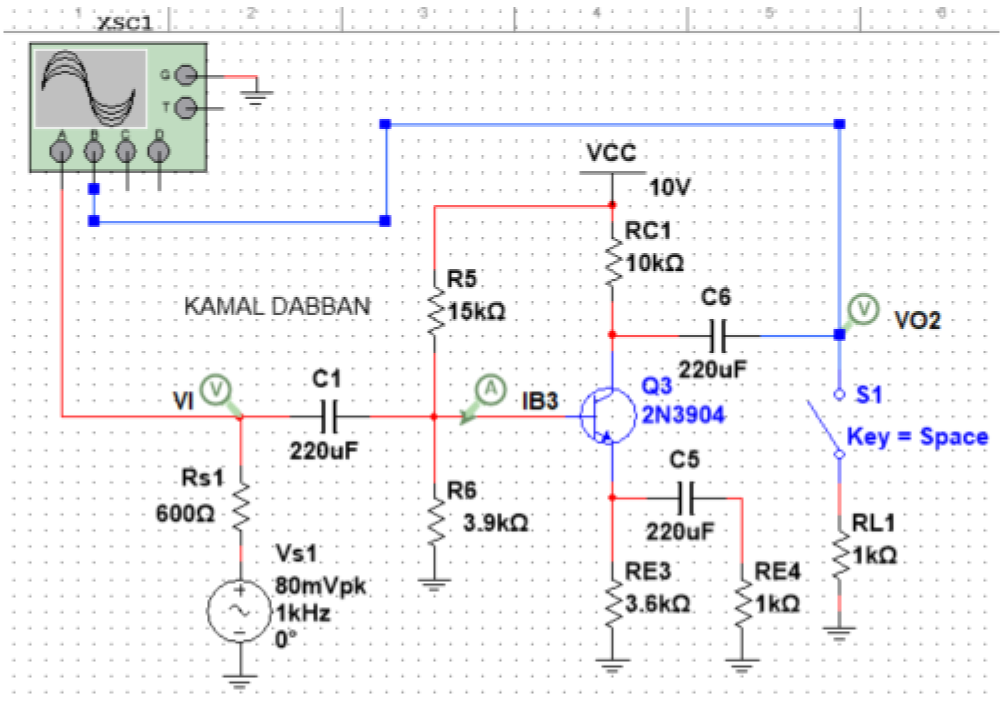
The manual calculations in this stage is similar to experimental results, because the gain of this amplifier is about 1.



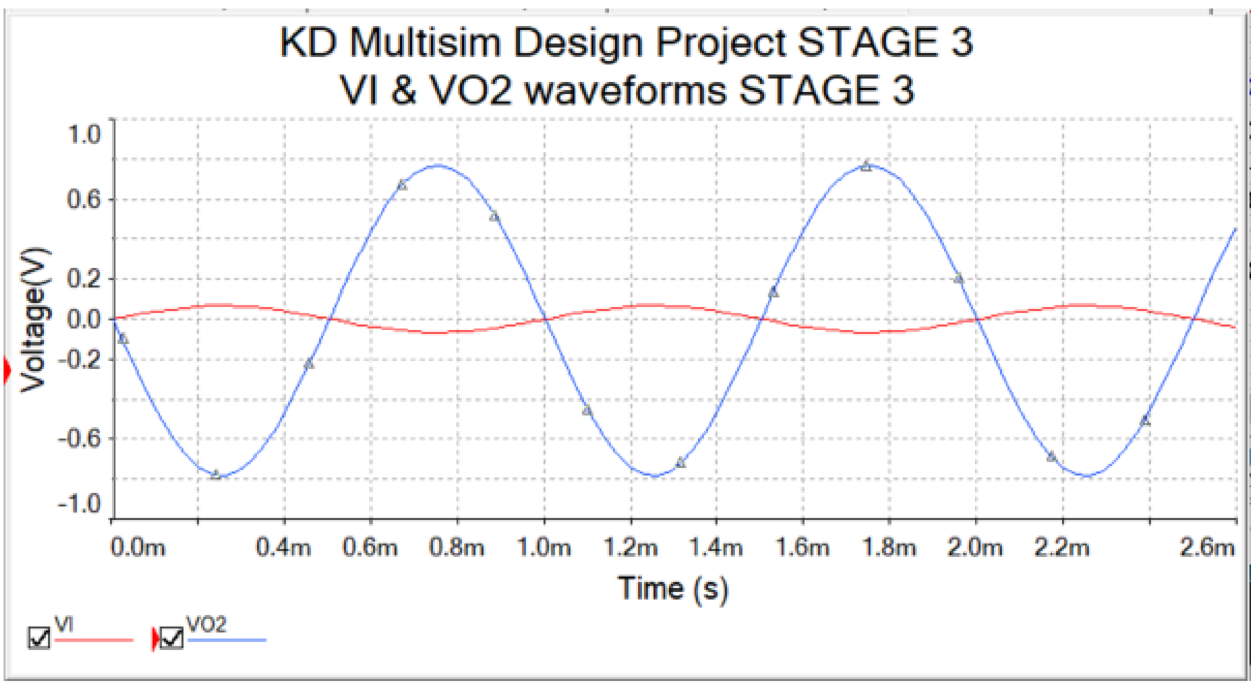
Schematic 3: Stage 2 (CE Amplifier Circuit)



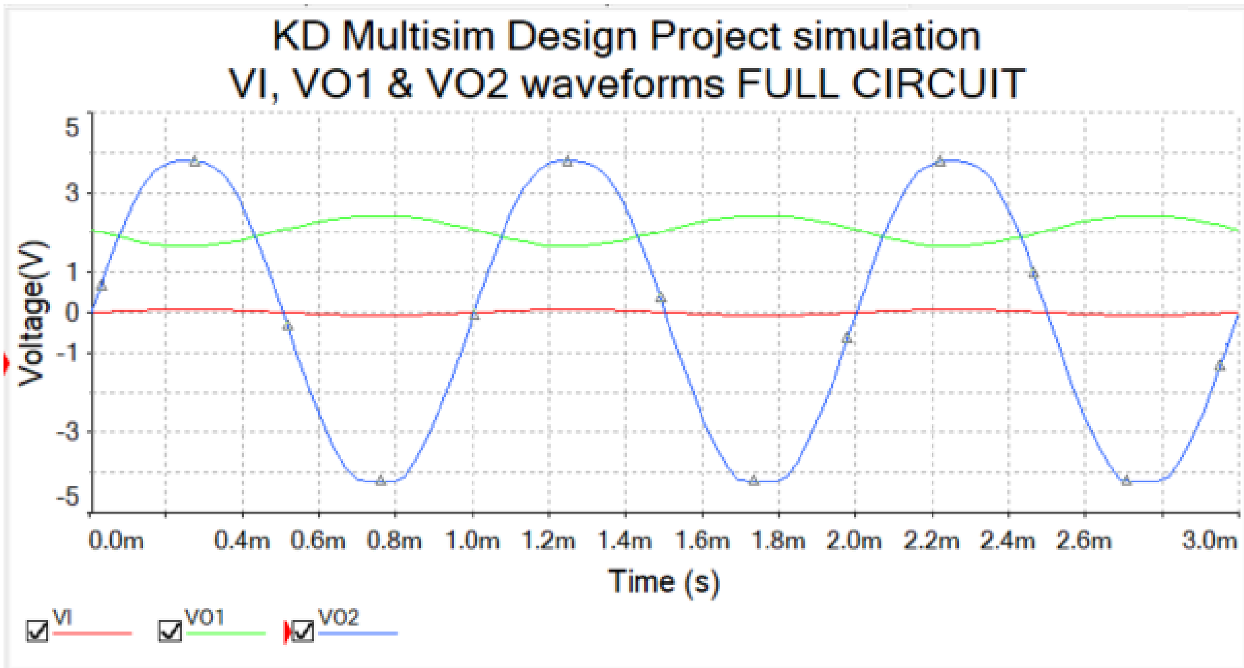
Graph 2: VI and VO1 waveforms of Stage 2 amplifier for schematic 3.



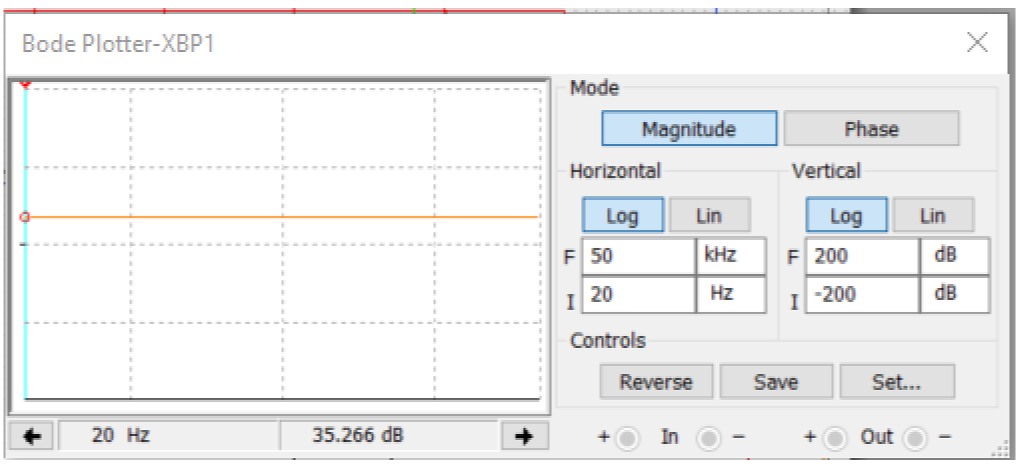
Schematic 4: Stage 3 (CE Amplifier Circuit)



Graph 3: VI and VO2 waveforms of Stage 3 amplifier for schematic 4.



Graph 4: VI, VO1 and VO2 waveforms of all stages from schematic 1.



Graph 5: The frequency response of the whole amplifier circuit from 20Hz to 50KHz.

5. Conclusions and Remarks:

Throughout this project, I showed you that the design meets the required specifications, even though there were some distortions found in the final output waveform.

Compared to the manual calculations, the only stage that had identical waveforms was the CC amplifier (State 1). This is because the gain is very close to one (thus a constant wave), and its only purpose is to meet the input resistance requirement of greater than 20k ohms, which was not impacted by the rest of the circuit because of the emitter resistance values.

As for the CE amplifier in stage 2, our experimental results met the manual calculations, while using special resistance values to avoid distortions. The gains of both experimental and manual do match. Take note that VI's amplitude is 77.79 mV, while VO1 (output of stage 2 specifically) has an amplitude of 378.39 mV. Therefore our experimental gain is 4.864, which is roughly consistent with my manual gain of 5.73.

As for our CE amplifier in stage 3, our experimental results met the manual calculations, while using special resistance values to avoid distortions. The gains of both the experimental and manual do actually match. Please note that stage 3's VI has an amplitude of 378.39 mV, while VO2 (stage 3's output) is 4.01V. This means that our experimental gain is 10.60, which is roughly consistent with our manual gain of 12.69.

I believe that the reason why our experimental and manual gains have small differences yet are consistent is because of the distortions in the graph. Those could be fixed if we changed some resistance values and recalculated and simulated the project again.