The worst case delay happens when Cin changes from 0 to 1, the carry bit needs to propagate through all the skip cells and the bit slices. The best case delay is when A[15] or B[15] switches. The signal only needs to travel through one bit slice.

Size	V_{dd}	T_{worst}	T_{best}	I_{avg}	P_{avg}
90nm	1.2V	1.2451ns	94.2523ps	2.0923mA	2.51076mW
65nm	1.0V	2.1994ns	168.1142ps	1.1041mA	1.1041mW
45nm	0.7V	3.7763ns	164.2519ps	363.0073uA	254.10511uW

Using a smaller technology and lower voltage source decreases V_{ds} and the current, so the power decreases. The decrease in current also increases the effective resistance, so the switching delay increases.

Temp	T_{worst}	T_{best}	I_{avg}	P_{avg}
27C	1.2455ns	94.8021ps	2.0607mA	2.47284mW
30C	1.2575ns	95.7096ps	2.0149mA	2.41788mW
40C	1.3317ns	98.5743ps	1.8738mA	2.24856mW
50C	1.4235ns	101.8353ps	1.7483mA	2.09796mW
60C	1.5275ns	105.9529ps	1.6354mA	1.96248mW
70C	1.6447ns	110.2570ps	1.5332mA	1.83984mW
80C	1.7734ns	114.8672ps	1.4402mA	1.72824mW
90C	1.9218ns	119.5351ps	1.3555mA	1.6266mW
100C	2.0792ns	125.1272ps	1.2781mA	1.53372mW
110C	2.2576ns	130.5061ps	1.2073mA	1.44876mW
120C	2.4576ns	135.7033ps	1.1425mA	1.371mW

The increase in temperature decreases mobility and junction capacitance, so the current decreases. The power will also decrease, but the delay increases.

V_{dd}	T_{worst}	T_{best}	I_{avg}	P_{avg}
1.08V	1.4097ns	104.2244ps	1.6639mA	1.797012mW
1.104V	1.3644ns	102.4736ps	1.7456mA	1.9271424mW
1.128V	1.3228ns	100.1086ps	1.8293mA	2.0634504mW
1.152V	1.2892ns	97.7542ps	1.9150mA	2.20608mW
1.176V	1.2619ns	95.9808ps	2.0027mA	2.3551752mW
1.2V	1.2451ns	94.2523ps	2.0923mA	2.51076mW
1.224V	1.2327ns	92.6107ps	2.1838mA	2.6729712mW
1.248V	1.2215ns	91.2536ps	2.2776mA	2.8424448mW
1.272V	1.2083ns	89.9080ps	2.3738mA	3.0194736mW
1.296V	1.1913ns	88.6828ps	2.4726mA	3.2044896mW
1.32V	1.1714ns	87.8892ps	2.5743mA	3.398076mW

The change in voltage source will also cause a similar change to the voltages on the transistors, so the current follows. This inversely changes the delay.