



main.cph

sample.txt

```

actor scale (k: unsigned<8>)
  in (i: unsigned<8>)
  out (o: unsigned<8>)
  rules i -> o
  | x -> k*x
  ;

stream inp: unsigned<8> from "sample.txt";
stream outp: unsigned<8> to "result.txt";

net outp = scale 2 inp;

```

Capture rectangulaire

main_net.vhd

scale_act.vhd

main_tb.vhd

```

-- This file has been automatically generated by the Caph compiler (version
2.8.3)
-- from file main.cph, on 2017-05-31 at 17:13:49, by <unknown>
-- For more information, see : http://caph.univ-bpclermont.fr
-- -----

library ieee,caph;
use ieee.std_logic_1164.all;
use caph.core.all;
use caph.data_types.all;
use ieee.numeric_std.all;

entity main_tb is
end main_tb;

architecture arch of main_tb is

component main_net is
  port (
    w3_f: out std_logic;
    w3: in std_logic_vector(7 downto 0);
    w3_wr: in std_logic;
    w6_e: out std_logic;
    w6: out std_logic_vector(7 downto 0);
    w6_rd: in std_logic;
    clock: in std_logic;

```

```

# This is the Caph compiler, version 2.8.3
# (C) 2011-2017 J. Serot (Jocelyn.Serot@univ-bpclermont.fr)
# For more information, see : http://caph.univ-bpclermont.fr
# -----
# warning: VHDL annotation file fifo_caps.dat does not exist.
# Wrote file .\main_expanded.dot
# Reverting to default size for fifo F5
# Reverting to default size for fifo F4
# Wrote file .\main_net.vhd
# Wrote file .\scale_act.vhd
# Wrote file .\main_tb.vhd

```