Quartus II 32-bit - Z:/vhdl/caph/simple/simple_net - simple_net

File Edit View Project Assignments Processing Tools Window Help

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simple_net

Project Navigator

Entity

- Cyclone III: AUTO
- simple_net
  - dup_act:B3
  - dec_act:B4
  - inc_act:B5
  - mul_act:B6
  - fifo_fb:F7
  - fifo_fb:F8
  - fifo_fb:F9

Parameter Settings
---
depth = 3
size = 8
dept_th = 32

Hierarchy | Files | Design Units

Tasks

Flow: Short Compilation | Customize...

	Task
✓	Compile Design
✓	Analysis & Synthesis

inc_act.vhd

Compilation Report - simple_net

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global S
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Message
- Assembler
- TimeQuest Timing Analyze

Flow Summary

Flow Status	Successful - Fri Jul 04 16:14:19 2014
Quartus II 32-bit Version	13.1.0 Build 162 10/23/2013 SJ Full Version
Revision Name	simple_net
Top-level Entity Name	simple_net
Family	Cyclone III
Total logic elements	178 / 5,136 (3 %)
Total combinational functions	133 / 5,136 (3 %)
Dedicated logic registers	144 / 5,136 (3 %)
Total registers	144
Total pins	22 / 183 (12 %)
Total virtual pins	0
Total memory bits	0 / 423,936 (0 %)
Embedded Multiplier 9-bit elements	1 / 46 (2 %)
Total PLLs	0 / 2 (0 %)
Device	EP3C5F256C6
Timing Models	Final

Messages

All | <<Search>>

Type	ID	Message
		Running Quartus II 32-bit Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off simple_net -c simple_net
	20029	Only one processor detected - disabling parallel compilation
	12021	Found 2 design units, including 1 entities, in source file /vhdl/caph/lib/fifo_fb.vhd

System | Processing (120)

100% 00:01:06

Démarrer | Quartus II 32-bit - Z:/... | FR | 16:15

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