Guilin University of Electronic Technology

School of Artificial Intelligence

Examination of Foundations of Analog and Digital Electronic Circuits

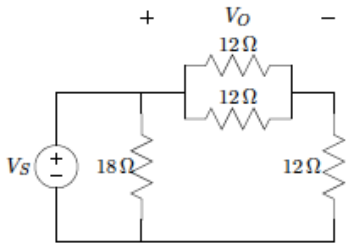
May 1, 2020

- Please write your name and ID in the space provided.
- Please verify that there are 8 pages in your exam.

Time:__120__minutes ID:_____ Name:_____

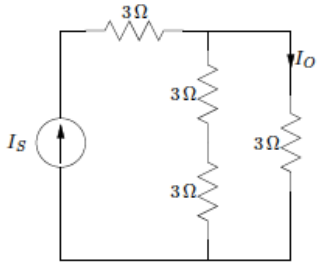
Number	一	二	三	四	Total
Points	50	10	20	20	100
Score					

1. (1A) (5 Points)



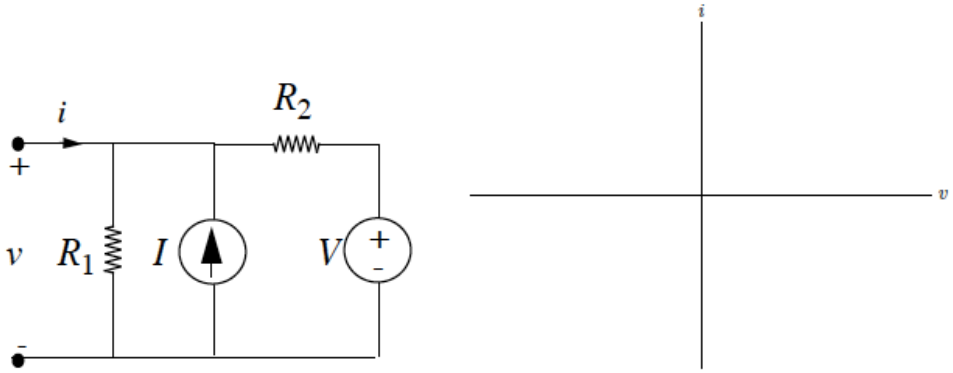
$\frac{V_O}{V_S} =$ 1/4 1/3 1/2 2/3 3/4

(1B) (5 Points)

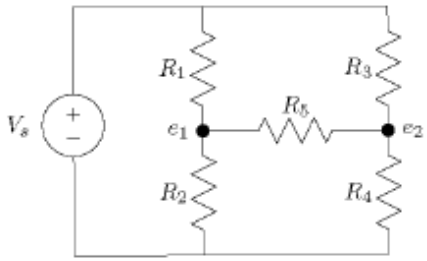


$\frac{I_O}{I_S} =$ 1/4 1/3 1/2 2/3 3/4

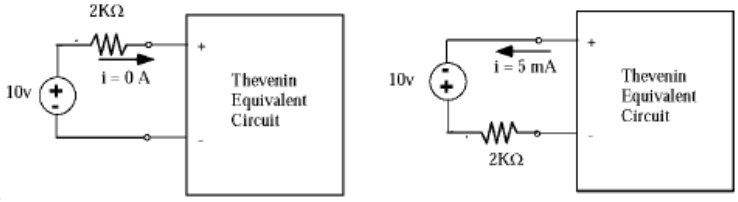
(1C) (5 Points) Graph the above network's *v-i* relations as viewed from its port. Clearly label the intercepts and the slope.



(1D) (5 Points) Write the node equations for the nodes e_1 and e_2 in the box below.

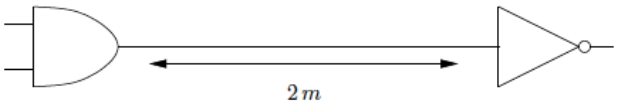


(1E) (5 Points) The current i is measured in two experiments which are performed on a Thevenin equivalent circuit as shown. What is the Thevenin equivalent resistance?



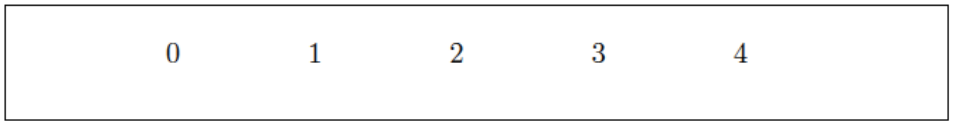
$R_{eq} =$ $0\,\Omega$ $1\,k\Omega$ $2\,k\Omega$ $10\,k\Omega$ $\infty\,\Omega$

(1F) (5 Points) Noise in the 2 meter digital channel shown above is added in at the rate of 0.6 V per meter. To correct for that noise, we introduce buffers into the channel. The purpose of a buffer is to take a signal, to which noise has been added so that it no longer meets the output specifications of the static discipline, and clean it up so that it once again meets the output specifications of the static discipline. These buffers, as well as the gates shown, obey the following static discipline:

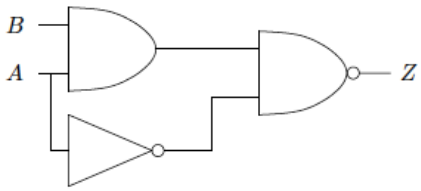


$V_{OL} = 1V$ $V_{OH} = 4V$
$V_{IL} = 2V$ $V_{IH} = 3V$

What is the minimum number of buffers required to connect between the digital links in order to insure correct operation?

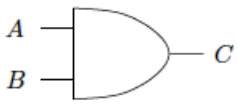


(1G) (5 Points) Fill in the truth table for the below digital circuit.

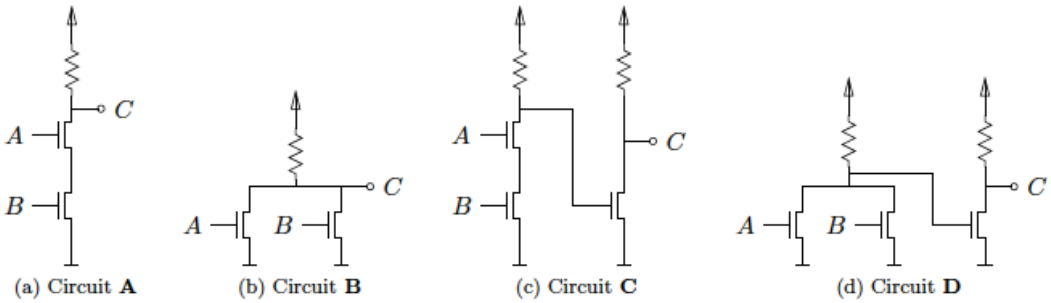


A	B	Z
0	0	
0	1	
1	0	
1	1	

(1H) (5 Points)



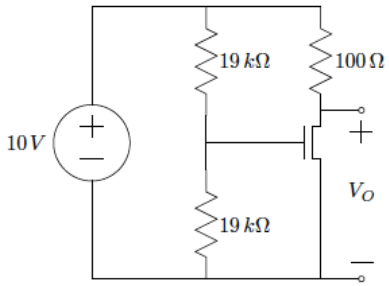
This gate is equivalent to:



(a) Circuit **A** (b) Circuit **B** (c) Circuit **C** (d) Circuit **D**

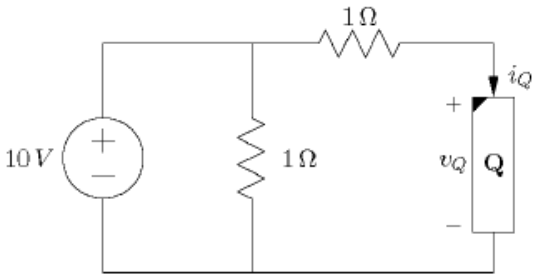
A	B	C	D	none of the above

(1I) (5 Points) Find the power dissipated in R_{ON}, if the MOSFETs are accurately represented by the switch-resistor model, where the threshold voltage V_T =2V and the on-resistance R_{ON} =100Ω.



P_{diss} =	0.25 W	0.5 W	0.75 W	1 W	2 W

(1J) (5 Points)



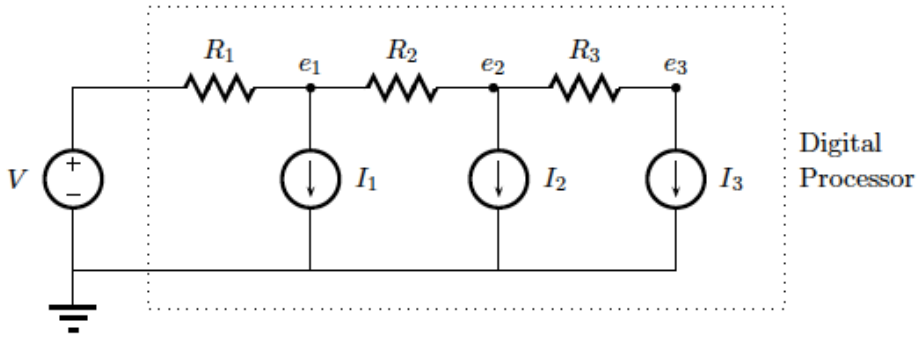
The device Q in the circuit shown above has the i–v relation

$$\begin{aligned} i_Q &= v_Q^2 + 2v_Q \quad && v_Q > 0 \\ i_Q &= 0 && v_Q \leq 0 \end{aligned}$$

Find the value of v_Q in the circuit.

v_Q =	$\frac{-3+\sqrt{11}}{2}$ V	1 V	2 V	$\frac{-3+\sqrt{29}}{2}$ V	10 V

2. (10 Points) The circuit shown below models the power distribution network in a digital processor. The voltage source models the external supply that powers the processor, the resistors model the power distribution wiring internal to the processor, and the current sources model the loads presented by the individual parts of the processor. The source values V, I_1, I_2 and I_3 are all positive, as are the three internal node voltages e_1, e_2 and e_3. Further, depending upon whether the corresponding part of the processor is in use or not, I_1, I_2 and I_3 can each take on only the value of either I or zero.

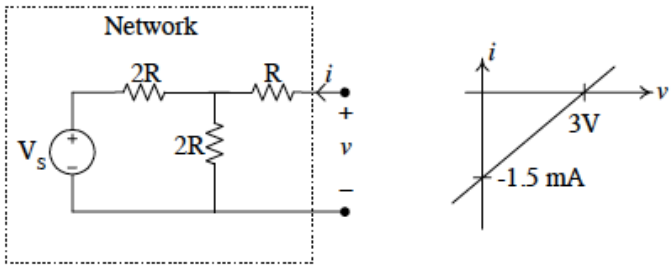


Using the node method, develop a set of simultaneous equations for the power distribution network that can be solved for the three unknown node voltages e_1, e_2 and e_3. Express these equations in the form

$$G \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = S$$

where G is a 3x3 matrix of conductance terms and S is a 3x1 vector of terms involving the sources V, I_1, I_2 and I_3. *You need not solve the set of equations for the node voltages.*

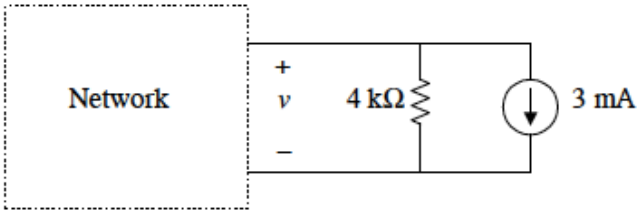
3. This problem involves a network that is implemented with three resistors and a voltage source as shown below. Its terminal characteristics are also given graphically below.



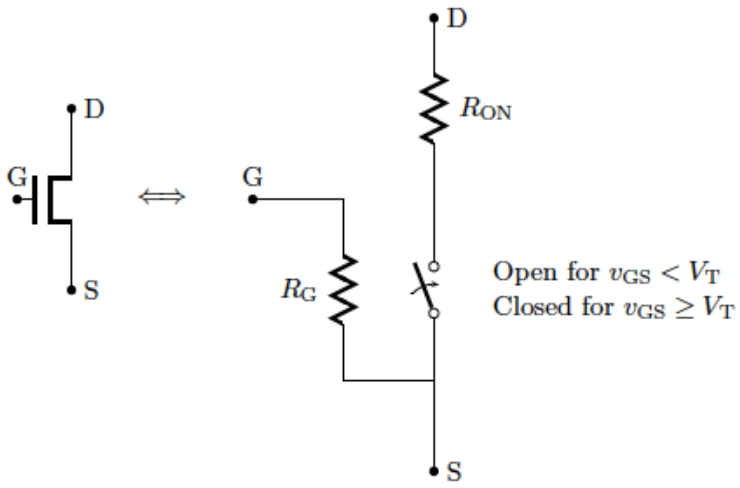
(3A) (10 Points) From the graphical data given above, determine numerical values for the parameters of the Thevenin equivalent of the network.

(3B) (5Points) Determine numerical values for the parameters V_S and R that characterize the implementation of the network shown above.

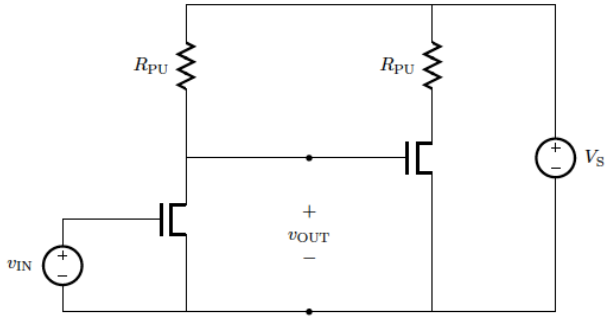
(3C) (5Points) The network is connected to an external current source and resistor as shown below. Determine the value of its terminal voltage v given the external connection.



4. In this problem the switch-resistor model of the MOSFET is expanded to include a finite gate-source resistance R_G. The corresponding model for the MOSFET is shown below.



(4A) (10 Points) Two inverters are connected in series as shown below. The MOSFET in both inverters has a finite gate-source resistance as modeled above. For this circuit, sketch and clearly label the transfer function for the first inverter, that is, v_{OUT} as a function of v_{IN}, over the range $0 \leq v_{IN} \leq V_S$ in the space given below. Assume that $V_S > V_T$.



(4B) (10 Points) Now consider the case in which the output of the first inverter is connected to the input of N identical inverters as shown below. Assuming that V_T, R_{ON} and R_G are all given, over what range must R_{PU} be designed so that the first inverter can successfully switch the states of the successive inverters. That is, over what range must R_{PU} be designed so that $v_{OUT} > V_T$ when $v_{IN} < V_T$, and $v_{OUT} < V_T$ when $v_{IN} > V_T$. Again, assume that $V_S > V_T$.