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| 1.1 **计算机组成与计算机体系结构在概念上有何区别?** |
| 计算机结构指的是系统的那些属性对程序员来说是可见的。程序员可见的属性，或者换句话说，那些对程序的逻辑执行有直接影响的属性。  计算机组织指的是实现架构规范的操作单元及其相互联系。  Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program.  Computer organization refers to the operational units and their interconnections that realize the architectural specifications. |

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| 1.2 **计算机结构与计算机功能在概念上有何区别?** |
| 计算机结构是指计算机各组成部分相互关联的方式。 互相关联的方式。  计算机功能指的是作为结构一部分的每个单独构成的一部分。  Computer structure refers to the way in which the components of a computer are interrelated.  Computer function refers to the operation of each individual component as part of the structure. |

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| 1.3 **计算机结构与计算机功能在概念上有何区别?** |
| Data processing; data storage; data movement; and control. |

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| 1.4**列出并概要定义计算机的主要结构部件。** |
| 中央处理单元（CPU):控制计算机的运行并执行其数据处理功能。通常简称为处理器。  主存储器：存储数据。  I/O：在计算机和其外部环境之间移动数据。  系统互连：提供CPU、主存储器和I/O之间通信的一些机制，它提供了CPU、主存储器和I/O之间的通信。系统互连的一个常见例子是通过系统总线由一些导电的电线组成，所有其他组件都连接在上面。  **Central processing unit (CPU):** Controls the operation of the computer and performs its data processing functions;  **Main memory:** Stores data.  **I/O:** Moves data between the computer and its external environment.  System interconnection: Some mechanism that provides for communication among CPU, main memory, and I/O. |

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| 1.5**列出并概要定义处理器的主要结构部件。** |
| 控制单元：控制CPU的运行，从而控制计算机的运行。  算术和逻辑单元（ALU）：执行计算机的数据处理功能  寄存器：提供CPU内部的存储  CPU互连：在控制单元、ALU和寄存器之间提供通信的某种机制。  **Control unit:** Controls the operation of the CPU and hence the computer.  **Arithmetic and logic unit (ALU):** Performs the computer’s data processing functions.  **Registers:** Provides storage internal to the CPU.  **CPU interconnection:** Some mechanism that provides for communication among the control unit, ALU, and registers. |

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| 3.3 **考虑一个假想的32位微处理器采用32位的指令格式，这种指令有两个部分:第1个字节包含操作码，其余部分是立即操作数或操作数的地址。**  **(a)最大可能直接寻址的存储器容量是多少(以字节为单位)?**  **(b)讨论下面的微处理器总线对系统的影响:**  **(1)32位局部地址总线和16位局部数据总线。**  **(2) 16 位局部地址总线和16位局部数据总线。**  **(c)程序计数器和指令寄存器需要多少位?** |
| a. 2的24次方=16MBytes  b.（1）如果本地地址总线是32位，整个地址可以一次性传输并在内存中解码。  然而，由于数据总线只有16位，需要2个周期来获取一个32位的指令或操作数。  （2）放在地址总线上的16位地址不能访问整个的地址，不能访问整个存储器。因此，需要一个更复杂的内存接口控制来锁定第一部分的地址，然后是第二部分对于一个32位的地址，我们可以假设前半部分会解码以访问内存中的 "行"，而后半部分将被发送以访问内存中的 "列"。除了两步的地址操作外，微处理器还需要两个周期的地址。  微处理器将需要2个周期来获取32位指令/操作数。  c.程序计数器必须至少有24位。通常情况下，一个32位的微处理将有一个32位的外部地址总线和一个32位的程序计数器，除非片上段寄存器，可以使用较小的程序计数器。如果指令寄存器包含整个指令，它必须是32位；如果它只包含操作代码（称为操作代码寄存器），那么它必须是8位。  a. 224 = 16 MBytes  b.  (1) If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.  (2) The 16 bits of the address placed on the address bus can't access the whole memory. Need a more complex memory interface control to latch the first part of the address and the second part (because the microprocessor will end in two steps). For a 32-bit address, one may assume the first half will decode to access a "row" in memory, while the second half is sent later to access a "column" in memory. In addition to the two-step address operation, the microprocessor will need 2 cycles to fetch the 32 bit instruction/operand.  c. The program counter must be at least 24 bits. Typically, a 32-bit microprocessor will have a 32-bit external address bus and a 32-bit program counter, unless onchip segment registers are used that may work with a smaller program counter. If the instruction register is to contain the whole instruction, it will have to be 32-bits long; if it will contain only the op code (called the op code register) then it will have to be 8 bits long. |

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| 3.4 **考虑一个假想的微处理器，它产生16位地址(例如，假设程序计数器和地址寄存器都是16位)，并且**  **有16位数据总线。**  **(a)如果处理器连接到“16位存储器”，那么它能直接访问的最大存储器地址空间是多少?**  **(b)如果处理器连到“8 位存储器”，那么它能直接访问的最大存储器地址空间是多少?**  **(c)结构上的什么特点允许处理器访问独立的“I/O 空间”?**  **(d)如果输人和输出指令能够指定一 个8位的I/O端口号，那么处理器能支持多少个8位的I/O端口?**  **它能支持多少个16位的I/O端口?请解释。** |
| 在(a)和(b)的情况下，微处理器将能够访问216=64K字节；唯一的区别是，8位内存的每次访问将传输一个字节，而16位内存的每次访问可以传输一个字节或一个16字节的字。对于情况（c）。需要单独的输入和输出指令，其执行将产生独立的 "I/O信号"（与执行内存型指令时产生的 "内存信号 "不同）。至少需要一个额外的输出引脚来承载这个新的信号。对于情况（d），它可以支持28=256个输入和28 = 256个输出字节端口，以及同样数量的输入和输出16位端口；在任何一种情况下，输入和输出端口之间的区别都是由执行的输入信号的不同来定义的。  **In cases (a) and (b),** the microprocessor will be able to access 216 = 64K bytes; the only difference is that with an 8-bit memory each access will transfer a byte, while with a 16-bit memory an access may transfer a byte or a 16-byte word.  **For case (c),** separate input and output instructions are needed, whose execution will generate separate "I/O signals" (different from the "memory signals" generated with the execution of memory-type instructions); at a minimum, need one additional output pin to carry this new signal.  **For case (d),** it can support 28 = 256 input and 28 = 256 output byte ports and the same number of input and output 16-bit ports; in either case, the distinction between an input and an output port is defined by the different signal that the executed input or output instruction generated. |

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| 4.5 **考虑一个32 位的微处理器，它采用16KB片内四路组相联cache。假设cache每行包含4个32位字。画出此cache的框图，并在图中表示其结构和如何使用不同的地址域来确定cache是否命中。存储单元地址ABCDE8F8映射到cache的什么地方?** |
| 块帧大小=16字节=4个双字  缓存中的块状框架数量 =16 KBytes/16个字节= 1024  套数=块状框架的数量/关联性=1024/4= 256组  Block frame size = 16 bytes = 4 doublewords  Number of block frames in cache =16 KBytes/16 Bytes= 1024  Number of sets =Number of block frames/Associativity=1024/4= 256 sets |

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| 4.8 **考虑一台机器，其主存可以按字节寻址，容量是216字节，块大小为8字节。假设该机器使用一个包含32行的直接映射cache。**  **(a)16位存储器地址如何划分成标记、行号和字节号?**  **(b) 如下地址的内容将存人cache的哪些行?**  **0001 0001 0001 1011**  **1100 0011 0011 0100**  **1101 0000 0001 1101**  **1010 1010 1010 1010**  **(c)假设地址0001 1010 0001 1010的字节内容存人cache,那么与它同存一行的其他字节的地址各是什么?**  **(d)存储器总共有多少字节能保存于cache 中?**  **(e)为何标记亦保存在cache中?** |
| a. 最左边8位=标签；中间5位=行号；最右边3位=字节数  b. 槽3；槽6；槽3；槽21  c. 地址为0001 1010 0001 1000至0001 1010 0001 1111的字节被存储在缓存中。  存储在高速缓存中  d. 256个字节  e. 因为两个不同内存地址的项目可以存储在缓存的同一个地方。  缓存中的同一个地方。标签是用来区分它们的。  a. 8 leftmost bits = tag; 5 middle bits = line number; 3 rightmost bits = byte number  b. slot 3; slot 6; slot 3; slot 21  c. Bytes with addresses 0001 1010 0001 1000 through 0001 1010 0001 1111 are stored in the cache  d. 256 bytes  e. Because two items with two different memory addresses can be stored in the same place in the cache. The tag is used to distinguish between them. |

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| 5.1 Semiconductor memory  **半导体存储器的主要性质是什么？** |
| 它们表现出两种稳定（或半稳定）的状态，可以用来表示二进制的1和0；它们能够被写入（至少一次）以设置状态；它们能够被读取以感知状态。  They two stable (or semistable) states, which can be used to represent binary 1 and 0; they are capable of being written into (at least once), to set the state; they are capable of being read to sense the state. |

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| 5.2  **术语“随机存取存储器”在使用上有哪两种含义？** |
| (1) 通过有线寻址逻辑直接访问内存中的各个字的存储器。  (2) 半导体主存储器，既可以从存储器中读取数据，又可以方便快捷地将新的数据写入存储器中。  (1) A memory in which individual words of memory are directly accessed through  wired-in addressing logic.  (2) Semiconductor main memory in which it is possible both to read data from the memory and to write new data into the memory easily and rapidly. |

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| 5.3  **DRAM和SRAM在应用上有何不同？** |
| SRAM用于高速缓冲存储器（包括片上和片下），DRAM用于主存储器。  SRAM is used for cache memory (both on and off chip), and DRAM is used for  main memory. |

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| 5.4  **在速度、容量、成本上DRAM和SRAM有何区别？** |
| SRAM的访问时间通常比DRAM快。DRAM的价格比SRAM低  比SRAM价格低，体积小。  SRAMs generally have faster access times than DRAMs. DRAMS are less  expensive and smaller than SRAMs. |

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| 5.5  **说明为什么一种类型的RAM被认为是模拟设备，而另一种类型的RAM被认为是数字设备？** |
| 一个DRAM单元本质上是一个使用电容器的模拟设备；电容器可以存储一定范围内的任何电荷值；一个阈值决定了电荷是否被解释为1或0。  一个SRAM单元是一个数字设备，在其中使用传统的触发器逻辑门配置存储二进制值。  A DRAM cell is essentially an analog device using a capacitor; the capacitor can store any charge value within a range; a threshold value determines whether the charge is interpreted as 1 or 0.  A SRAM cell is a digital device, in which binary values are stored using traditional flip-flop logic-gate configurations. |

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| 5.6  **试给出ROM的某些应用** |
| 微程序控制单元存储器；常用功能的库子程序；系统程序；功能表。要的功能；系统程序；功能表。  Microprogrammed control unit memory; library subroutines for frequently  wanted functions; system programs; function tables. |

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| 5.7  **EPROM、EEPROM和快闪存储器三者之间有什么不同？** |
| EPROM：在写入操作前，让封装芯片经紫外线擦除所有存储单元。紫外线可擦除，属于芯片级英语翻译。  Before writing, the package chip erases all memory cells by ultraviolet light.  ultraviolet light is erasable belongs to the chip level  EEPROM：可以在任何时候写入而不擦除先前的内容。  Previous content can be written at any time without erasing.  electricity is erasable belongs to the byte level  闪存：在成本和功能上都介于EPROM和EEPROM之间。  和EPROM一样，闪存每比特只使用一个晶体管，但擦除速度比EPROM快。比EEPROM有更高的存储密度。英语翻译。  Both in terms of cost and functionality are somewhere between EPROM and EEPROM. Like EPROM, flash memory uses only one transistor per bit, but erases faster than EPROM. It has a higher storage density than EEPROM.  electricity is erasable belongs to the block level |

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| 5.8  **解释图5-4b中每个引脚的功能**  IMG_20220525_000230 |
| A0 - A10 = 地址线：。CAS = 列地址选择：。D1 - D4 = 数据线。NC: =  无连接。OE：输出使能。RAS=行地址选择：。Vcc：=电压源。  Vss：=接地。WE：写入能。  A0 - A10= address lines:.  CAS = column address select:.  D1 - D4 = data lines.  NC: =no connect.  OE: output enable.  RAS = row address select:.  Vcc = voltage source.  Vss: = ground. WE: write enable. |

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| 5.9  **什么是奇偶校验位？** |
| 附加到二进制数字阵列中的一个位，使所有二进制数字的总和，包括奇偶校验位，总是奇数（奇数校验）或总是偶数（偶数校验）。  A bit appended to an array of binary digits to make the sum of all the binary  digits, including the parity bit, always odd (odd parity) or always even (even  parity). |

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| 6.4  **说明简单的CAV系统与多带记录系统的区别。** |
| 对于恒定角速度（CAV）系统，每条轨道的比特数是恒定的。密度的增加是通过多区记录实现的，在多区记录中，表面被分为若干区，离中心较远的区比离中心较近的区包含更多比特。  For the constant angular velocity (CAV) system, the number of bits per track is  constant. An increase in density is achieved with multiple zoned recording, in  which the surface is divided into a number of zones, with zones farther from the  center containing more bits than zones closer to the center. |

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| 6.9  **简要定义RAID的七个级别** |
| 0: 非冗余  1: 镜像；每个磁盘都有一个包含相同数据的镜像磁盘。  2: 通过汉明码冗余；在每个数据盘的相应位上计算纠错码，并将纠错码的位存储在多个奇偶校验盘的相应位上。  3：位交错奇偶校验；类似于第2级，但不是纠错码，而是为所有数据盘上相同位置的单个位集计算一个简单的奇偶校验位。  4：块状交错奇偶校验；在每个数据盘上的相应条带中逐位计算奇偶校验，奇偶校验位被存储在奇偶校验盘上的相应条带中。  盘。  5：块状交错分布式奇偶校验；与第4级类似，但将奇偶校验条分布在所有的  磁盘。  6：块交错式双分布式奇偶校验；进行两种不同的奇偶校验计算，并存储在不同磁盘的不同块中。    0: Non-redundant  1: Mirrored; every disk has a mirror disk containing the same  data.  2: Redundant via Hamming code; an error-correcting code is calculated  across corresponding bits on each data disk, and the bits of the code are stored in  the corresponding bit positions on multiple parity disks.  3: Bit-interleaved parity;  similar to level 2 but instead of an error-correcting code, a simple parity bit is  computed for the set of individual bits in the same position on all of the data disks.  4: Block-interleaved parity; a bit-by-bit parity strip is calculated across  corresponding strips on each data disk, and the parity bits are stored in the  corresponding strip on the parity disk.  5: Block-interleaved distributed parity;  similar to level 4 but distributes the parity strips across all disks.  6: Block interleaved dual distributed parity; two different parity calculations are carried out  and stored in separate blocks on different disks. |

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| 6.12  **在RAID环境中，并行存取和独立存取有何不同？** |
| 在并行访问阵列中，所有成员磁盘都参与执行每个I/O请求。通常情况下，各个驱动器的主轴是同步的，所以每个磁盘的磁头在任何时候都处于每个磁盘的相同位置。在独立访问阵列中，每个成员盘都独立运行，所以单独的I/O请求可以被并行满足。  In a parallel access array, all member disks participate in the execution of every I/O request. Typically, the spindles of the individual drives are synchronized so that each disk head is in the same position on each disk at any given time. In an independent access array, each member disk operates independently, so that separate I/O requests can be satisfied in parallel. |

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| 6.14  **什么原因造成DVD比CD有更大的盘容量？** |
| 1. 在DVD上，比特被包装得更紧密。CD上螺旋线的环间距是1.6μm，沿螺旋线的凹坑之间的最小距离是0.834μm。DVD使用波长更短的激光器，实现了0.74微米的环形间距和0.4微米的凹坑之间的最小距离。这两项改进的结果是容量增加了约7倍，达到约4.7GB。  2. DVD采用了第二层凹坑，并在第一层之上着陆 双层DVD在反射层之上有一个半反射层，通过调整焦点，DVD驱动器中的激光器可以分别读取每一层。这种技术几乎使磁盘的容量增加了一倍，达到约8.5GB。第二层的反射率较低，限制了它的存储容量，因此无法实现完全翻倍。  3. DVD-ROM可以是两面的，而数据只记录在CD的一面。这使得总容量达到了17GB。  1. Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 μm and a minimum distance between pits of 0.4 μm. The result of these two improvements is about a seven-fold increase in capacity, to about 4.7 GB.  2. The DVD employs a second layer of pits and lands on top of the first layer A dual-layer DVD has a semireflective layer on top of the reflective layer, and by adjusting focus, the lasers in DVD drives can read each layer separately. This technique almost doubles the capacity of the disk, to about 8.5 GB. The lower reflectivity of the second layer limits its storage capacity so that a full doubling is not achieved.  3. The DVD-ROM can be two sided whereas data is recorded on only one side of CD. This brings total capacity up to 17 GB. |

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| 7.1  **列出外设或外围设备的三种主要分类。** |
| 人类可读。适用于与计算机用户交流。机器可读。适用于与设备通信。通信。适用于与远程设备的通信  Human readable: Suitable for communicating with the computer user.  Machine readable: Suitable for communicating with equipment.  Communication: Suitable for communicating with remote devices |

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| 7.2  **什么是国际参考字母表（IRA）？** |
| 最常用的文本代码是国际参考字母表（IRA），其中每个字符由一个独特的7位二进制代码表示；因此，可以表示128个不同的字符。  The most commonly used text code is the International Reference Alphabet (IRA), in which each character is represented by a unique 7-bit binary code; thus, 128 different characters can be represented. |

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| 7.3  **I/O模块的主要功能是什么？** |
| 控制和计时。处理器通信。设备通信。数据缓冲。错误检测。  Control and timing. Processor communication. Device communication. Data buffering. Error detection. |

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| 7.4  **列出并简单定义实现I/O的三种技术。** |
| 编程式I/O。处理器代表一个进程向一个I/O模块发出I/O命令；然后该进程忙于等待操作完成后再继续。  中断驱动的I/O。处理器代表一个进程发出一个I/O命令，继续执行后续指令，当I/O模块完成其工作时，被I/O模块打断。后续指令可以在同一进程中，如果该进程没有必要等待I/O的完成。否则，该进程将被暂停，等待中断并执行其他工作。直接内存访问  (DMA)。一个DMA模块控制主存储器和I/O模块之间的数据交换。处理器向DMA模块发送一个数据块的传输请求，只有在整个数据块被传输后才会中断。  Programmed I/O: The processor issues an I/O command, on behalf of a process, to an I/O module; that process then busy-waits for the operation to be completed before proceeding.  Interrupt-driven I/O: The processor issues an I/O command on behalf of a process, continues to execute subsequent instructions, and is interrupted by the I/O module when the latter has completed its work. The subsequent instructions may be in the same process, if it is not necessary for that process to wait for the completion of the I/O. Otherwise, the process is suspended pending the interrupt and other work is performed. Direct memory access  (DMA): A DMA module controls the exchange of data between main memory and an I/O module. The processor sends a request for the transfer of a block of data to the DMA module and is interrupted only after the entire block has been transferred. |

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| 7.5  **存储器映射式I/O与分离式I/O有什么区别？** |
| 有了内存映射的I/O，内存位置和I/O设备就有了一个单一的地址空间。处理器将I/O模块的状态和数据寄存器视为内存位置，并使用相同的机器指令来访问内存和I/O设备。在隔离的I/O中，一个命令指定了地址是指内存位置还是指I/O设备。  地址是指一个内存位置还是一个I/O设备。全部的地址范围可能对两者都可用。  With memory-mapped I/O, there is a single address space for memory locations and I/O devices. The processor treats the status and data registers of I/O modules as memory locations and uses the same machine instructions to access both memory and I/O devices. With isolated I/O, a command specifies whether the  address refers to a memory location or an I/O device. The full range of addresses may be available for both. |

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| 7.6  **当设备出现中断时，处理器如何知道是那、哪个设备发出的中断？** |
| 常用的技术一般有四类：多条中断线；软件轮询；菊花链（硬件轮询，有节制）；总线仲裁（有节制）。  Four general categories of techniques are in common use: multiple interrupt lines ; software poll; daisy chain (hardware poll, vectored); bus arbitration (vectored). |

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| 7.7  **DMA模块取得总线控制权并占用了总线时，处理器做什么？** |
| 处理器在DMA模块盗用的每个总线周期中都会暂停。  The processor pauses for each bus cycle stolen by the DMA module. |