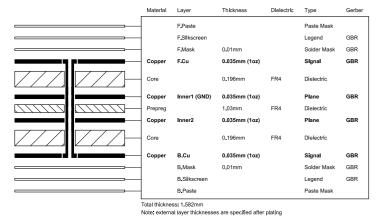
# **Watch-DevKit-HW Fabrication Document**

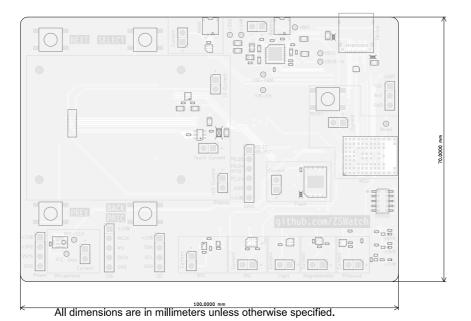
#### **Layer Stack Legend**



### **Impedance Table**

Transmission Line | Impedance [ohms] | Tolerance [%] | Layer | Trace Width [mm] | Gap [mm] | Ref. Layers

## **Top Fabrication (Scale 1:1)**



FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.

DIMENSIONS OF CIRCUMSIZED RECTANGLE SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

- 4) SURFACE FINISH: HAL LEAD-FREE
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR WHITE.
- SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING BLACK NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
- 9) PCB MATERIAL REQUIREMENTS:
- FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
   B. Tg 150 C OR EQUIVALENT.

#### 10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

100.000 × 70.000 mm 1.582 mm 0.127 mm 0.125 mm 0.250 mm 0.650 mm 0.100 mm 0.125 mm 0.125 mm BOARD SIZE
BOARD THICKNESS
TRACE WIDTH
TRACE TO TRACE
MIN. HOLE (PTH)
MIN. HOLE (NPTH)
ANNULAR RING
COPPER TO HOLE
COPPER TO EDGE
HOLE TO HOLE

Variant: Git Hash: Company: ZSWatch ZSWatch CHECKED 2c23067 Board Name: Watch-DevKit-HW ZSWatch Watch-DevKit Sheet Title: File Name: Designer: Date: Revision: Top Fabrication (Scale 1:1) ZSWatch-Watch-DevKit.kicad\_pcb 2025-07-13 1.1.0+ (Unreleased) Daniel Kampert Sheet Path: Size: **A3** of 10

