VLSI Lab

LABORATORY MANUAL

Spring 2019

LAB 07

Title of Lab Experiment: Implementation of Transmission Gate Circuits Layout using available CAD Tools

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STUDENT NAME	ROLL NO	SEC

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LAB ENGINEER SIGNATURE & DATE

MARKS AWARDED: /10

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LAB:	07	Implementation of Transmission Gate Circuits Layout using available CAD Tools

1. Learning Objectives:

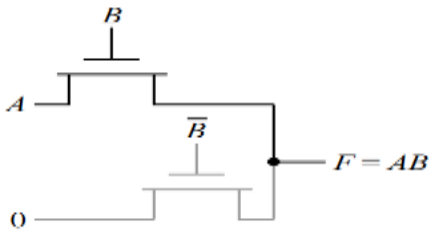
a. Transmission Gate circuits
b. Layout design using Transmission Gate.

2. Equipment Required:

Software : L-Edit

3. Introduction:

Pass Transistor Logic



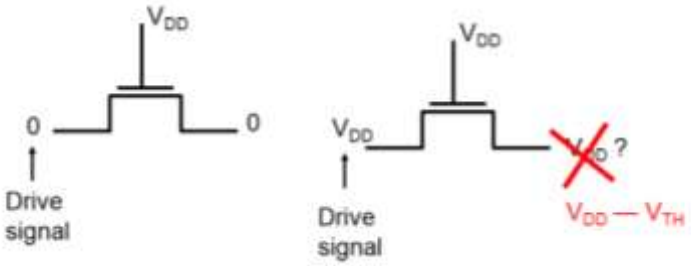
When B is “1”, top device turns on and copies the input A to output F. When B is low, bottom device turns on and passes a “0”. The presence of the switch driven by B is essential to ensure that the gate is static – a low-impedance path must exist to supply rails.

Adv.: Fewer devices to implement some functions. Example: AND2 requires 4 devices (including inverter to invert B) vs. 6 for complementary CMOS (lower total capacitance). NMOS is effective at passing a 0, but poor at pulling a node to Vdd. When the pass transistor a node high, the output only charges up to Vdd-Vtn.

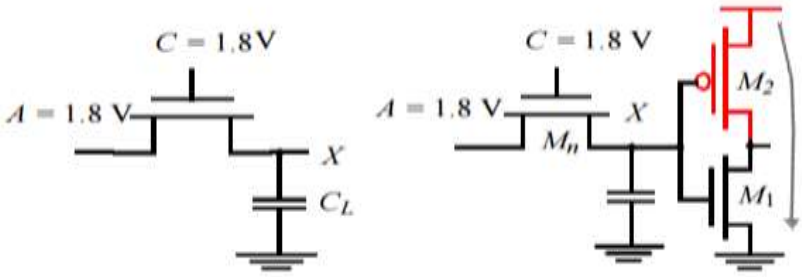
Issues with pass transistor

1) Signal Degradation

There must be at least V_{TH} between the gate and source for NMOS to conduct: What does it mean ?



2)Static power loss



V_X does not pull up to 1.8V, but 1.8V - V_{TN}
Threshold voltage loss causes static power consumption

Transmission Gate Logic

A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a pMOS transistor and nMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off.

When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is a Logic 0, the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes.

The schematic diagram (Figure 1) includes the arbitrary labels for IN and OUT, as the circuit will operate in an identical manner if those labels were reversed. This design provides true bidirectional connectivity without degradation of the input signal.

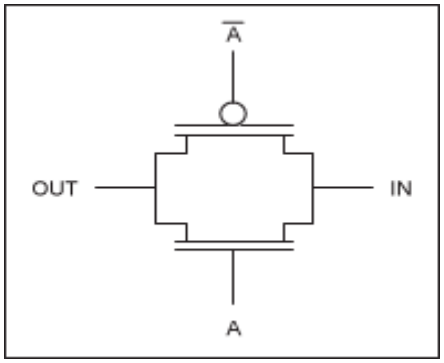


Figure 1. Schematic representation of a transmission gate.

The common circuit symbol for a transmission gate depicts the bidirectional nature of the circuit's operation (Figure 2).

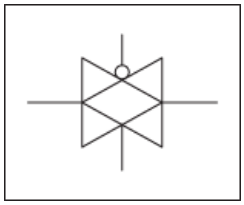
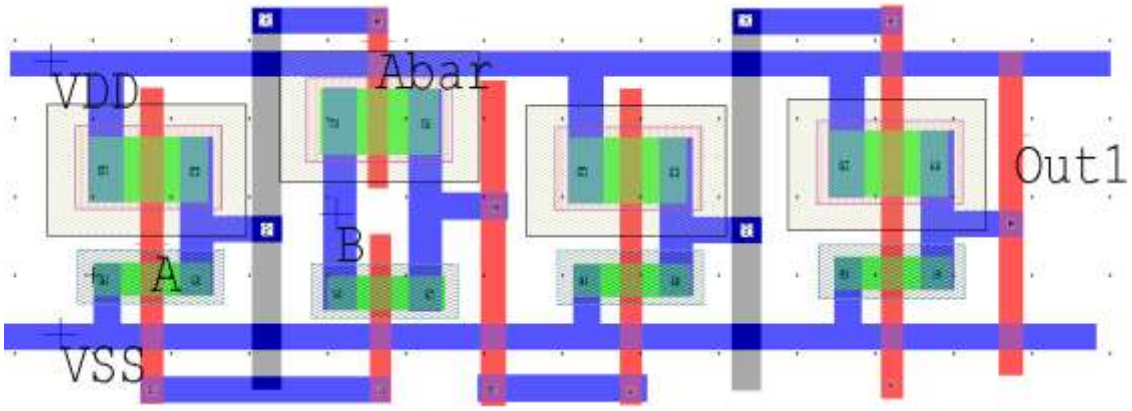


Figure 2. Circuit symbol.

4. Procedure :

Transmission gate AND.

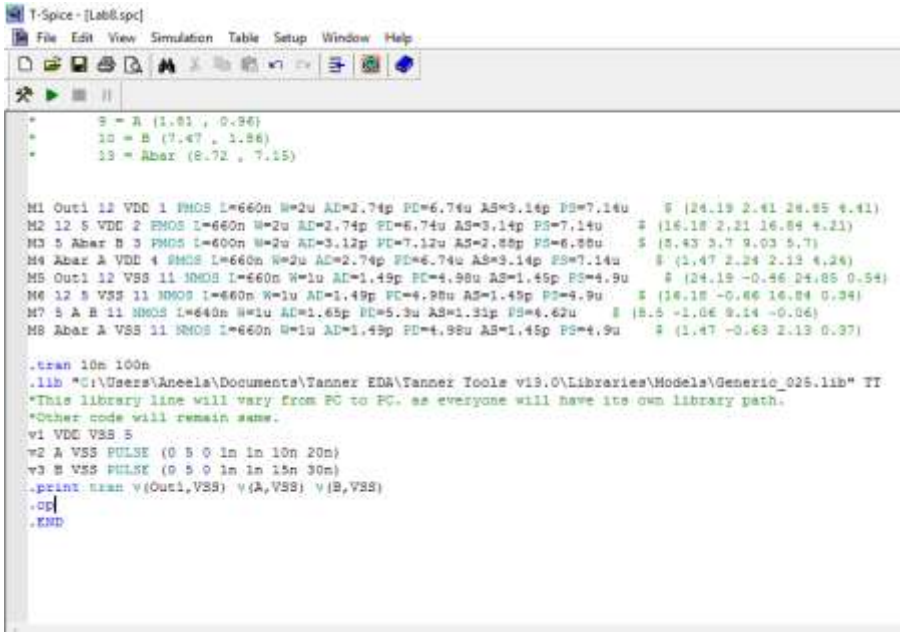
Layout



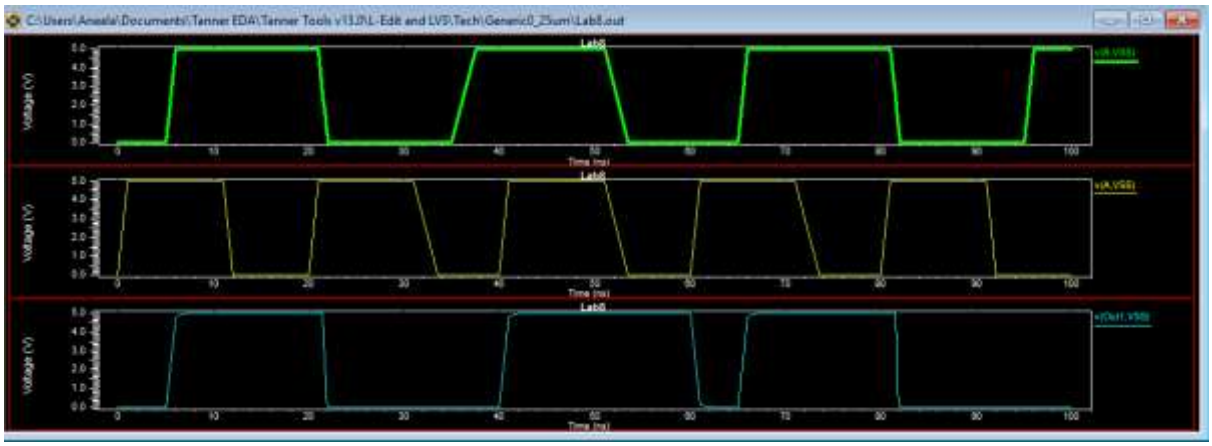
Metal 2 and **Metal 1** are connected using **via1** contact. Dimension of via1 Contact is **0.36x0.36** in Microns.

Please note that Metal 2 cannot be directly connected through Polysilicon.

Layout Spice file:



Layout Simulations results:



5. Task :

Students with odd last digit of Student ID: Make layout of XNOR using Transmission gate.
Students with even last digit of Student ID: Make layout of XOR using Transmission gate.

Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

_____

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Student's signature and Date

Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)
  _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission
  _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed?
  _____/10
- ☐ **TOTAL:**
  _____/50

Feedback on student behaviour:

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2

- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2
- ☐ Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

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Lab Engineer's signature and Date

Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisified
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedabck is for LAB session: LAB Number: _____, Date: _____
- ☐ General (to provide feedback on a persistent practice/ocurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

This feedback is:

- ☐ For a Particular
- ☐ Who conducted the LAB? _____
- ☐ Actual Start time: _____ Total Duration of Lab: _____
- ☐ Instruction Duration: _____ Practical Duration: _____
- ☐ LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE

- Had the theory related to lab been covered in theory class? Yes/No

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

Instruction Session	Was duration of instruction session adequate?	-2	-1	0	+1	+2
	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
Staff	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2
	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
Equipment	Performance of Electronic Instruments?	-2	-1	0	+1	+2
	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2
	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

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