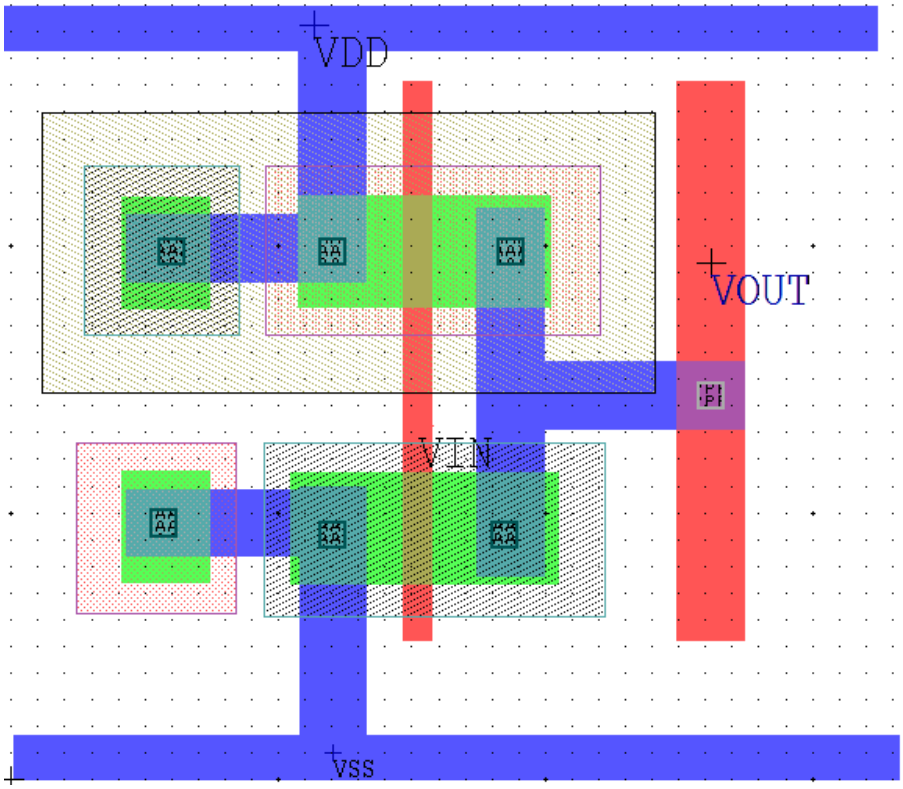
# Inverter Layout Designing and Testing

## Design Step:

Design inverter layout by following the steps provided in lab 4 Manual.

(I have uploaded inverter Layout as well.)

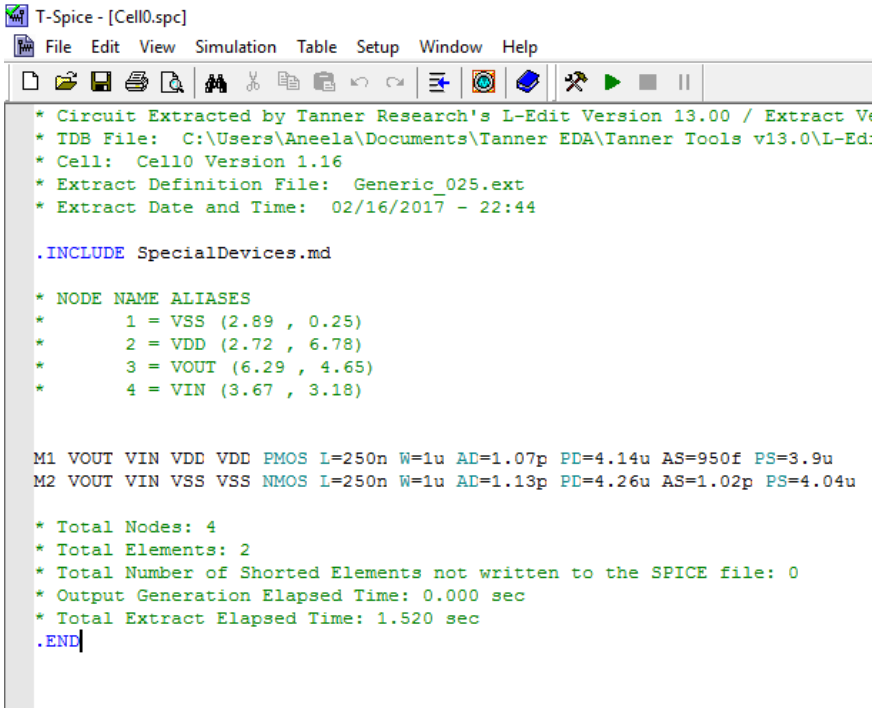



To test the inverter you have to extract a spice file from the layout file. Before this make sure that the labels (VDD, VSS, VIN and VOUT) are assigned to correct masks.

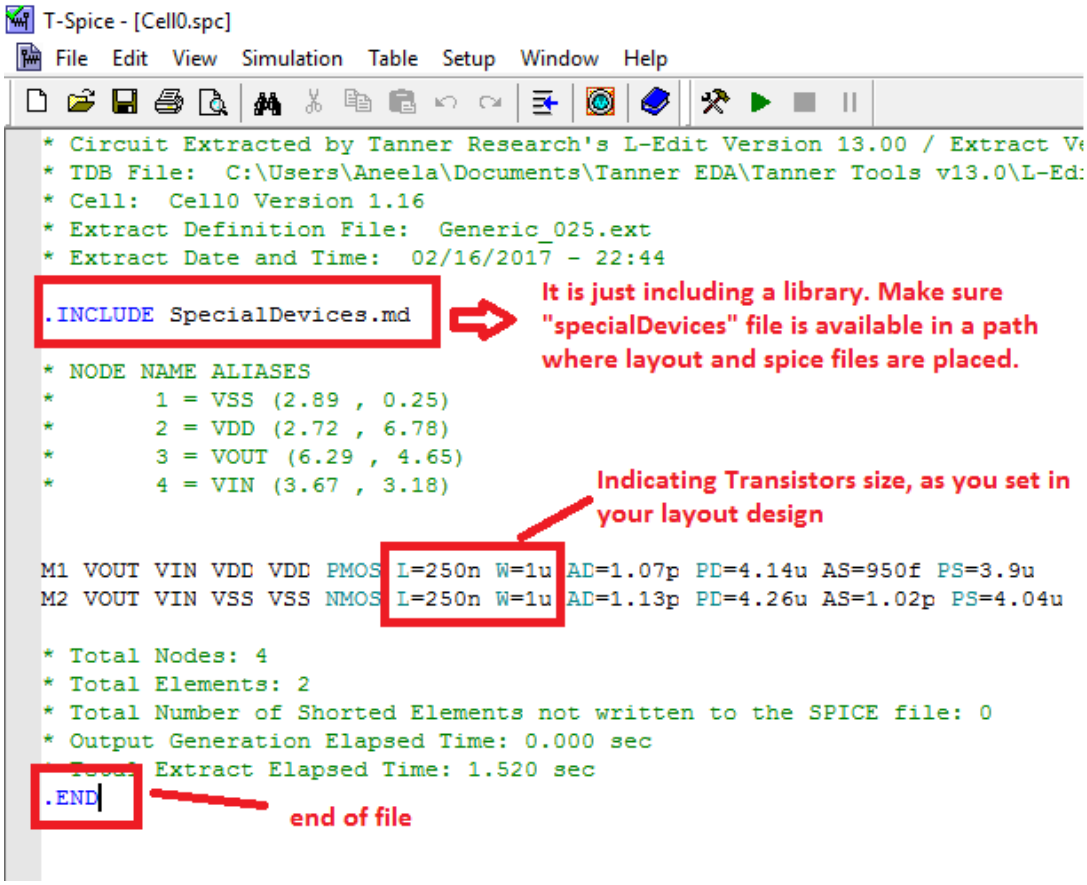
**VSS and VDD connected on Metal1**

**VOUT and VIN connected on Poly**

Once you have extracted a file named Cell0.spc will be created. Open this file, you will get a window like this:




The question here is what is meant by given lines of code? And what do we need to do in this file to test our inverter? You will find answers here in a few lines later…



**How to test the inverter?**

You have to write code to test your inverter. Now there are two different ways of writing the code.

1. Using “insert command” technique as you did in Lab 4.
2. Write code directly into your spice file as shown in figure below.

```
.INCLUDE SpecialDevices.md

* NODE NAME ALIASES
*       1 = VSS (2.89 , 0.25)
*       2 = VDD (2.72 , 6.78)
*       3 = VOUT (6.29 , 4.65)
*       4 = VIN (3.67 , 3.18)


M1 VOUT VIN VDD VDD PMOS L=250n W=1u AD=1.07p PD=4.14u AS=950f PS=3.9u    $ (3.53 4.25 3.78 5.25)
M2 VOUT VIN VSS VSS NMOS L=250n W=1u AD=1.13p PD=4.26u AS=1.02p PS=4.04u    $ (3.53 1.76 3.78 2.76)

* Total Nodes: 4
* Total Elements: 2
* Total Number of Shorted Elements not written to the SPICE file: 0
* Output Generation Elapsed Time: 0.000 sec
* Total Extract Elapsed Time: 1.520 sec

.tran 10n 100n
.lib "C:\Users\Aneela\Documents\Tanner EDA\Tanner Tools v13.0\Libraries\Models\Generic_025.lib" TT
v1 VDD VSS 5
v2 VIN VSS PULSE (0 5 0 1n 1n 10n 30n)
.print tran v(VOUT,VSS) v(VIN,VSS)

.END
```

**<u>What is meant by individual code line?</u>**

**.tran 10n 100n**

This is the most important line of your code to plot the waveform. If you miss this line, you won’t be able to see your waveform into W-Edit software. In this command **.tran** means transient response. **100n** means total simulation time. **10n** means step size.

If you miss above command, you will not get any error, but when you will run this file, nothing will be displayed as an output.

**.lib "C:\Users\Aneela\Documents\Tanner EDA\Tanner Tools v13.0\Libraries\Models\Generic_025.lib" TT**

This is the library file that is used to define Transistors (NMOS, PMOS) definitions. If you missed this line in your code, you will get an error like this:

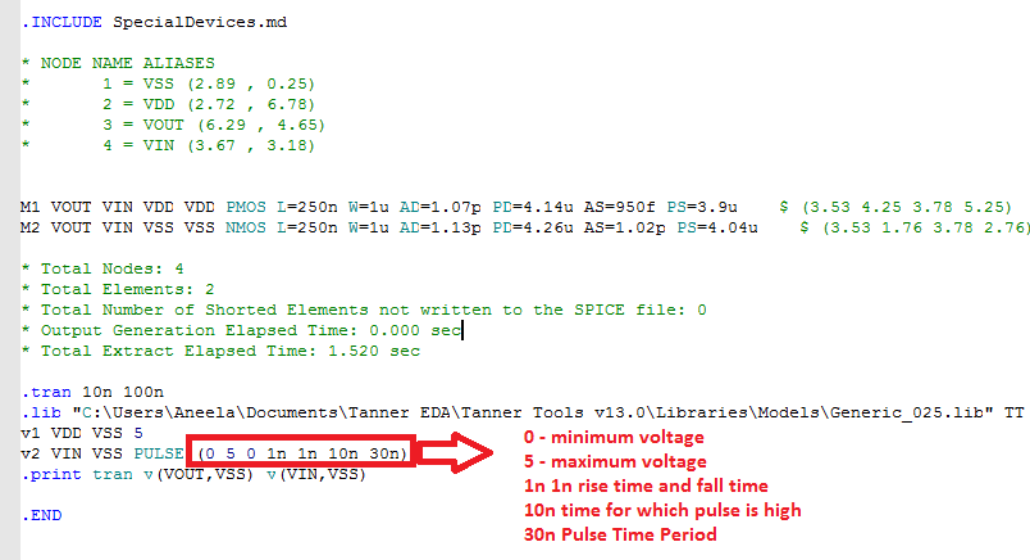
```
Fatal Error : "Cell0.spc" line 25 Missing MOSFET model definition for "PMOS"
 : Referenced by device(s):
 :    M1


Parsing                     0.00 seconds
Setup                       0.00 seconds
Overhead                    3.17 seconds
-----------------------------------------
Total                       3.17 seconds

Simulation failed with  1 Fatal Error
```

**v1 VDD VSS 5**

This line is defining a constant voltage that is VDD and GND. **v1** is just a variable name. VDD and VSS means positive and negative voltages. 5 means maximum voltage i.e. VDD here.

**v2 VIN VSS PULSE (0 5 0 1n 1n 10n 30n)**

v2 is again a variable name. VIN is input name. It should be same as provided in your layout input name. PULSE mean you are providing pulse as in input.




**.print tran v(VOUT,VSS) v(VIN,VSS)**

Command to display the output. Put all input and output names here that you want to see n W-Edit.

## Complete Code:

. .tran 10n 100n

.lib "C:\Users\Aneela\Documents\Tanner EDA\Tanner Tools v13.0\Libraries\Models\Generic_025.lib" TT

*Above library line will vary from PC to PC. As everyone will have its own library path.

*Other code will remain same.

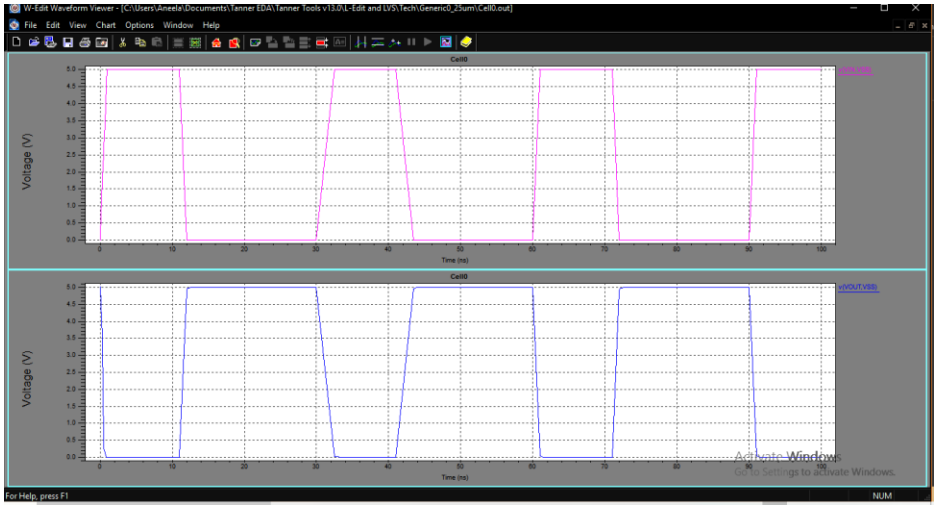
v1 VDD VSS 5

v2 VIN VSS PULSE (0 5 0 1n 1n 10n 30n)

.print tran v(VOUT,VSS) v(VIN,VSS)

.END

Once you have written all the commands, you can run to check the simulation.




That’s it ☺