VLSI Lab

LABORATORY MANUAL

Spring 2019

LAB 02

Title of Lab Experiment : Gate and Transistor Level

Implementation of Boolean expressions using DSCH

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STUDENT NAME ROLL NO SEC

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LAB ENGINEER SIGNATURE & DATE

MARKS AWARDED: /10

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LAB:	02	Gate and Transistor Level Implementation of Boolean expressions using DSCH

1. Learning Objectives:

a. Gate level implementation of Boolean expressions.
b. Transistor level implementation of Boolean expressions.

2. Equipment Required:

Software : Dsch v2

3. Introduction:

1) Boolean Expressions

A **Boolean expression** is an expression that results in a Boolean value, that is, in a value of either **true** or **false**

Examples:

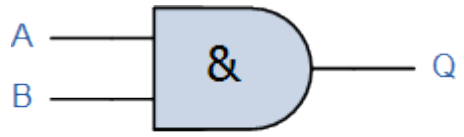
Z = Output A,B = Inputs

Z = A + B OR
Z = A . B AND
Z = ~ A NOT

2) Gate Level Implementation :

2-input AND Gate

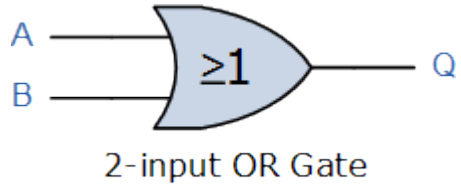
For a 2-input AND gate, the output Q is true if BOTH input A "AND" input B are both true, giving the Boolean Expression of: (Q = A and B).

Symbol	Truth Table		
 2-input AND Gate	A	B	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A.B	**Read as A AND B gives Q**		

Note that the Boolean Expression for a two input AND gate can be written as: A.B

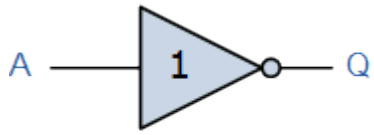
2-input OR (Inclusive OR) Gate

For a 2-input OR gate, the output Q is true if EITHER input A "OR" input B is true, giving the Boolean Expression of: (Q = A or B).

Symbol	Truth Table		
 2-input OR Gate	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression Q = A+B	**Read as A OR B gives Q**		

NOT Gate

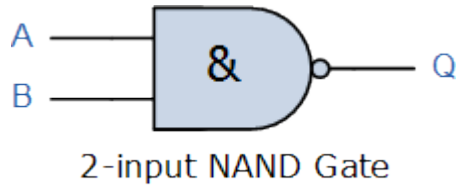
For a single input NOT gate, the output Q is ONLY true when the input is “NOT” true, the output is the inverse or complement of the input giving the Boolean Expression of: (Q = NOT A).

Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0
Boolean Expression Q = NOT A or A	**Read as inversion of A gives Q**	

The NAND and the NOR Gates are a combination of the AND and OR Gates with that of a NOT Gate or inverter.

2-input NAND (Not AND) Gate

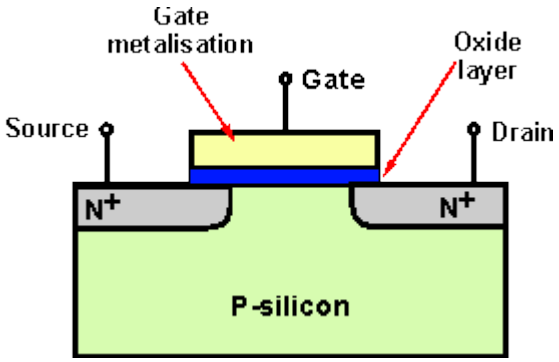
For a 2-input NAND gate, the output Q is true if BOTH input A and input B are NOT true, giving the Boolean Expression of: (Q = not(A and B)).

Symbol	Truth Table		
 2-input NAND Gate	A	B	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A .B	**Read as A AND B gives NOT-Q**		

3) Transistor Level Implementation

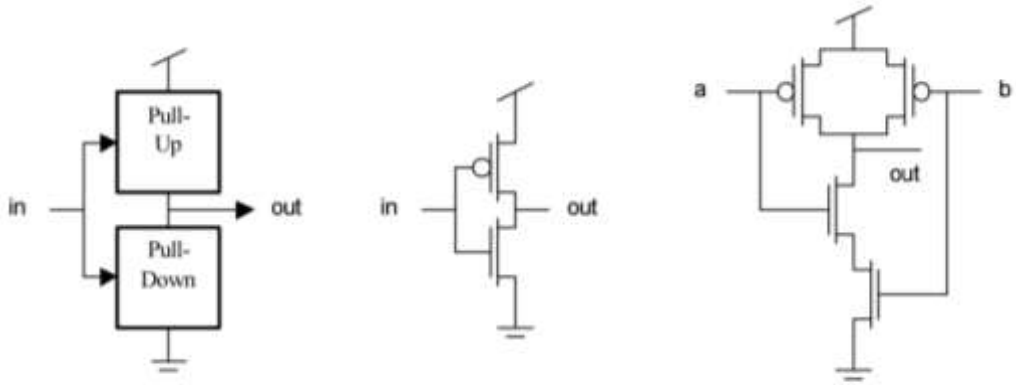
- MOS transistor:

The key factor of the MOSFET is the fact that the gate is insulated from the channel by a thin oxide layer. This forms one of the key elements of its structure. For an N-channel device the current flow is carried by electrons and in the diagram below it can be seen that the drain and source are formed using N+ regions which provide good conductivity for these regions.



- CMOS Technology

A typical static CMOS gate is built of two complementary networks: · A pull-down network composed of NMOS, with sources connected to GND · A pull-up network composed of PMOS, with sources connected to VDD



Generic CMOS gate Inverter NAND

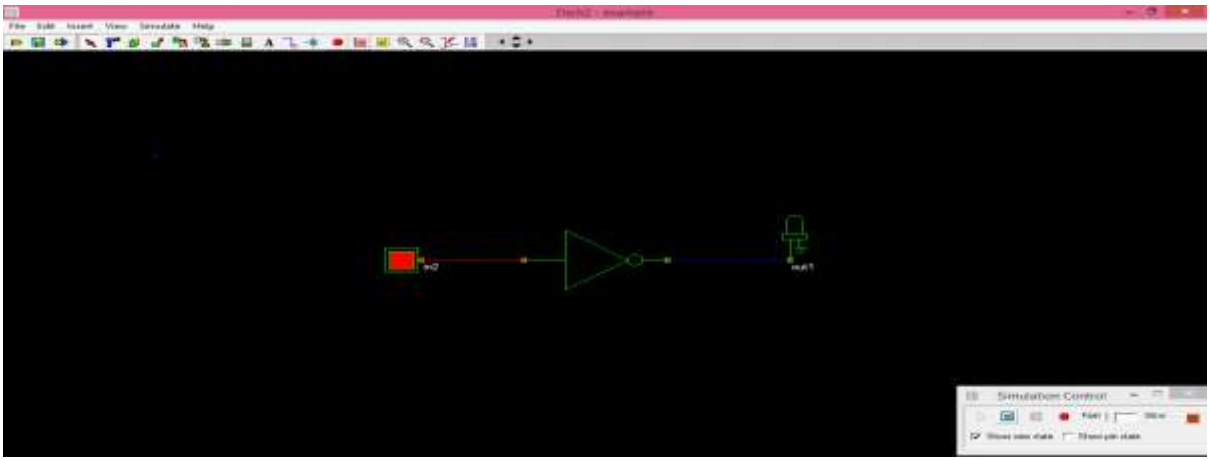
4. Procedure:

Designing simple inverter using Dsch v2.

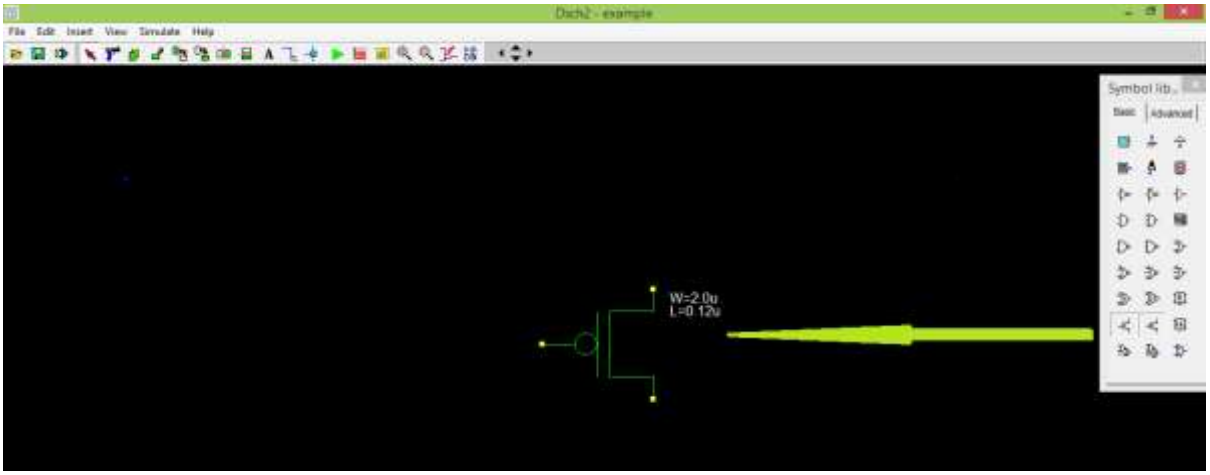
Steps:

1) Run Dsch software
2) Select Foundry -> CMOS025

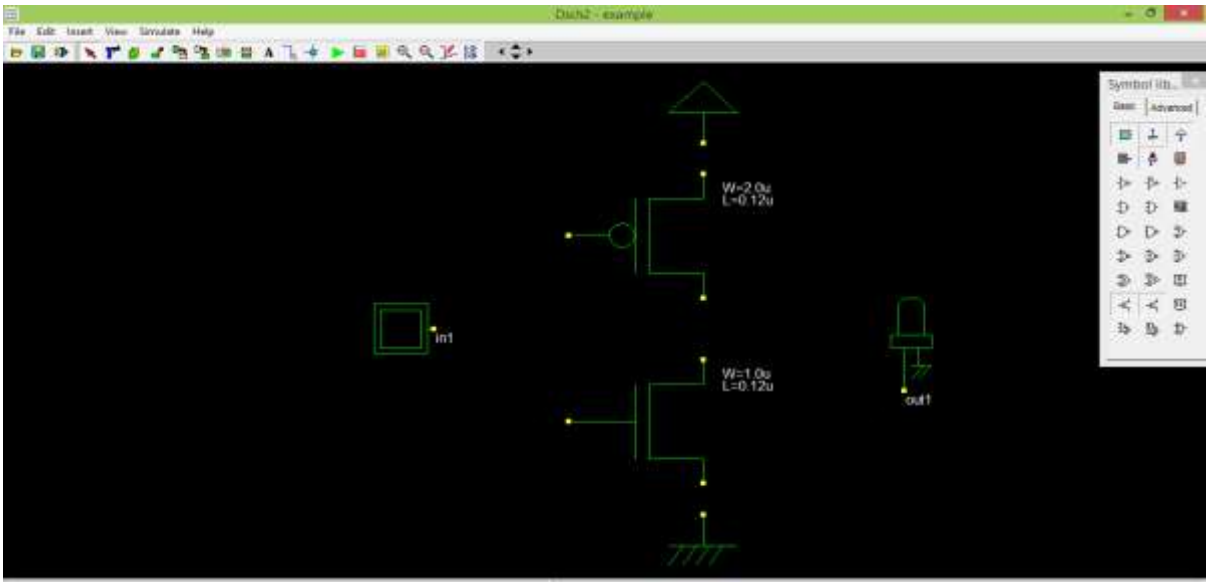
3) Implement NOT gate level circuit.



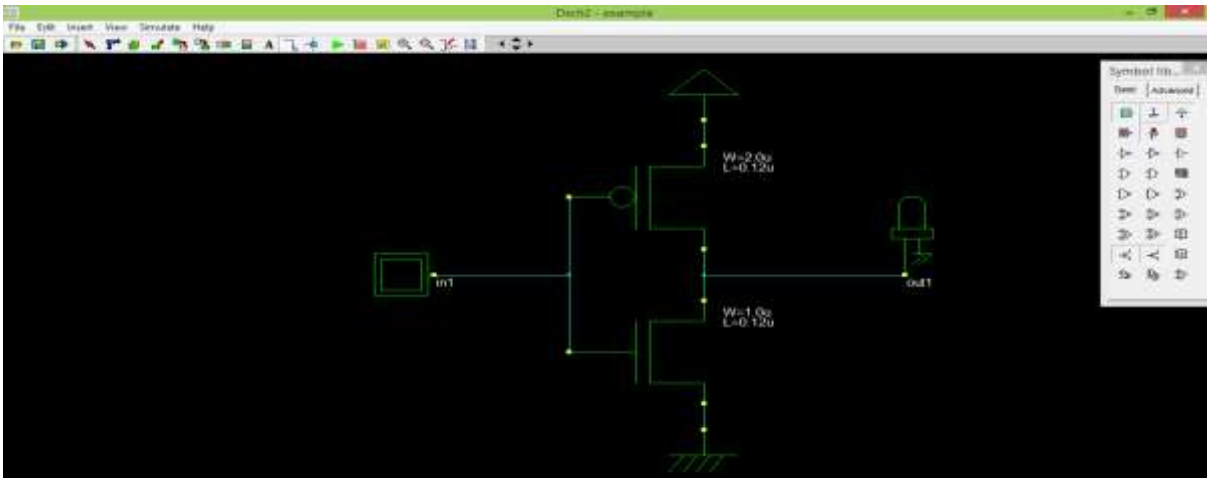
4) Now Transistor level implementation.Drag and Drop transistor.



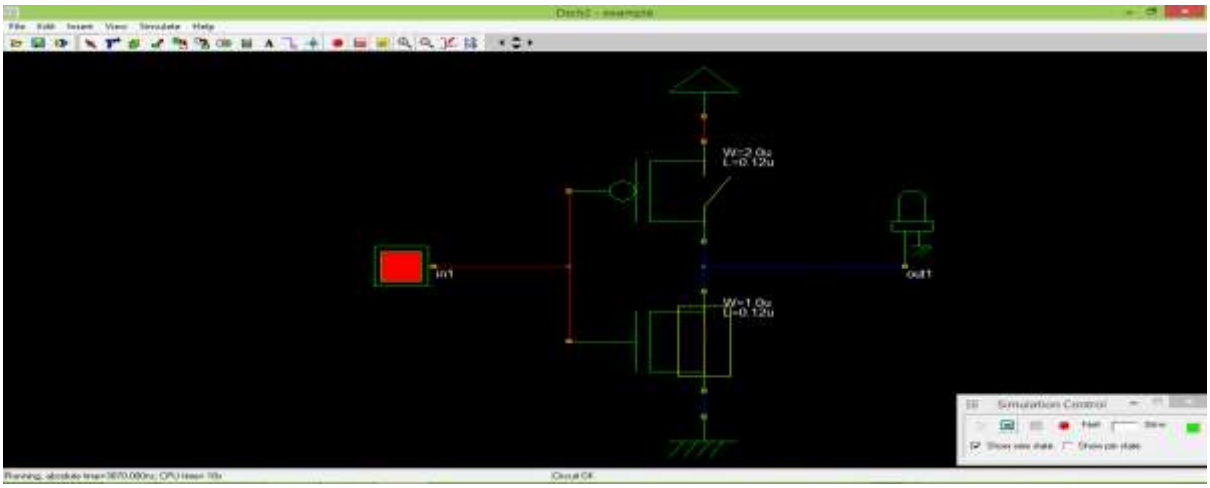
5) Similarly Place other components required for an inverter. (e.g PMOS,NMOS,VDD,GND,LED,BUTTON)

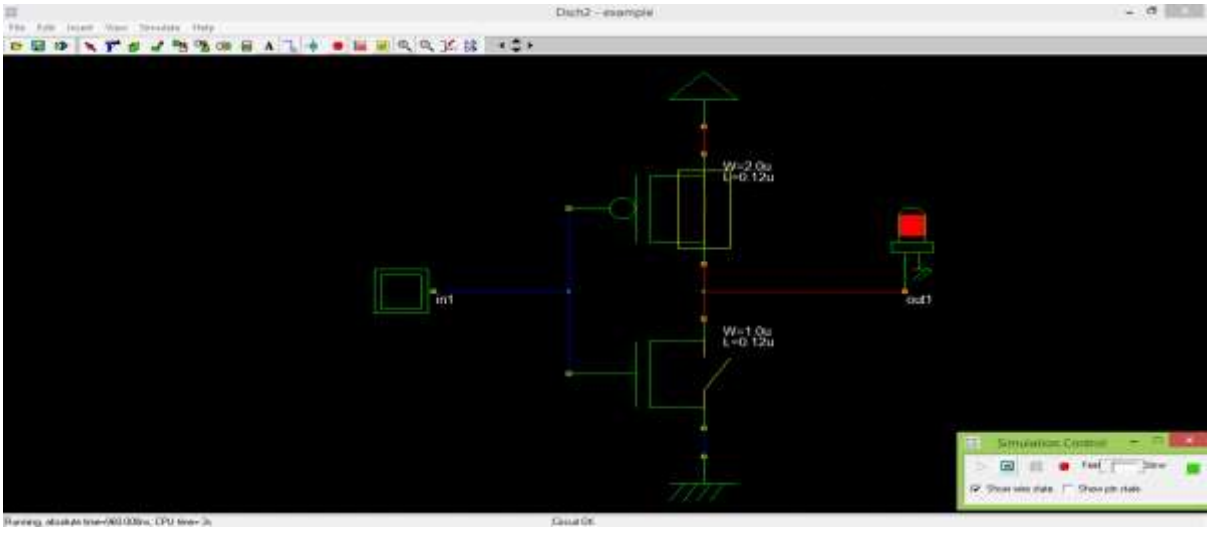


6) Now click on “ADD A LINE” and make connections between components.

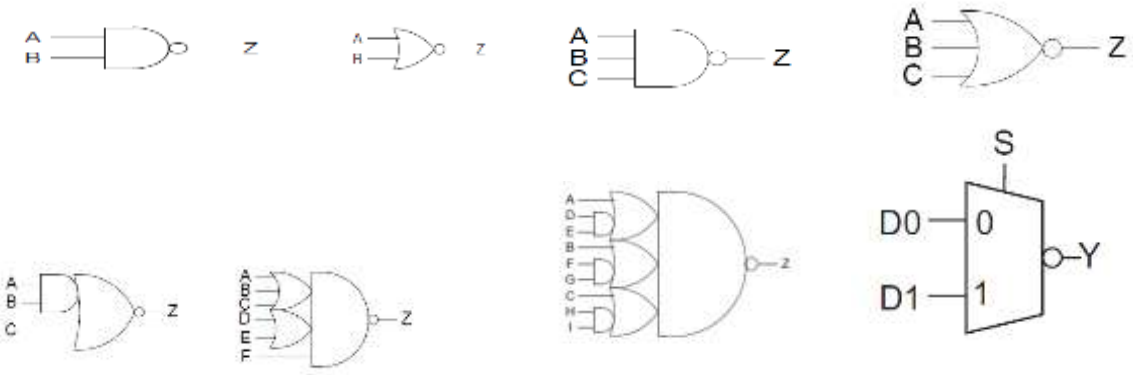


7) Press " RUN SIMULATION" button and verify the working of circuit.(Relationship between input/output)





5. **Tasks:**
   Write Boolean expression of following Gates and implement transistor level diagrams using CMOS Logic in Dsch software.



Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

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Student's signature and Date

Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)
  _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission
  _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed?
  _____/10
- ☐ **TOTAL:**
  _____/50

Feedback on student behaviour:

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2

- Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

_____

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Lab Engineer's signature and Date

Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- Providing feedback for every lab session is optional. No feedback means you are satisified
- The Lab Committee will consider only duly filled forms submitted within one week after the lab
- This feedabck is for LAB session: LAB Number: _____, Date: _____
- General (to provide feedback on a persistent practice/ocurrence in LABs).
- Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

This feedback is:

- For a Particular
- Who conducted the LAB? _____
- Actual Start time: _____ Total Duration of Lab: _____
- Instruction Duration: _____ Practical Duration: _____
- LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- Had the theory related to lab been covered in theory class? Yes/No

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

Instruction Session	Was duration of instruction session adequate?	-2	-1	0	+1	+2
	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
Staff	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2
	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
Equipment	Performance of Electronic Instruments?	-2	-1	0	+1	+2
	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2
	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

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