

## EL309 VLSI LAB

### ASSIGNMENT #1

Marks: 100

Assignment start date: 13-03-2019

Assignment Deadline: 27-03-2019 @ in lab

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You are required to search and write a formal technical report, not more than 5 pages, on the following topic:

**Topic: Design Rules Check (DRC) Errors**

Your report should include:

- (1) Name of at-least 25 different DRC errors which commonly occur during digital ICs layout design
- (2) A brief description of each DRC error/Reason why does a specific DRC error occur?  
It is essential to use the sketch of layouts to explain a DRC error.
- (3) How to eliminate these DRC errors in layout?

### Submission

- Write a formal technical report not more than 5 pages long. Please remember I am not looking for a type of the report you submit in your labs. **I want a proper technical report, else you will get nominal marks. Learn how to write a technical report.**
- The report should be **type-written**. Hand written assignments will not be accepted.
- Include references for your work in **IEEE format**. Please learn how to provide references in IEEE format.
- There will be a **plagiarism check for the assignment via plagiarism software**. Following formula will be used for marking of the plagiarised assignments:

If (Plagiarism  $\leq$  20 %)

Deduction = 0 marks; normal grading

else

Deduction = 100 marks; 0 mark will be awarded

- Please learn how does **plagiarism software work?**
- Hard and soft copies of the assignment report are required, soft copies in the assignment section of slate and hard copies in the lab.
- **Your report submitted on slate should not include any scanned text/comment/derivation/mathematical formula. Only scan version of figures and circuits (if any) is allowed.**
- In case of any query related to the assignment, you are welcome to email me ([rashid.karim@nu.edu.pk](mailto:rashid.karim@nu.edu.pk)) or visit my office.