# VLSI Lab

# LABORATORY MANUAL

## Spring 2019


# LAB 04

## Title of Lab Experiment : Layout design of inverter using L-Edit

## Engr. Rashid Karim

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STUDENT NAME ROLL NO SEC

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LAB ENGINEER SIGNATURE & DATE

**MARKS AWARDED: /10**

**NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD**

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|---|---|---|---|
| Prepared by: | Engr. Furqan Mehmood | Version: | 2.00 |
| Last Edited by: | Engr. Aneela Sabir | Date: | 18 Feb,2019 |
| Verified by: | Engr. Rashid Karim. | | |

| LAB: | 04 | Layout design of inverter using L-Edit |
|---|---|---|

# 1. Learning Objectives:

a. Software learning L-Edit.
b. Implementing Layout of CMOS Inverter.
c. Extracting Spice file from the Layout.
d. Testing Inverter using Spice File

# 2. Equipment Required:

Software : L-Edit , T-Spice, W-Edit

# 3. Introduction:

Tanner EDA's L-Edit Pro meets your needs by combining the fastest rendering available with powerful features that exceed the needs of the most demanding user. This leading analog/mixed signal IC design tool enables you to get started with minimal training. You can draw and edit quickly, with fewer keystrokes and mouse clicks than other layout tools. Using powerful features such as interactive DRC, you can work more efficiently to save time and money. L-Edit includes L-Edit for layout editing, Interactive DRC for real-time design rule checking during editing, Standard DRC for hierarchical DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic.

# 4. Procedure :

## Create your layout for the CMOS inverter

- Technology**:** 0.25um CMOS

- All transistor fixed sizes

  Ln = Lp = 0.25um
  Wp = Wn = 1um
  Poly Contact – (To connect Metal 1 and Poly) = 0.24x0.24um
  Active Contact – (To connect Metal1 and Active Area) = 0.24x0.24um
  Power Rails (Vdd and Gnd) = 0.4um
  For Routing, use Metal1 and keep its dimension to be minimum.

**NMOS Layout Design**

The process that we are using is N-well CMOS. This means that the blank screen you see is p-type silicon. We explicitly draw active regions on the screen to open up the field-oxide to insert diffusion regions. This means you can think of the screen as p-type silicon with FOX everywhere on it to begin with. In order to create the NMOS structure, we use three layers:

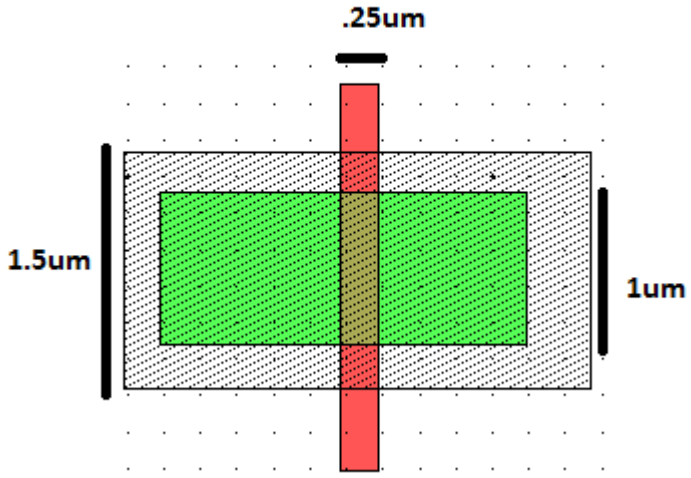
| | |
|---|---|
| Active | - This tell the process where to implant the n-type ions (P or As). Remember that we want to implant into the Poly to reduce its resistance. The "Width" of the N-Select dictates the width of the transistor (Wn) |
| N-Select | - This layer tell where the field-oxide should be opened up for the active regions. This layer must overlay the active region. |
| Poly | - This specifies the gate of the device. Under the poly will be thin oxide forming MOS structure. The "Length" of the Poly dictates the length of transistor (Ln). |

Display Notes

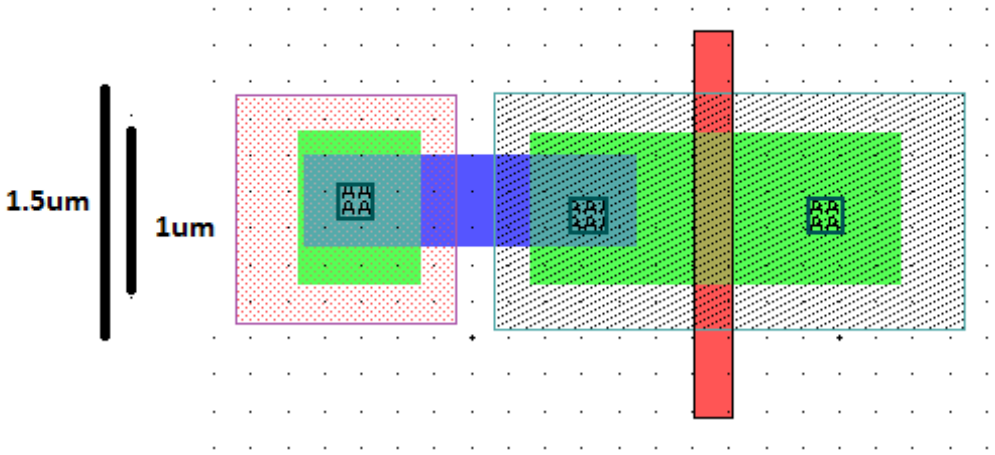
- You can setup the default units to use (micron vs. lambda) in the upper corner of the screen.
- You can setup the grid display and snap using the “Setup – Design” menu and “Grid” tab

Design Steps for NMOS Layout:

1- Place a ploy line of .25um width. You can keep hight of your own choice.
2- Place active area and then N Select according to given dimensions.
3- Check DRC after each step.

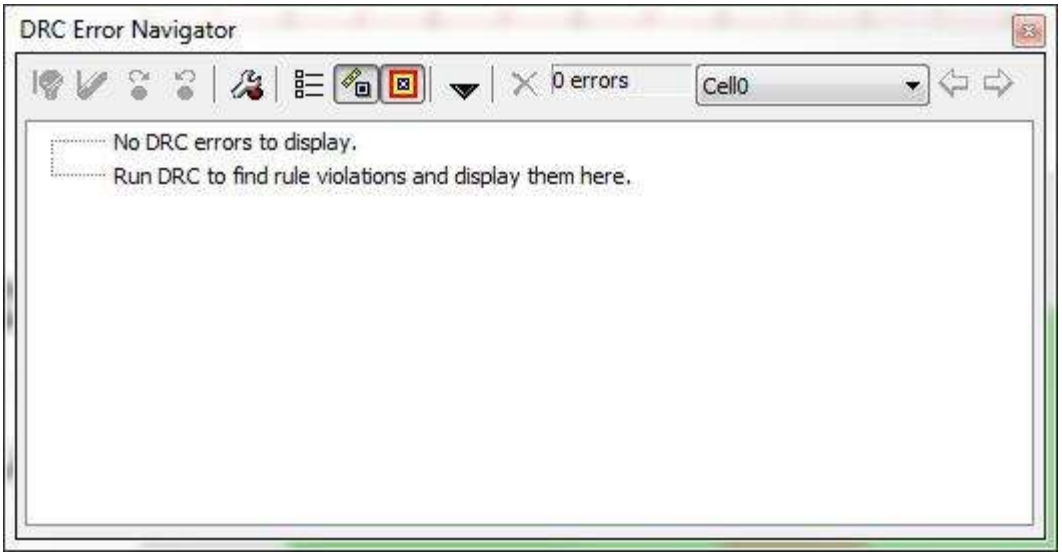



After Drawing Source and drain , next step is to draw substrate.
Use metal1 and draw active contacts of .24x.24 size to connect substrate and source.

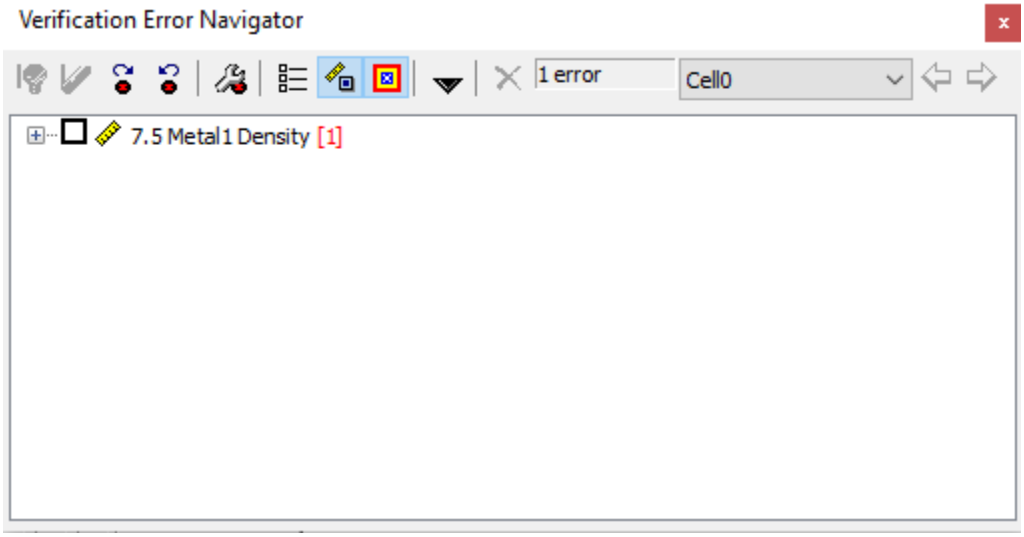


Run DRC to make sure your dimensions are not violating any design rules

- Click on the DRC button in the upper left corner of the screen (little green play arrow). If everything checks out, you should see:

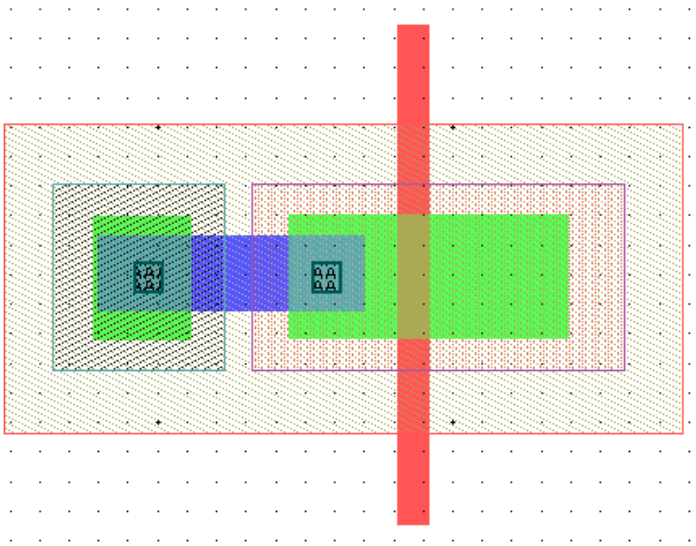



You can ignore Metal density error.

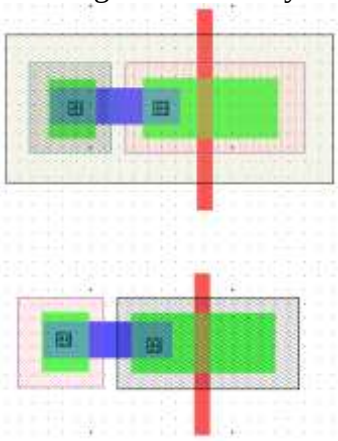


## PMOS Layout Design:

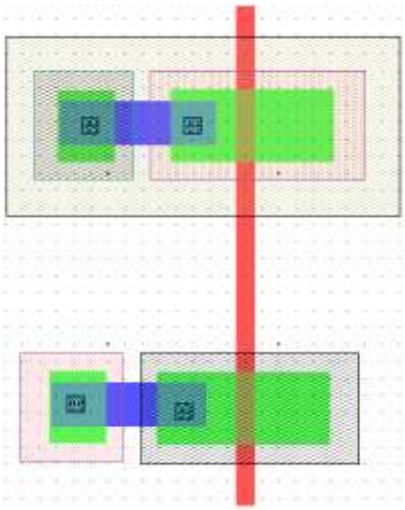
Use same deminsions as you set for NMOS to design PMOS Transistors.



After designing both transistors, your design window may look like this:



Extend Poly Lines to connect both gates. As shown in figure given below:

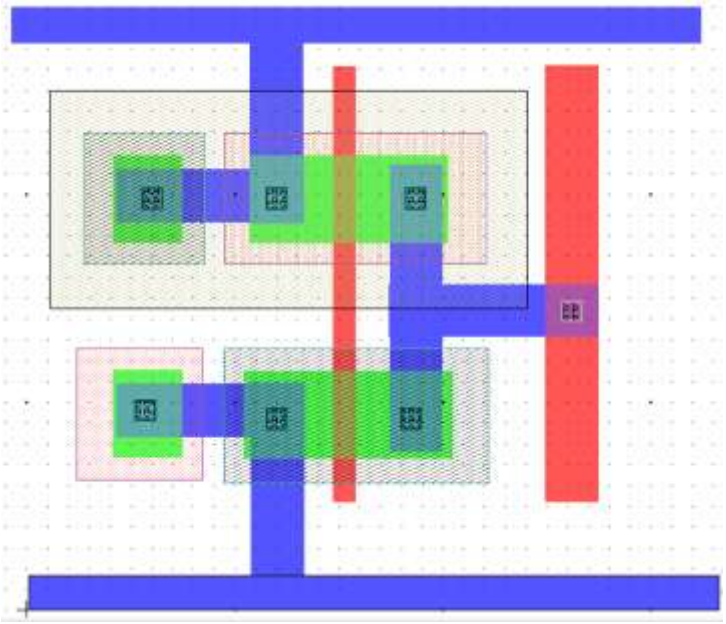


Connecting the Inverter

Metal and Poly are connected together by simply drawing \rectangles that are adjacent to or overlap another rectangle of the same type (i.e., M1 to M1, Poly to Poly). Connect the inverter together as shown in the following figure:

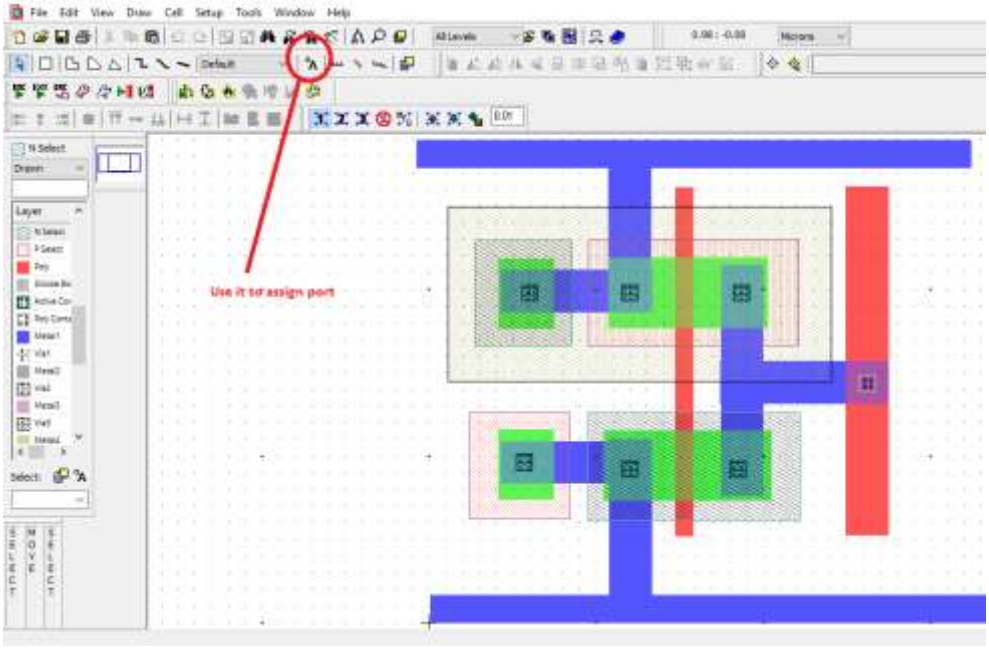
- We typically put horizontal strips across the chip to route VDD and VSS to multiple devices. These are called power supply “rails”.

- Connect the drains together using Metal 1

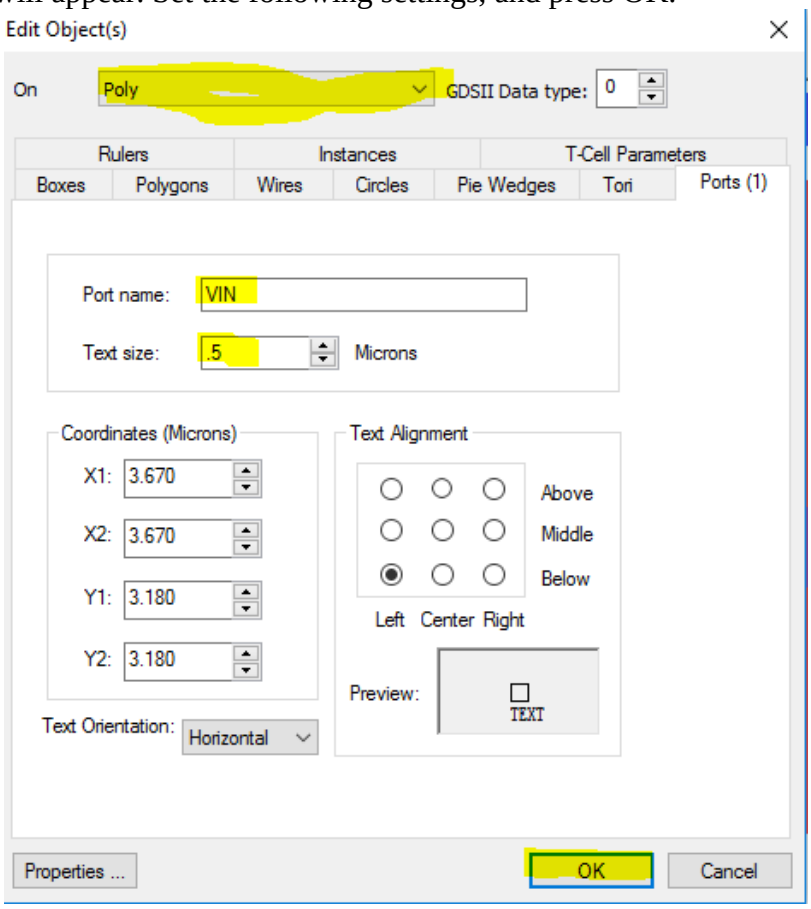


Label the 4-nodes of the inverter using the Drawing Ports button. (VDD, VSS, VIN, VOUT)

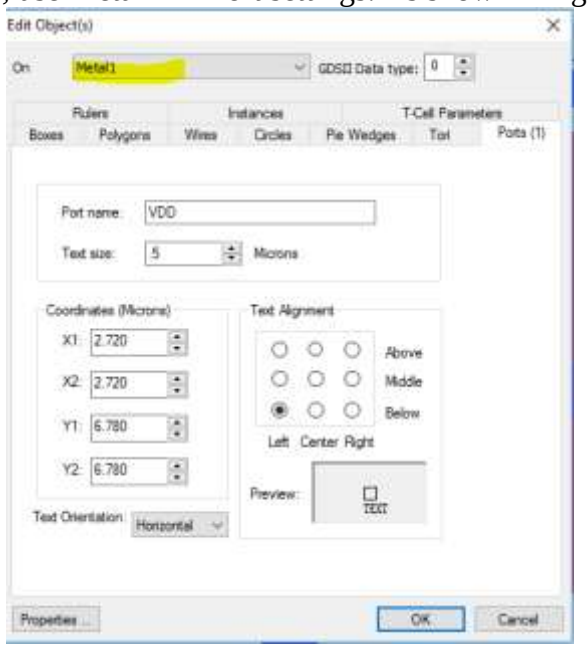
- Select Port button as indicated in figure below:



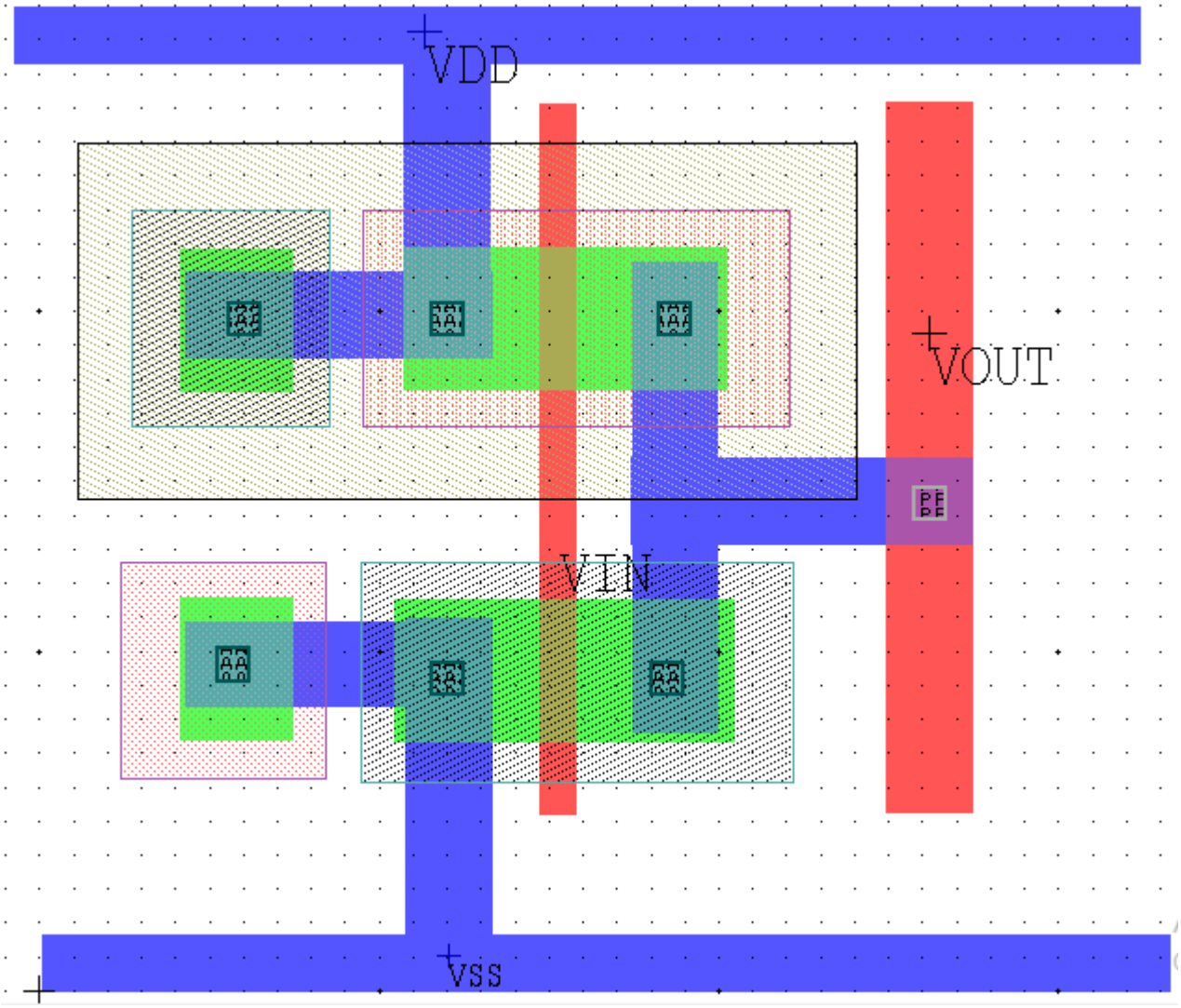
- Click on Poly Line
- A window will appear. Set the following settings, and press OK.



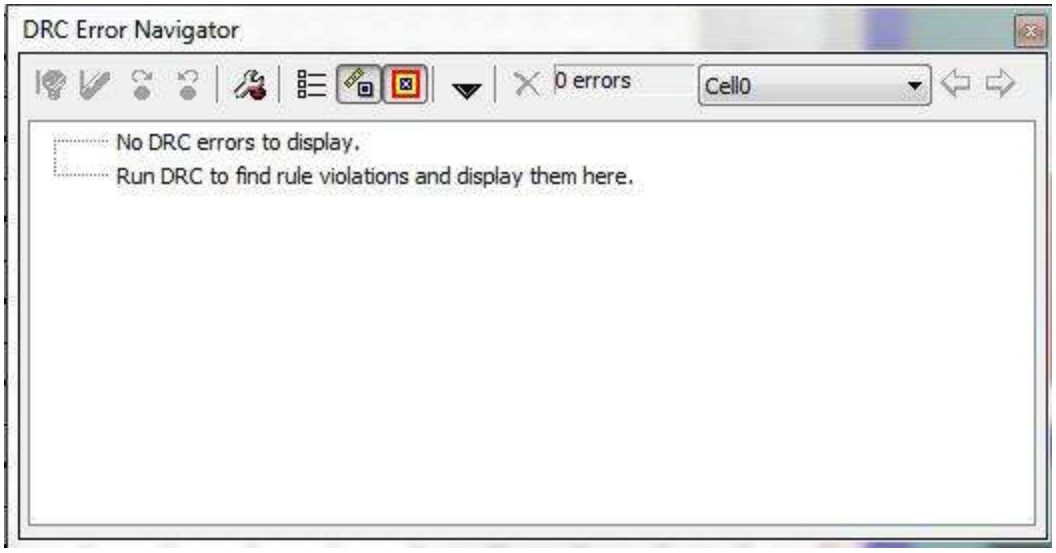

- Same steps for VOUT.
- For VDD and VSS, use Metal 1 in Port settings. As shown in figure below:




Your Final design may look like this:

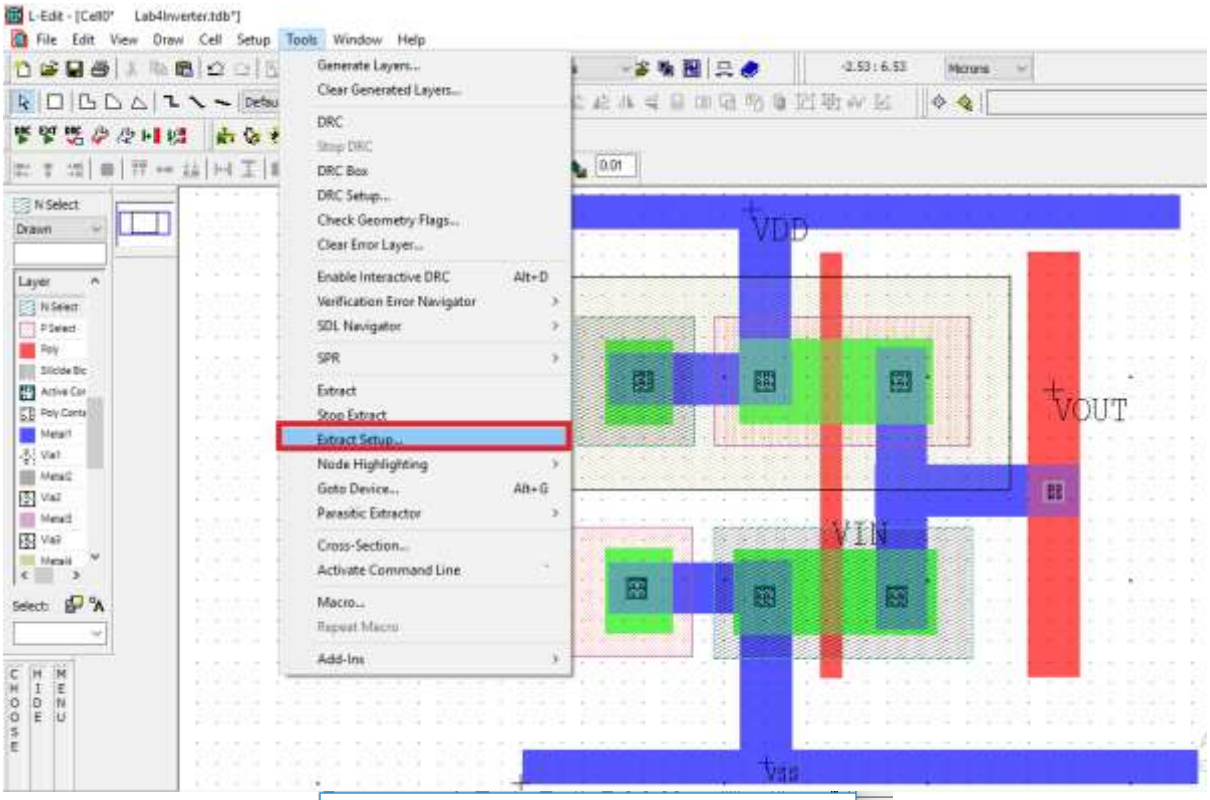


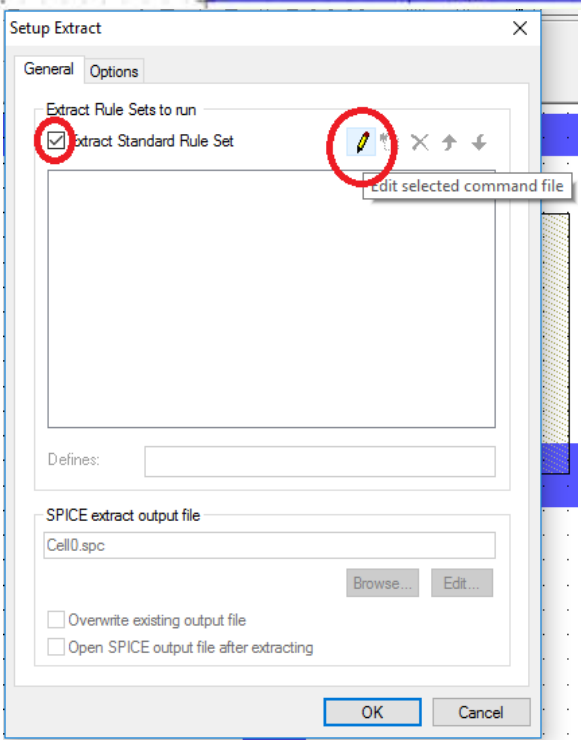

Perform a Final DRC on the Design

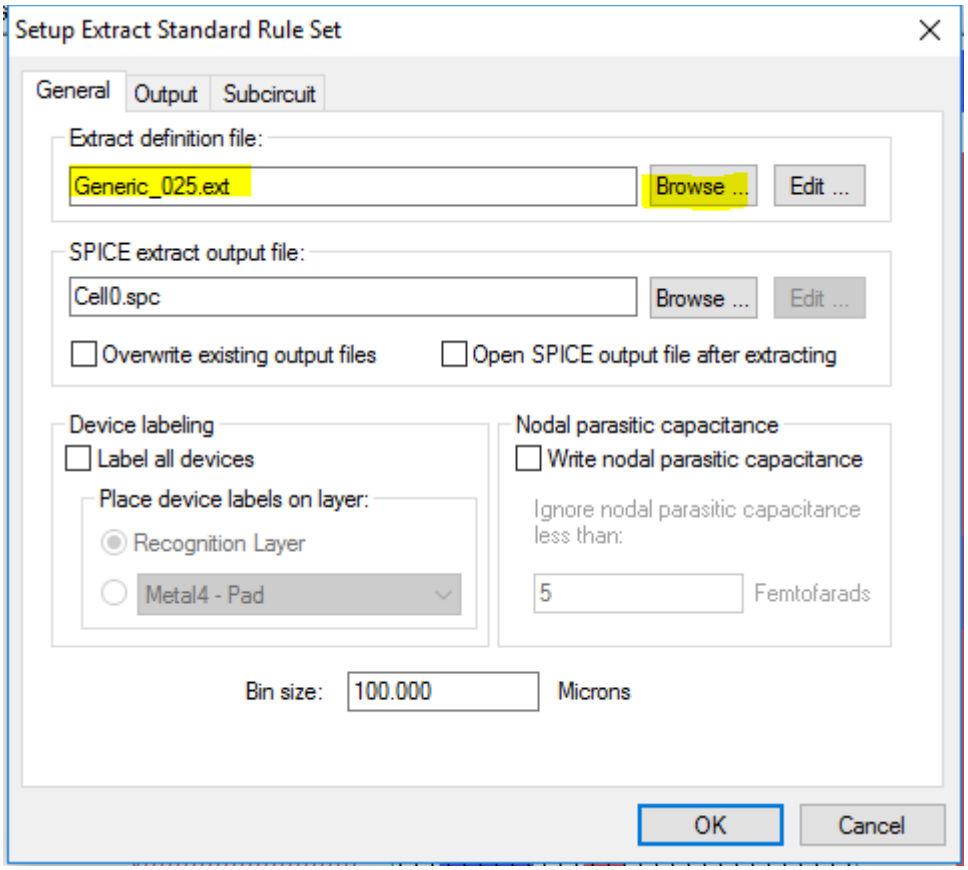


**Design steps are complete now. Next part is to test your inverter. Follow the steps given below:**

**Step 1:**



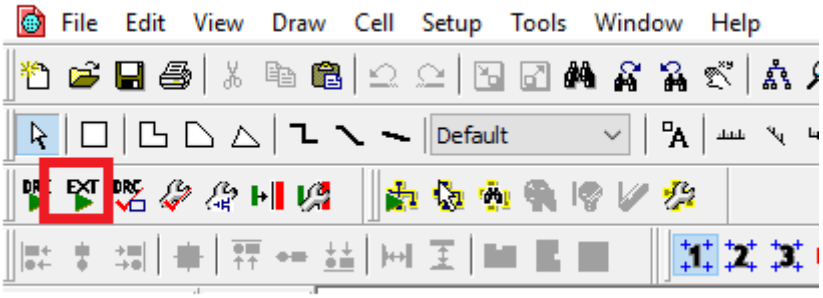






In the Extract dialog that appears, specify the extract definition file at: …Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and VS\Tech\Generic0_25um \ Generic_025.ext

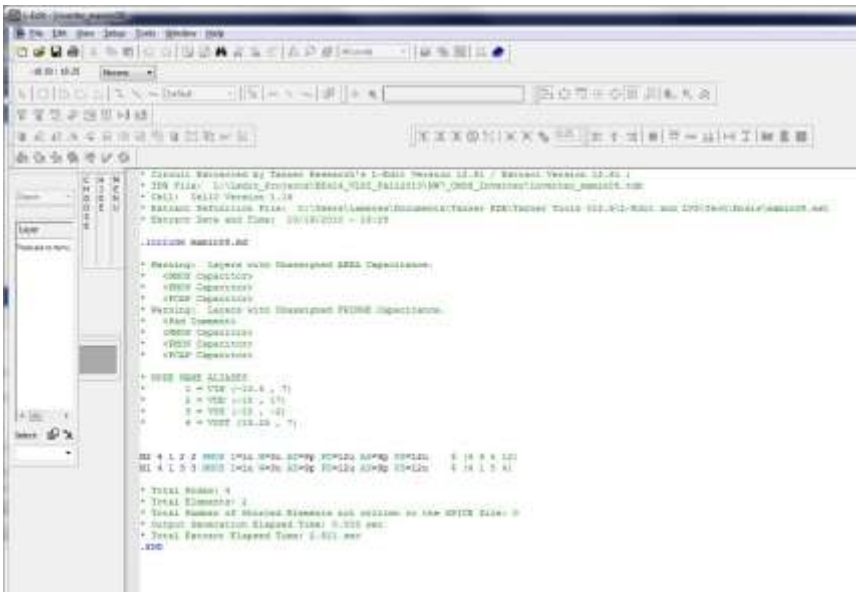
- specify the output name

Click on Extraction button.




A new file will be created at the same path where your layout is saved with an extension ".spc". Open they file.

- you should see an extracted spice Netlist as follows:



Notice that the Length and Width of our transistors is what we wanted (W/L=1um/.25um) = 1u/250n

Notice that the node name aliases show up as we wanted indicating that our inverter is connected correctly.

1) Click on insert command button. Now follow the steps.

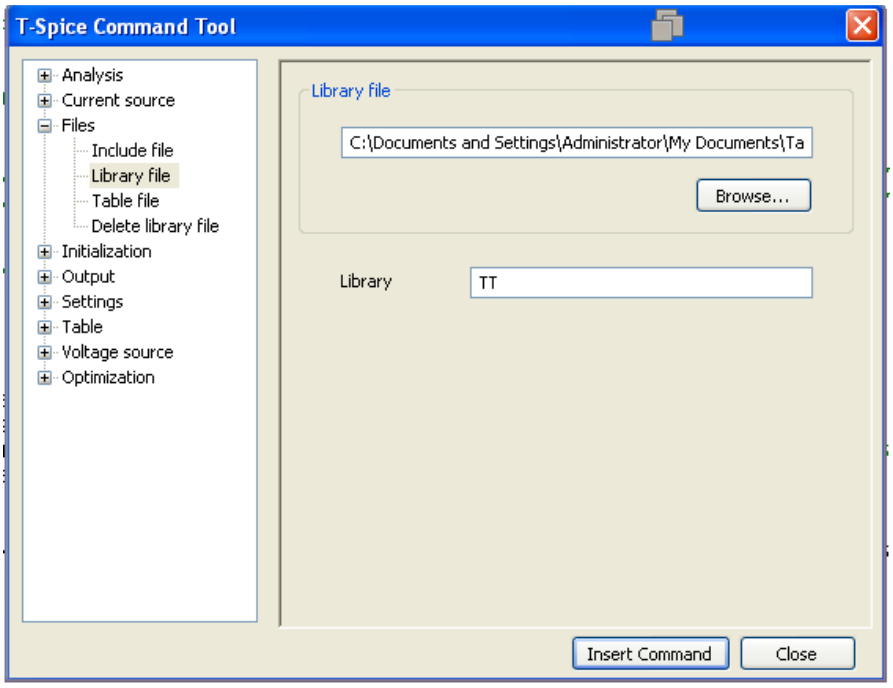
➔ Transient – Maximum time = 10n , Simulation time = 100n

Click “Insert command”

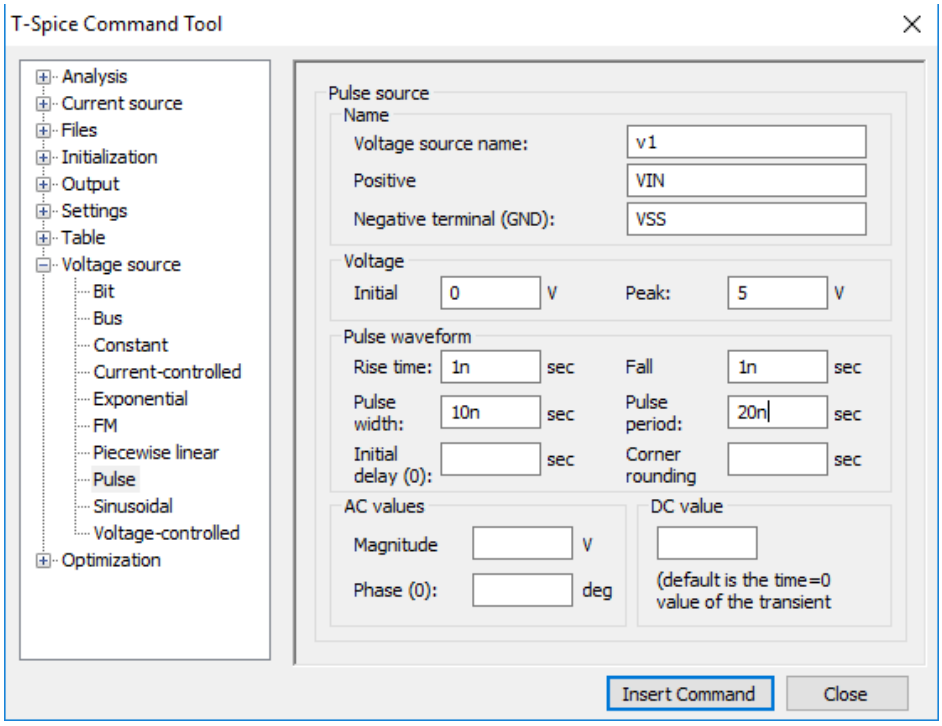
➔ Files – Library files – Browse – “Documents – Tanner EDA – Tanner Tools v14.1- Libraries – Models – Generic_025”

Library = TT

Click “Insert command”

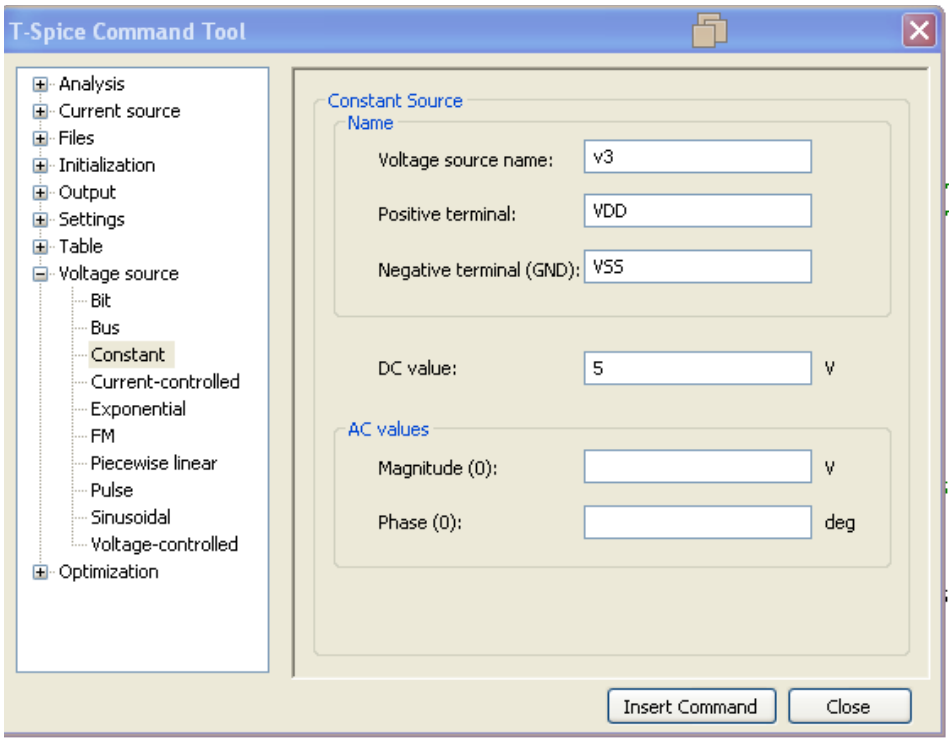



➔ Voltage source – Pulse “For applying inputs VIN or A,B etc and VDD”




Click “Insert command”

➔ Applying VDD

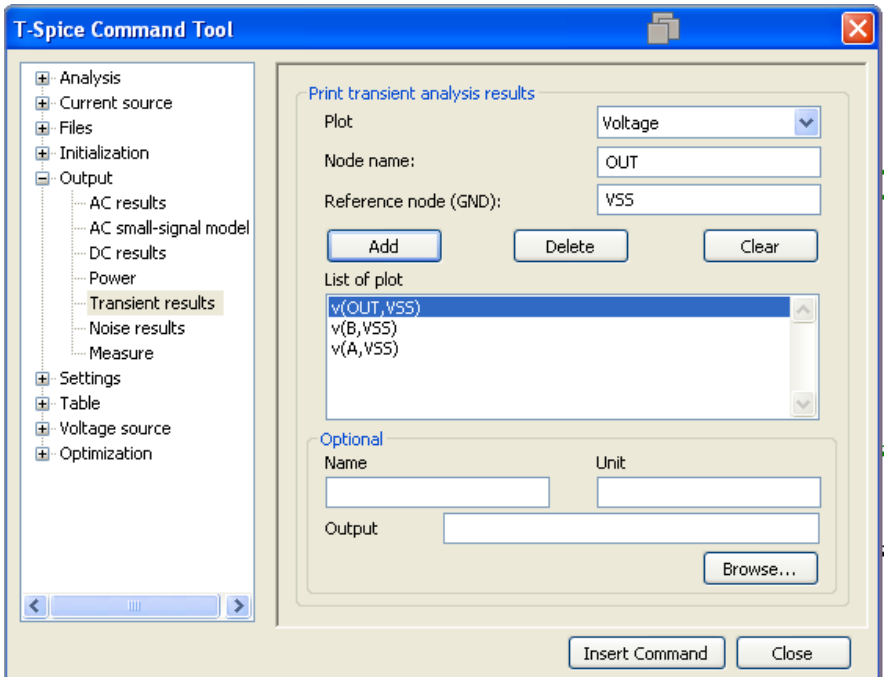



➔ Now settings for displaying outputs.

Output – Transient results “Node name = VIN ， Reference node = VSS”

Click Add

Similarly for other voltages to be printed.



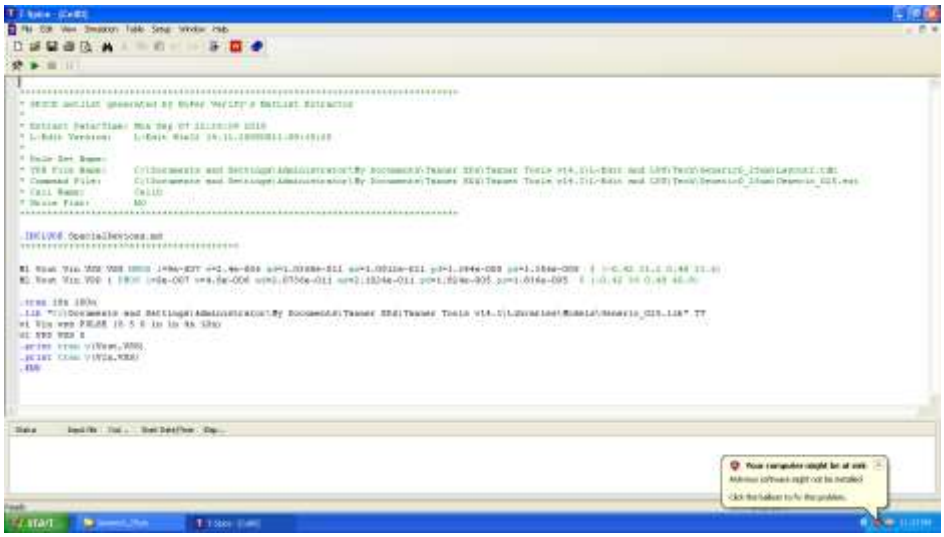

Close Window

➔ Add these commands at the end of your spice file

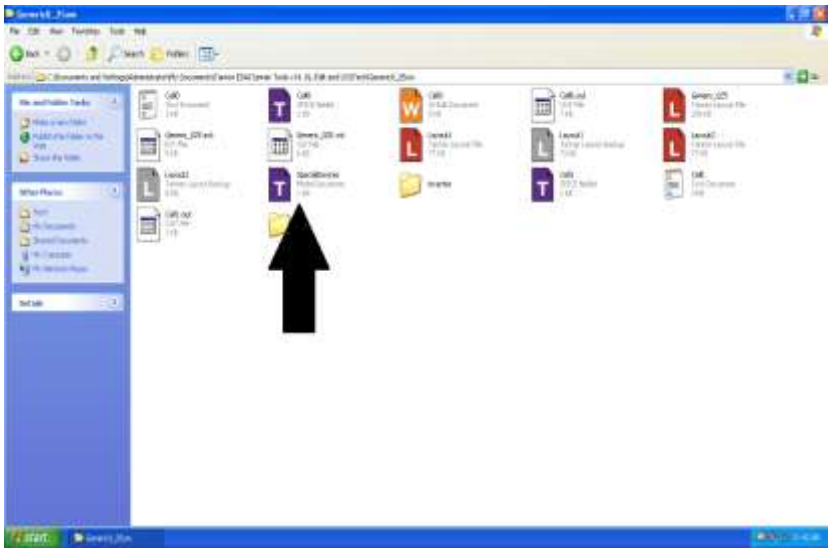
.op

.END

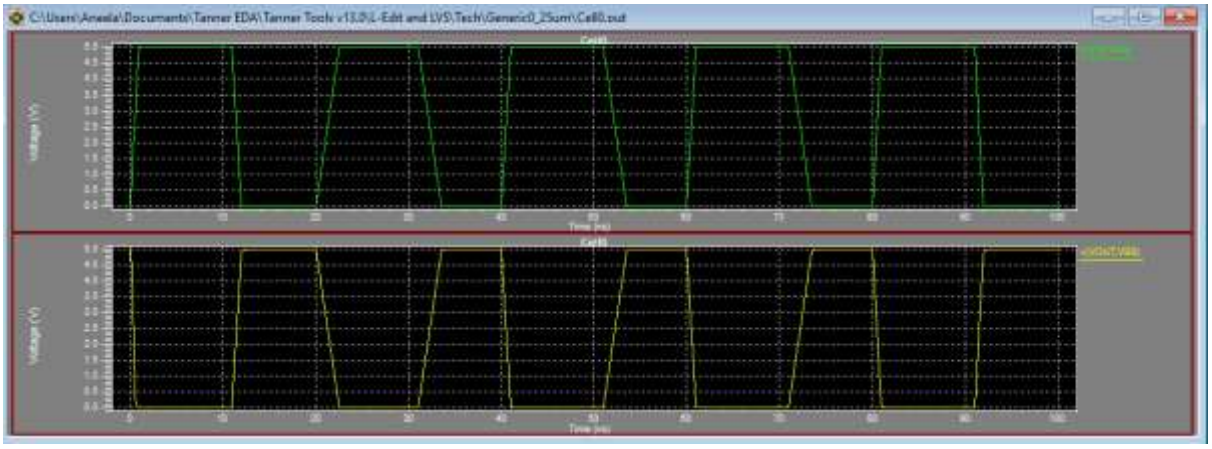
Spice file should look like this



➔ Copy “Special Devices “and paste in your design(NAND) folder.



➔ Click “RUN”



## Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

_____

_____

_____

_____

_____

_____

Student's signature and Date

## Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)
  _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission
  _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed?
  _____/10
- ☐ **TOTAL:**
  _____/50

## Feedback on student behaviour:

***Encircle*** your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2

- ☐ Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

_____

_____

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_____

Lab Engineer's signature and Date

## Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisified
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedabck is for LAB session: LAB Number: _____, Date: _____
- ☐ General (to provide feedback on a persistent practice/ocurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

**This feedback is:**

- ☐ For a Particular
- ☐ Who conducted the LAB? _____
- ☐ Actual Start time: _____ Total Duration of Lab: _____
- ☐ Instruction Duration: _____ Practical Duration: _____
- ☐ LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- ☐ Had the theory related to lab been covered in theory class? Yes/No

***Encircle*** your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

| | | | | | | |
|---|---|---|---|---|---|---|
| **Instruction Session** | Was duration of instruction session adequate? | -2 | -1 | 0 | +1 | +2 |
| | How much did you understand about the practical? | -2 | -1 | 0 | +1 | +2 |
| | How much content was irrelevant to the practical? | -2 | -1 | 0 | +1 | +2 |
| | Did the instructor allowed Q/A and discussion? | -2 | -1 | 0 | +1 | +2 |
| **Practical** | Did you get sufficient time for practical? | -2 | -1 | 0 | +1 | +2 |
| **Lab Engineer** | Presence in lab at all time? | -2 | -1 | 0 | +1 | +2 |
| | Ability to convey? | -2 | -1 | 0 | +1 | +2 |
| | Readiness to help during practical? | -2 | -1 | 0 | +1 | +2 |
| | Readiness to discuss theoretical aspects? | -2 | -1 | 0 | +1 | +2 |
| | Helps in troubleshooting? | -2 | -1 | 0 | +1 | +2 |
| | Guides hows & whys of troubleshooting? | -2 | -1 | 0 | +1 | +2 |
| **Staff** | How friendly was the lab staff? | -2 | -1 | 0 | +1 | +2 |
| | Presence of staff throughout the lab session? | -2 | -1 | 0 | +1 | +2 |
| | Impact of availability of staff on your practical? | -2 | -1 | 0 | +1 | +2 |
| **Equipment** | Performance of Electronic Instruments? | -2 | -1 | 0 | +1 | +2 |
| | Performance of Breadboard/experiment kit? | -2 | -1 | 0 | +1 | +2 |
| | Performance of circuit components esp. ICs? | -2 | -1 | 0 | +1 | +2 |
| **Overall** | Your overall rating for the whole lab session? | -2 | -1 | 0 | +1 | +2 |

Other comments:

_____

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