VLSI Lab

LABORATORY REPORT

Spring 2019

LAB 07

Title of Lab Experiment: Implementation of Transmission Gate Circuits Layout using available CAD Tools

Engr. Rashid Karim

_____Kamran_____	___i140420___	_A_
STUDENT NAME	ROLL NO	SEC

Submission Date: _____13/3/19_____

_____

LAB ENGINEER SIGNATURE & DATE

MARKS AWARDED: **/10**

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD

LAB:	07	Implementation of Transmission Gate Circuits Layout using available CAD Tools

1. Learning Objectives:

a. Transmission Gate circuits
b. Layout design using Transmission Gate.

2. Equipment Required:

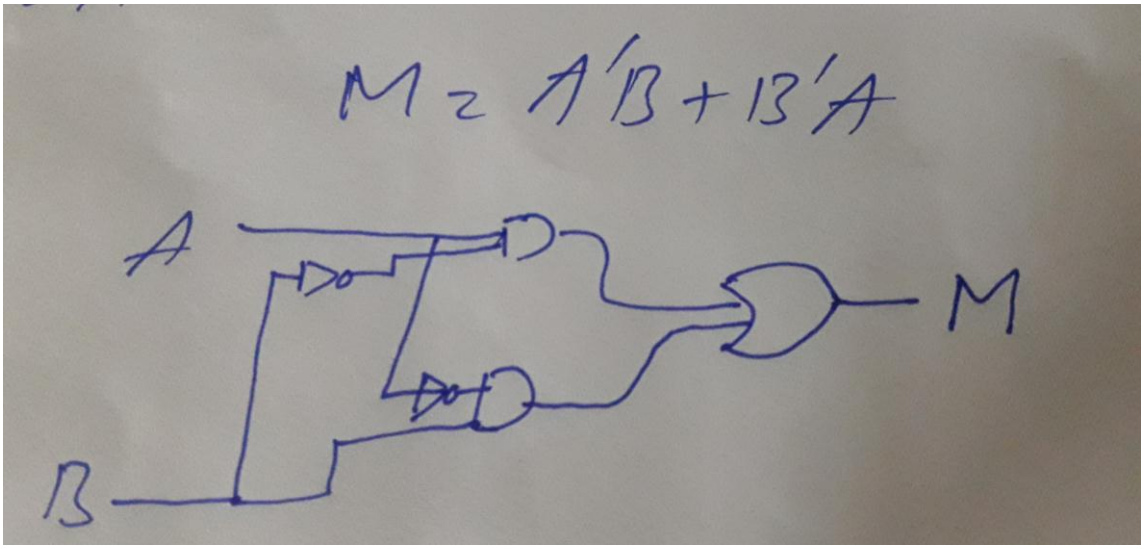
Software : L-Edit

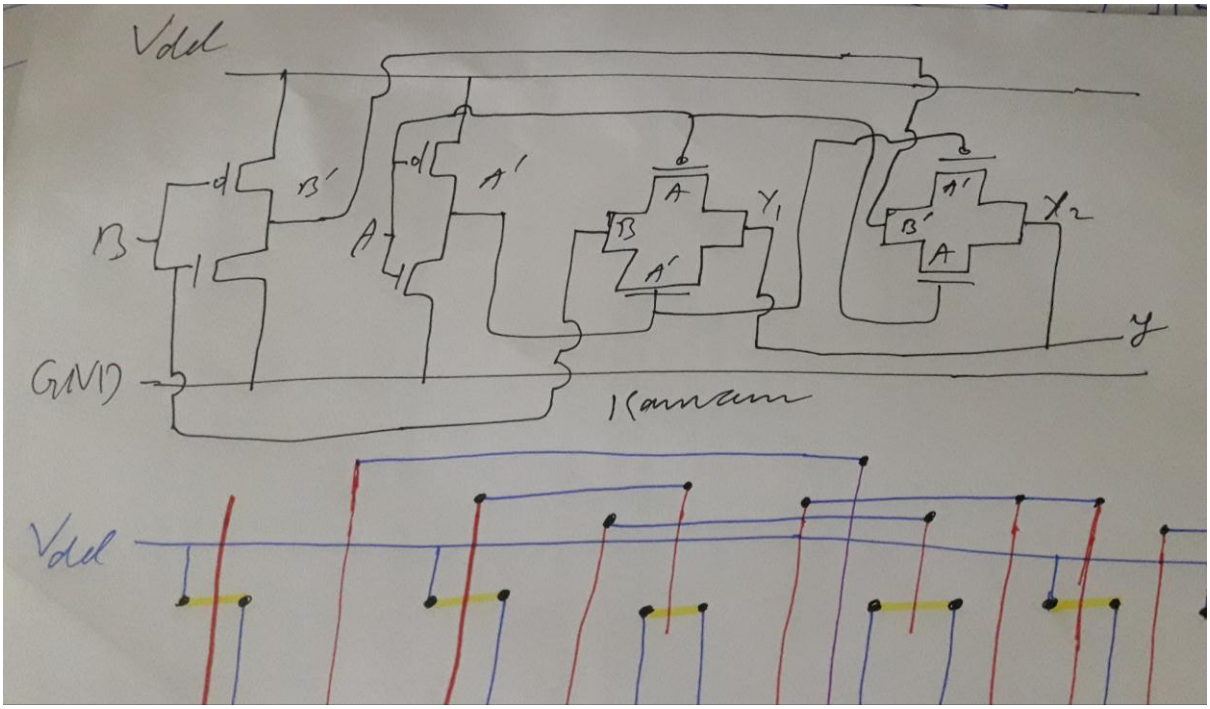
3. Lab Summary:

In this lab,we made gate level, transistor level and stick diagrams of XOR gate using Transmission gates.We then implemented it's layout on L-Edit,extracted into T-Spice file code and simulated and verified using W-Edit tools.

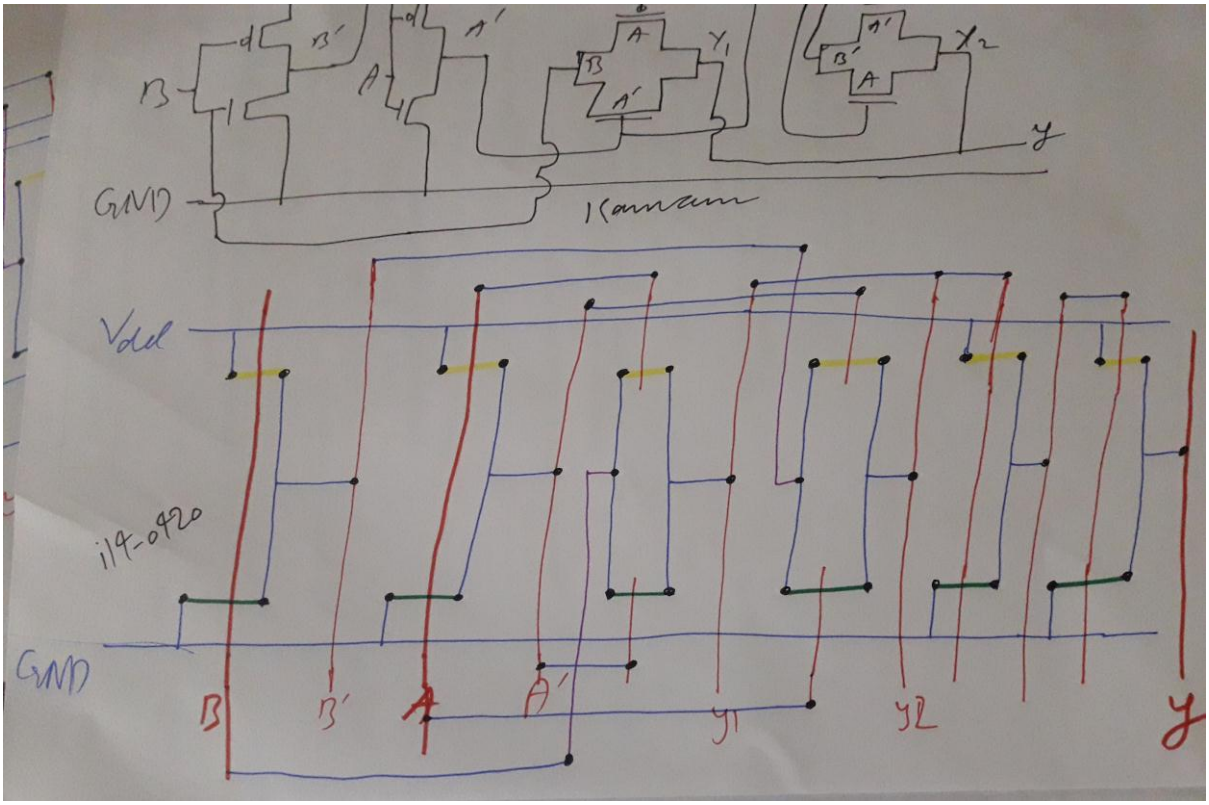
4. Task

Transistor Level Diagram

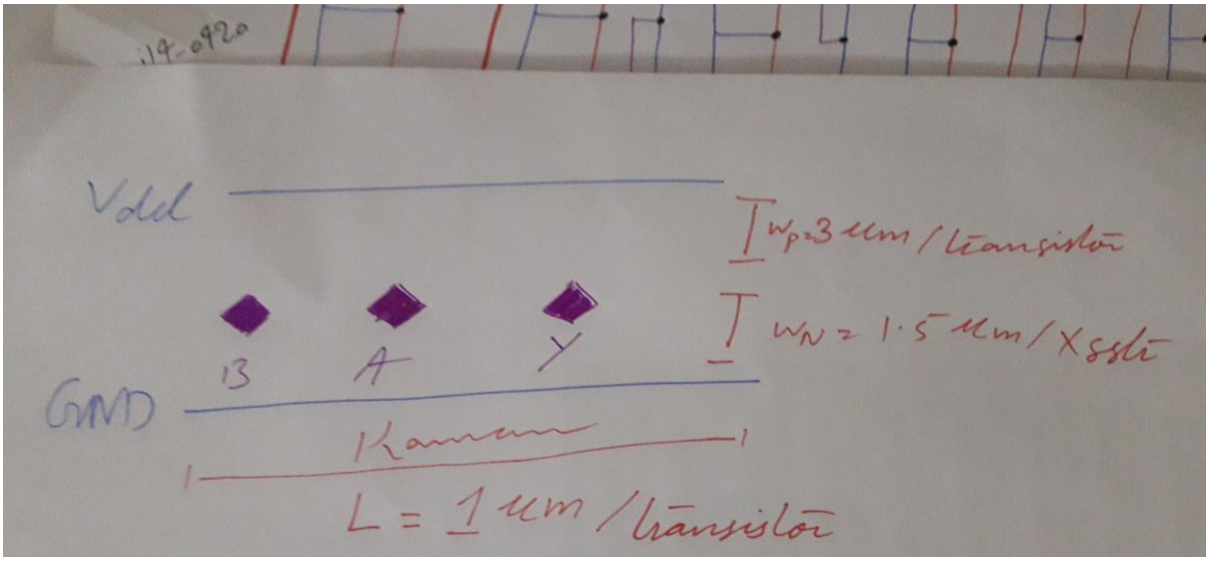




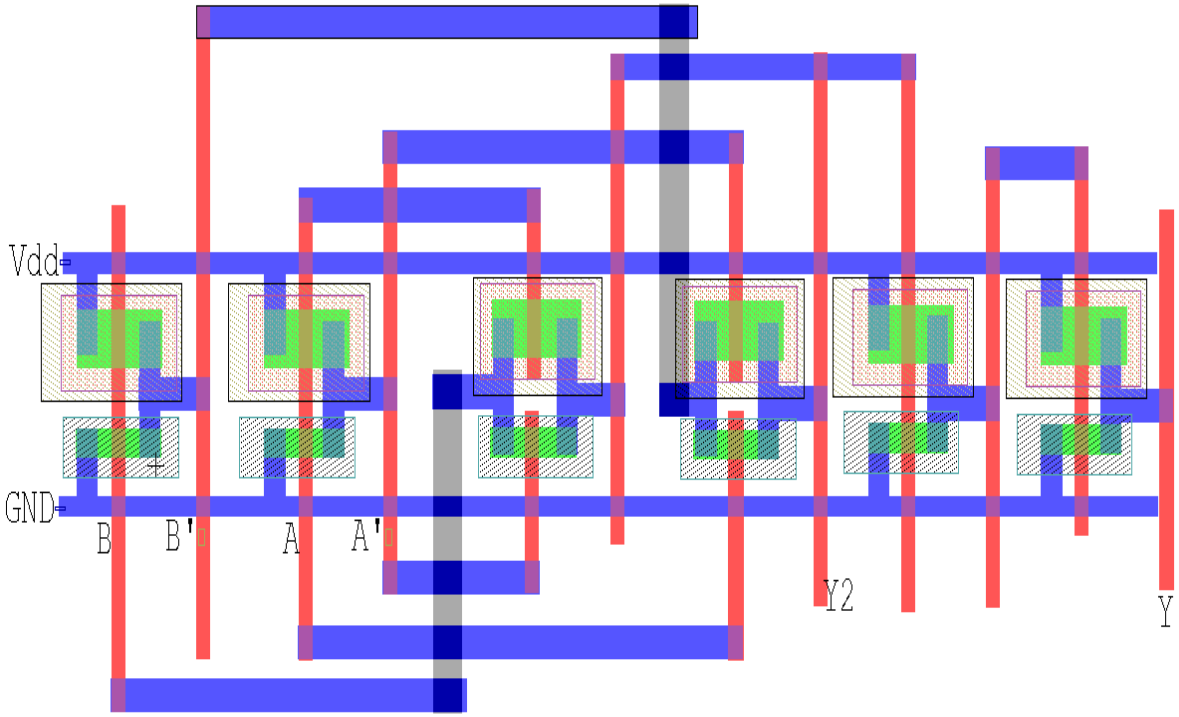
Stick Diagram



Abstract



Layout:



Spice File Code

* Circuit Extracted by Tanner Research's L-Edit Version 13.00 / Extract Version 13.00 ;

* TDB File: D:\Kamran\Study\FAST NUCES\Mad Max 19\VLSI Lab\Kamran_VLSI_7_13-3\New Xmsn XOR.tdb

* Cell: Cell0 Version 1.26

* Extract Definition File: Generic_025.ext

* Extract Date and Time: 03/14/2019 - 23:08

.INCLUDE SpecialDevices.md

.lib "D:\Kamran\Study\FAST NUCES\Mad Max 19\VLSI Lab\Kamran_VLSI_7_13-3\Generic_025.lib" TT

.tran 10n 100n

v1 A GND PULSE (0 5 0 1n 1n 10n 20n)

v3 B GND PULSE (0 5 5n 1n 1n 10n 20n)

v4 Vdd GND 5

.print tran v(A,GND) v(B,GND) v(Y,GND)

* NODE NAME ALIASES

* 3 = Y (77.26 , -6.19)
* 4 = GND (-7.7 , -2.35)
* 5 = Vdd (-7.3 , 10.4)
* 6 = Y2 (50.68 , -6.95)
* 8 = A (11.12 , -4.28)
* 17 = B (-3.24 , -4.28)

M1 Y 2 Vdd 9 PMOS L=1u W=3u AD=8.91p PD=11.94u AS=7.59p PS=11.06u $ (70.42 5.23 71.42 8.23)

M2 2 Y2 Vdd 10 PMOS L=1u W=3u AD=8.91p PD=11.94u AS=7.59p PS=11.06u $ (57.17 5.33 58.17 8.33)

M3 Y2 1 16 11 PMOS L=1.02u W=3u AD=9.3p PD=12.2u AS=7.98p PS=11.32u $ (43.98 5.49 45 8.49)

M4 7 A Vdd 12 PMOS L=1u W=3u AD=8.55p PD=11.7u AS=7.95p PS=11.3u $ (11.01 5.05 12.01 8.05)

M5 Y2 A B 13 PMOS L=1.02u W=3u AD=9.3p PD=12.2u AS=7.98p PS=11.32u $ (28.46 5.61 29.48 8.61)

M6 16 B Vdd 14 PMOS L=1u W=3u AD=8.55p PD=11.7u AS=7.95p PS=11.3u $ (-3.35 5.05 -2.35 8.05)

M7 Y 2 GND 15 NMOS L=1u W=1.5u AD=3.825p PD=8.1u AS=3.795p PS=8.06u $ (70.42 0.58 71.42 2.08)

M8 2 Y2 GND 15 NMOS L=1u W=1.5u AD=3.825p PD=8.1u AS=3.795p PS=8.06u $ (57.17 0.68 58.17 2.18)

M9 Y2 A 16 15 NMOS L=1.1u W=1.5u AD=4.065p PD=8.42u AS=4.035p PS=8.38u $ (43.91 0.32 45.01 1.82)

M10 7 A GND 15 NMOS L=1u W=1.5u AD=3.645p PD=7.86u AS=3.975p PS=8.3u $ (11.01 0.4 12.01 1.9)

M11 Y2 7 B 15 NMOS L=1u W=1.5u AD=4.29p PD=8.72u AS=3.96p PS=8.28u $ (28.34 0.44 29.34 1.94)

M12 16 B GND 15 NMOS L=1u W=1.5u AD=4.125p PD=8.5u AS=4.125p PS=8.5u $ (-3.35 0.4 -2.35 1.9)

* Total Nodes: 17

* Total Elements: 12

* Total Number of Shorted Elements not written to the SPICE file: 0

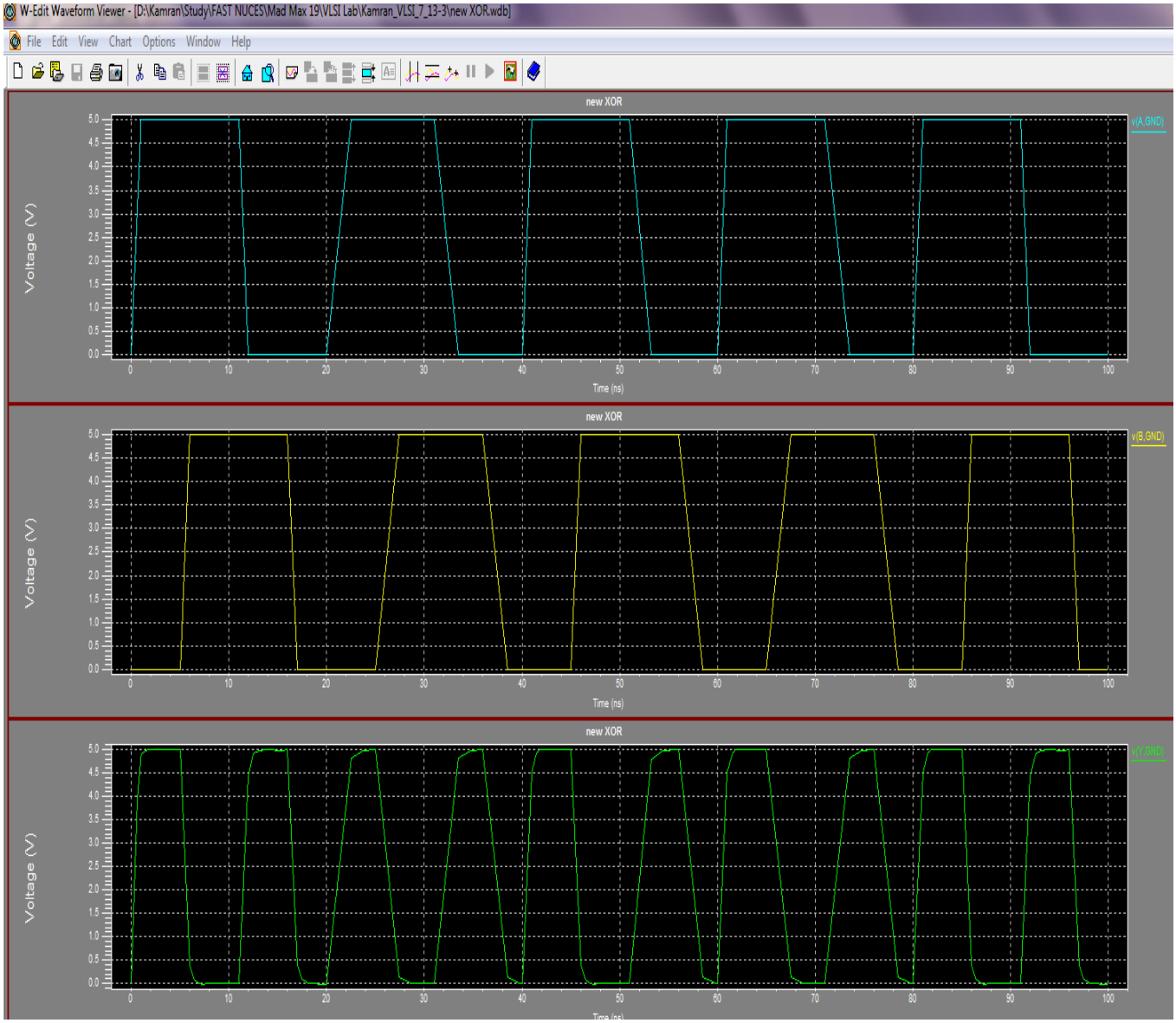
* Output Generation Elapsed Time: 0.000 sec

* Total Extract Elapsed Time: 0.705 sec

.op

.END

Simulation Results/Waveforms


W-Edit Waveform Viewer - [D:\Kamran\Study\FAST NUCES\Mad Max 19\VLSI Lab\Kamran_VLSI_7_13-3\new XOR.wdb]
File Edit View Chart Options Window Help
new XOR
Voltage (V)
Time (ns)
vA.GND)
new XOR
Voltage (V)
Time (ns)
vB.GND)
new XOR
Voltage (V)

Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

_____

_____

_____
Student's signature and Date

Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion) _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed? _____/10
- ☐ **TOTAL:** _____/50

Feedback on student behaviour:

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2
- ☐ Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

_____

_____

_____

_____

_____
Lab Engineer's signature and Date

Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisified
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedabck is for LAB session: LAB Number: _____, Date: _____
- ☐ General (to provide feedback on a persistent practice/ocurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

This feedback is:

- ☐ For a Particular
- ☐ Who conducted the LAB? _____
- ☐ Actual Start time: _____ Total Duration of Lab: _____
- ☐ Instruction Duration: _____ Practical Duration: _____
- ☐ LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- ☐ Had the theory related to lab been covered in theory class? Yes/No

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

Instruction Session	Was duration of instruction session adequate?	-2	-1	0	+1	+2
	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
Staff	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2
	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
Equipment	Performance of Electronic Instruments?	-2	-1	0	+1	+2
	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2

	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

_____

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