VLSI Lab

LABORATORY MANUAL

Spring 2019

LAB 05

Title of Lab Experiment : Implementation and Simulation of Basic Cells Layout using L-Edit

Engr. Rashid Karim

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STUDENT NAME ROLL NO SEC

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LAB ENGINEER SIGNATURE & DATE

MARKS AWARDED: /10

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD

Prepared by:	Furqan Mehmood	Version:	3.00
Last Edited by:	Aneela Sabir	Date:	26 Feb,2019
Verified by:	Rashid Karim.		

LAB:	05	Implementation and Simulation of Basic Cells Layout using L-Edit

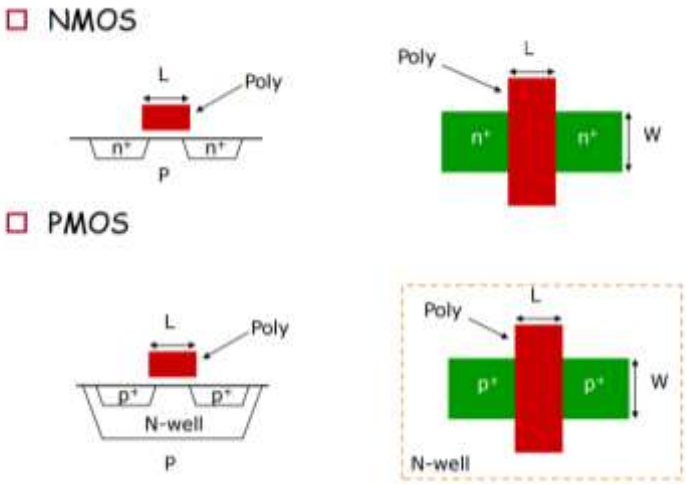
1. Learning Objectives:

a. Mask level implementation of all basic cells
b. Functional verification through output/input waveforms.

2. Equipment Required:

Software : L-Edit , T-Spice, W-Edit

3. Introduction:



Functions of masks:

- Five masks must be used to define the transistor:
  - P Well
  - Active Area
  - Polysilicon
  - N+ implant
  - P+ implant
- P Well, for isolation.
- Top *substrate* connection.
- P+/N+ implants produce good *ohmic* contacts.

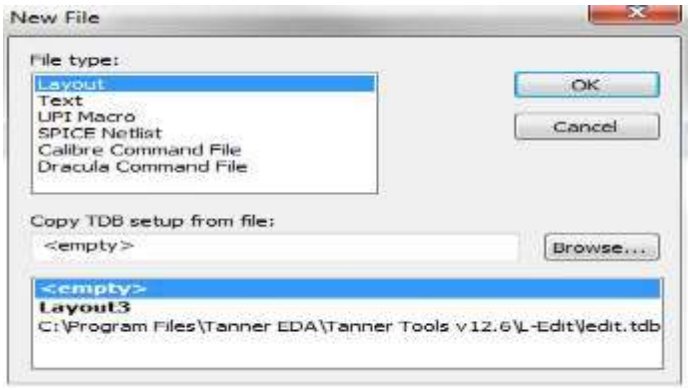
4. Procedure:

Designing NAND gate in L-Edit.

1) Launch L-edit using: Start – All Programs – Tanner EDA – Tanner Tools v13– L-Edit v13

2) Create a new layout design:

- File – New
  - select "Layout"
  - under "Copy TDB…", select **<empty>** from the bottom dialog
  - Click "OK"



3) Load in the Generic0_25um design kit: -

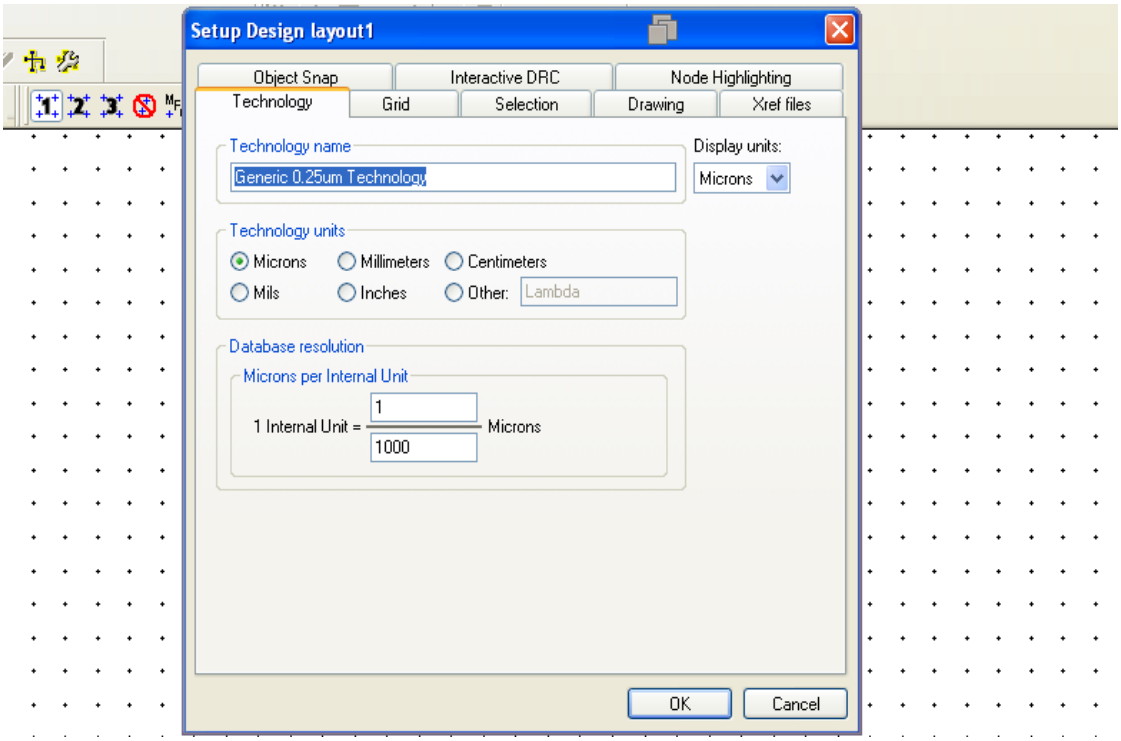
File –Replace Setup

Browse to:

…Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\Tech\Generic0_25um and select the "**Generic0_25um.tbd**" file Click "OK", and "OK" again.

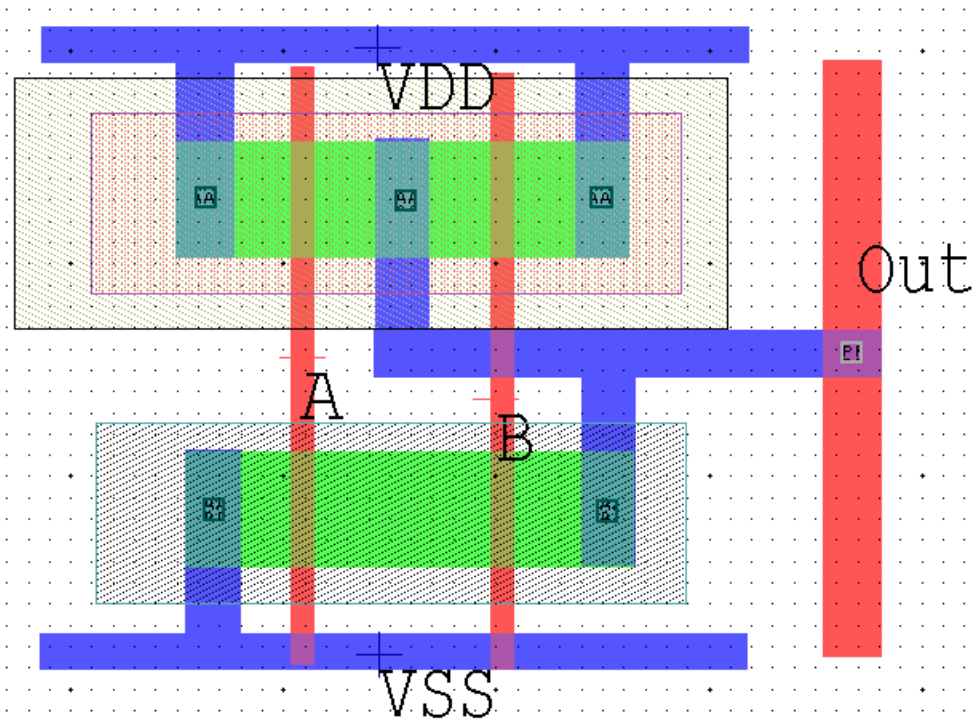
Notice that all of the layers available in the 0_25um design kit are now in the drawing palette on the left.

4) Verify the technology rule options: - Setup – Design



5) Save your design according to following path.
Documents – Tanner EDA –Tanner Tools v13.0 – L-Edit and LVS – Tech - Generic0_25um - NAND(Folder)-NANDLayout.

6) Now creating layout of NAND gate(Any Dimensions Least possible will be best).

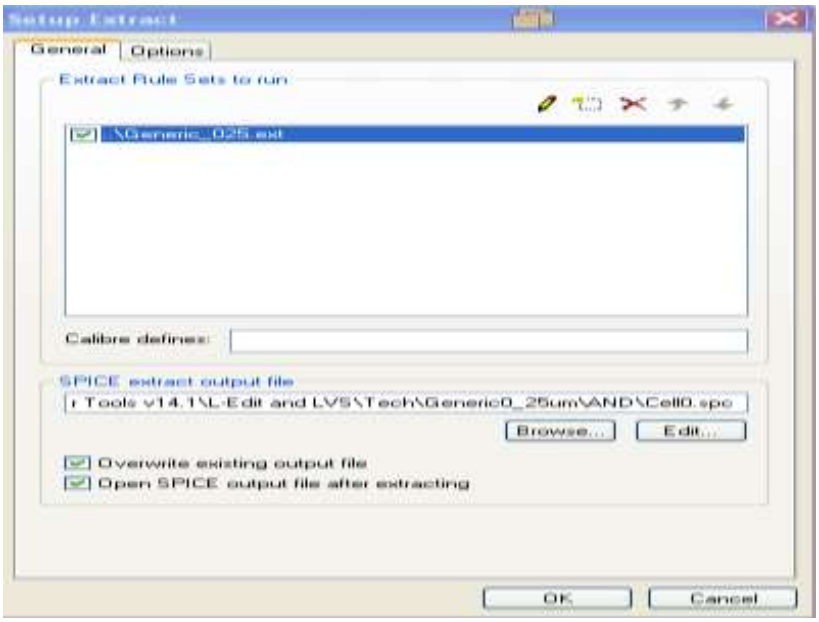


7) Extract setup –

Documents – Tanner EDA –Tanner Tools v14.1 – L-Edit and LVS – Tech - Generic0_25um.ext

Set Spice extract output file location -

C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools v14.1\L-Edit and LVS\Tech\Generic0_25um\AND\Cell0.spc



8) Extract your design. A spice file is generated in your target folder. Open it.

9) Click on insert command button. Now follow the steps.

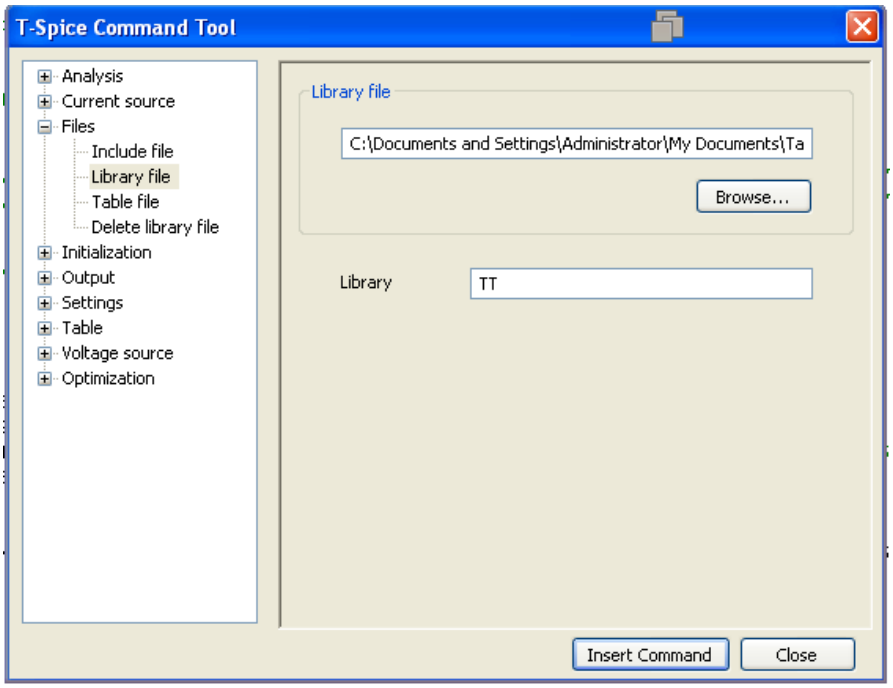
➔ Transient – Maximum time = 10n , Simulation time = 100n

Click “Insert command”

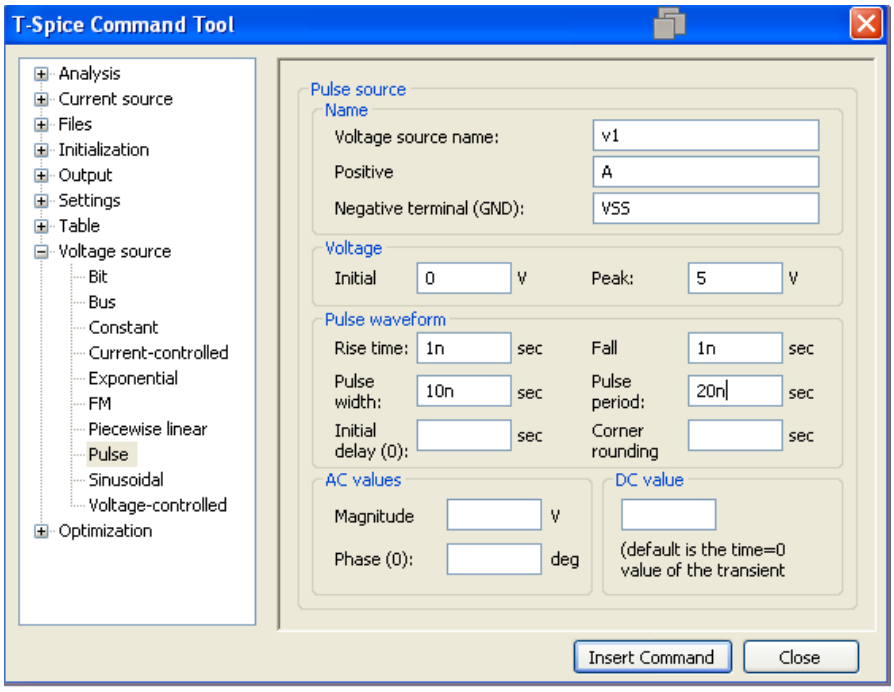
➔ Files – Library files – Browse – “Documents – Tanner EDA – Tanner Tools v13.0- Libraries – Models – Generic_025”

Library = TT

Click “Insert command”

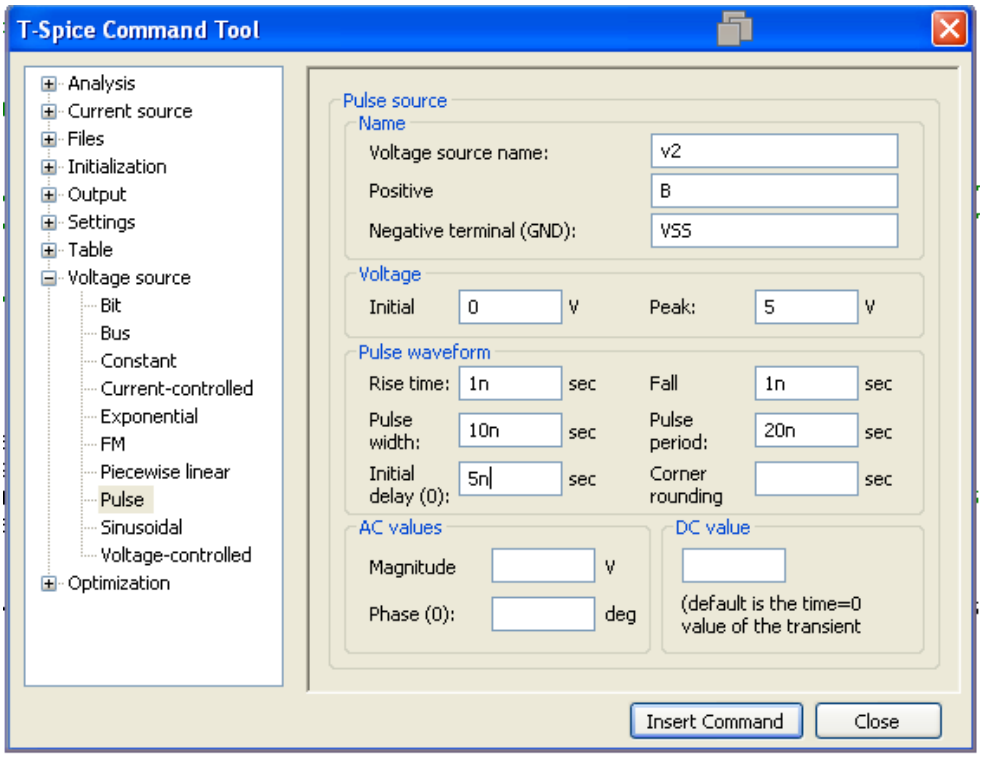


➔ Voltage source – Pulse “For applying inputs A,B and VDD”

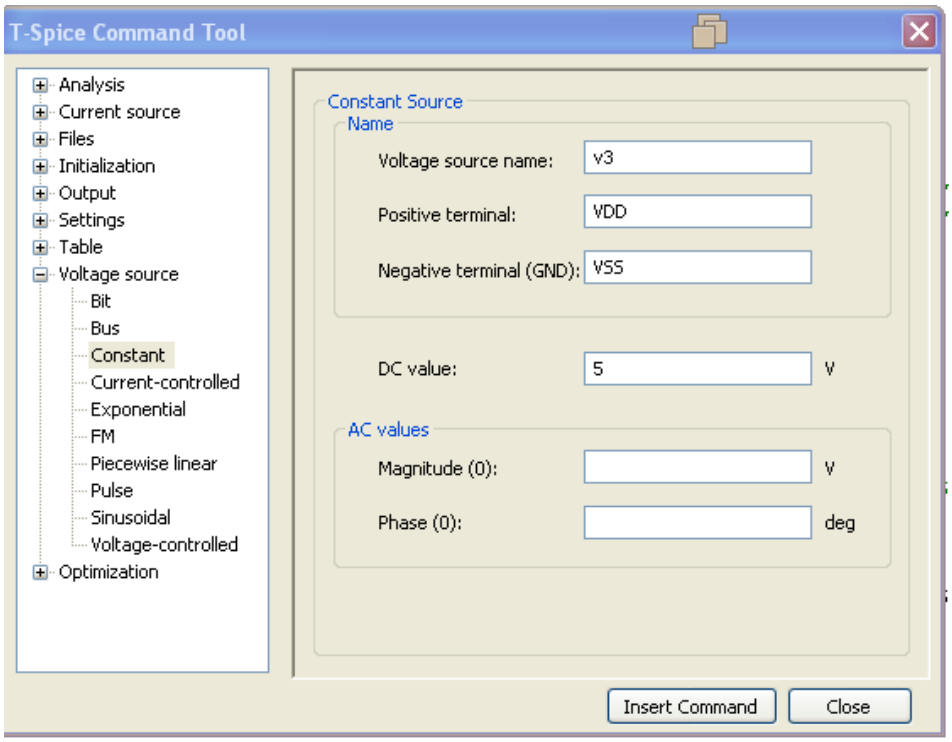


Click “Insert command”

Similarly for input voltage B



➔ Applying VDD

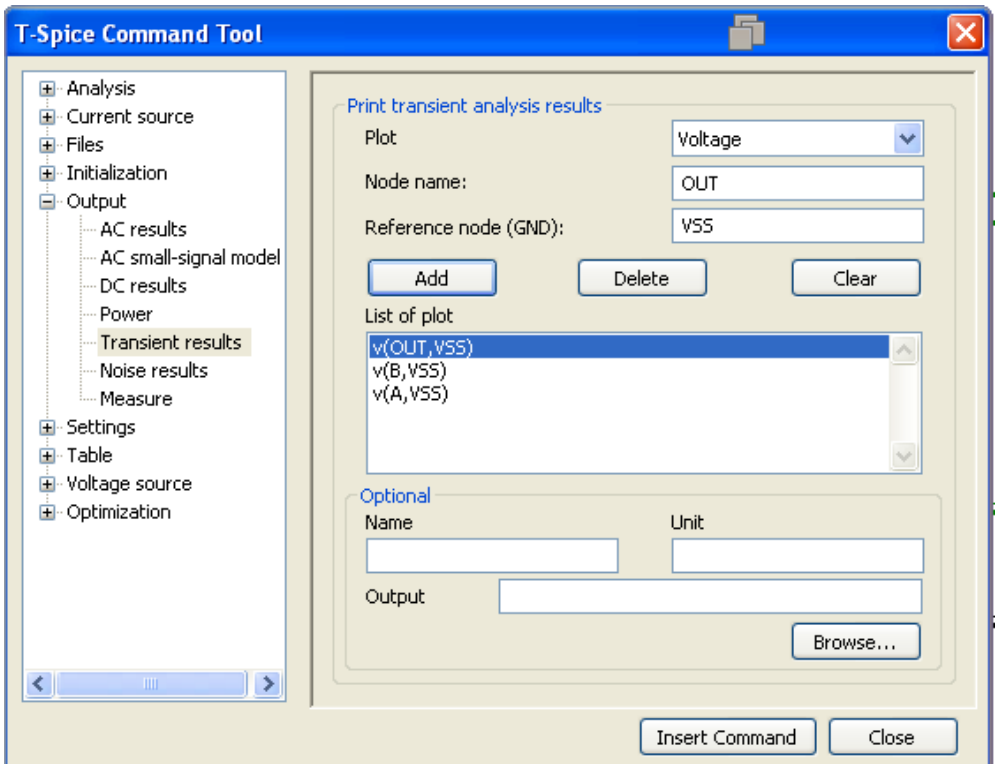


➔ Now settings for displaying outputs.

Output – Transient results “Node name = A , Reference node = VSS”

Click Add

Similarly for other voltages to be printed.



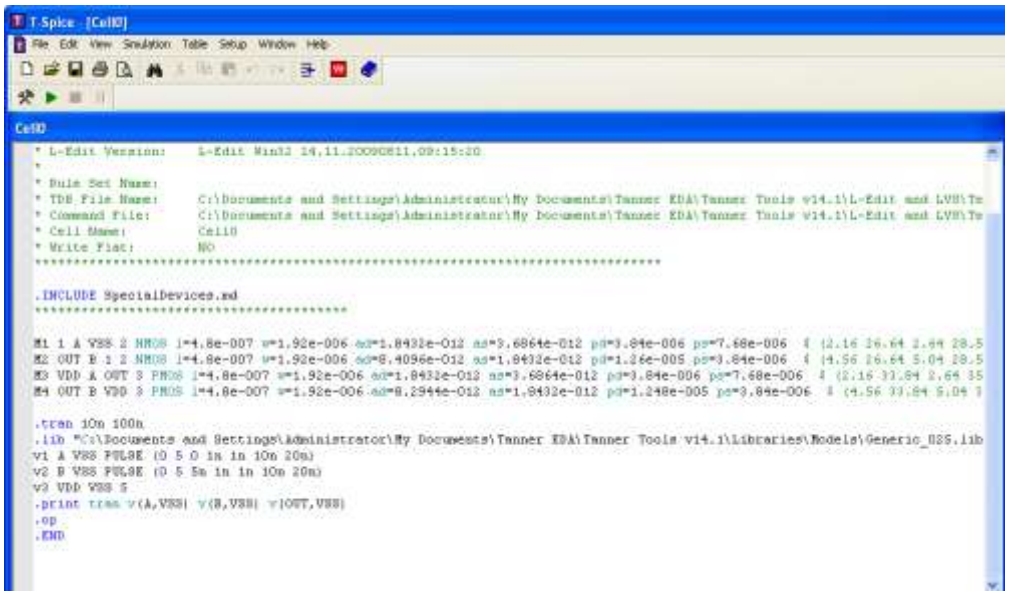
Close Window

➔ Add these commands at the end of your spice file

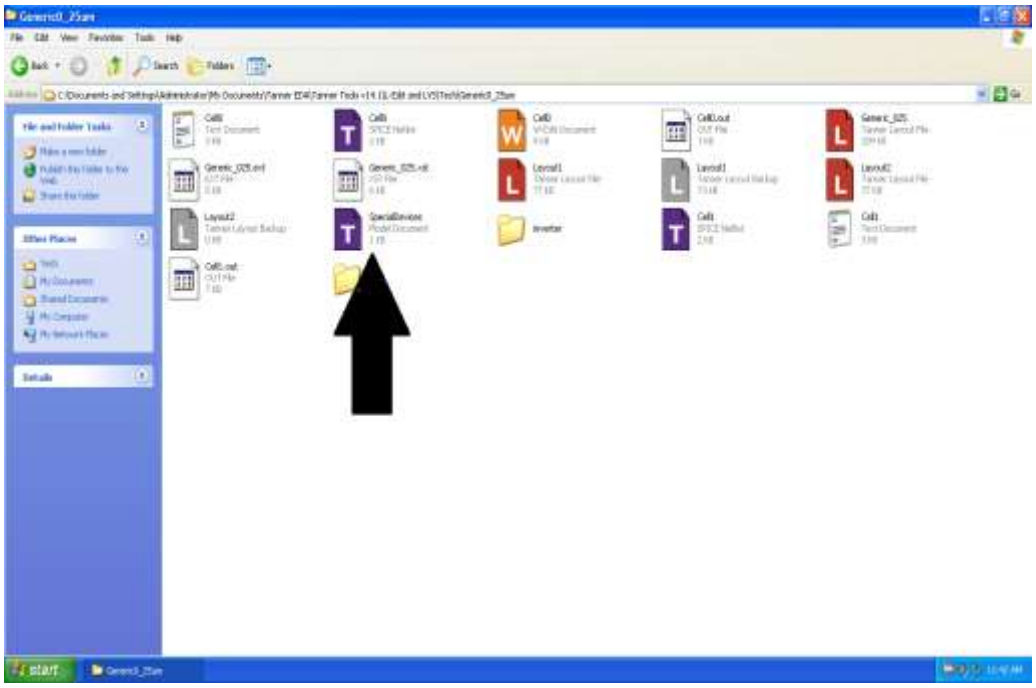
.op

.END

Spice file should look like this

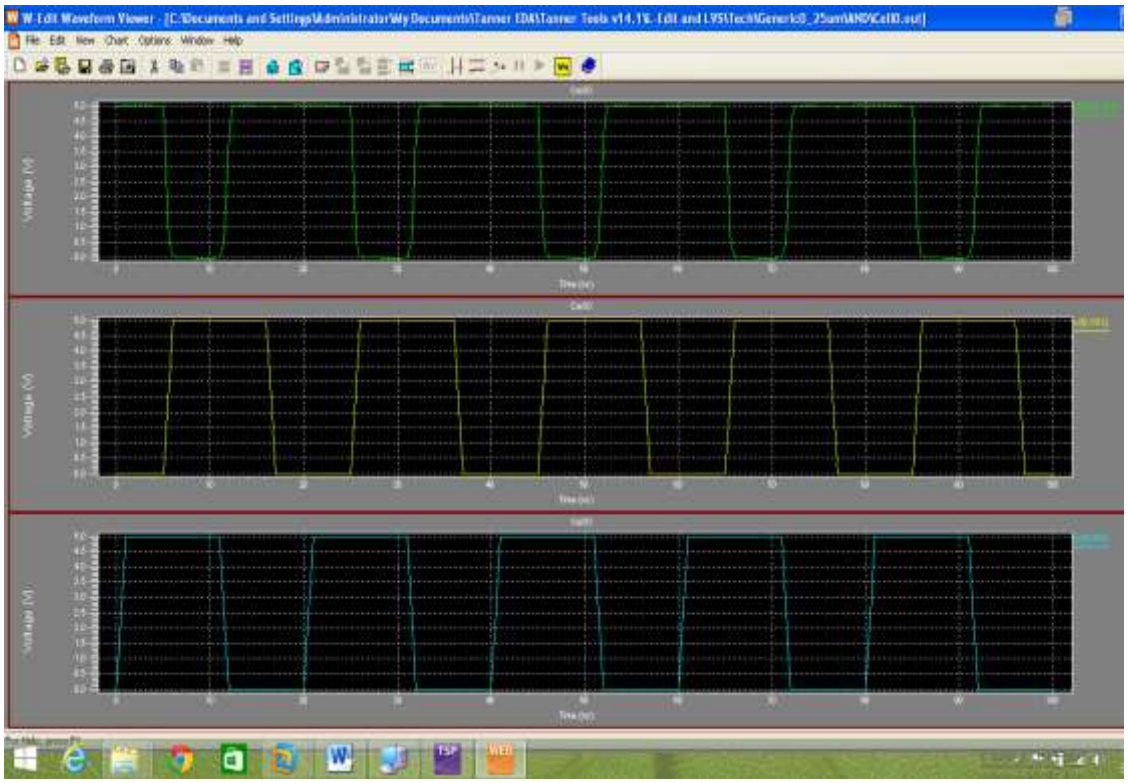


➔ Copy “Special Devices “and paste in your design(NAND) folder.



➔ Click “RUN”

Results



5. **Tasks:**

(For Students with even last digit of Student ID)

Design Layout of the following cells using CMOS 025Process.

- Inverter (Layout is uploaded on SLATE. Simulate it to view the results.)
- 2 input NAND (Layout + Simulation Results)
- 3 input NOR (Layout + Simulation Results)

All Transistors fixed sizes: Wn=1um, Wp= 2um, Ln=Lp=0.4um

Power Rails = Try to keep it as minimum as you can.

(For Students with odd last digit of Student ID)

Design Layout of the following cells using CMOS 025Process.

- Inverter (Layout is uploaded on SLATE. Simulate it to view the results.)
- 2 input NOR (Layout + Simulation Results)
- 3 input NAND (Layout + Simulation Results)

All Transistors fixed sizes: Wn=1.5um, Wp= 3um, Ln=Lp=0.6um

Power Rails = Try to keep it as minimum as you can.

Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

_____

_____

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_____

_____

_____

Student's signature and Date

Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)
  _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission
  _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed?
  _____/10
- ☐ **TOTAL:**
  _____/50

Feedback on student behaviour:

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2

- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2
- ☐ Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

_____

_____

_____

_____

_____

Lab Engineer's signature and Date

Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisified
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedabck is for LAB session: LAB Number: _____, Date: _____
- ☐ General (to provide feedback on a persistent practice/ocurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

This feedback is:

- ☐ For a Particular
- ☐ Who conducted the LAB? _____
- ☐ Actual Start time: _____ Total Duration of Lab: _____
- ☐ Instruction Duration: _____ Practical Duration: _____
- ☐ LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- ☐ Had the theory related to lab been covered in theory class? Yes/No

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

Instruction	Was duration of instruction session adequate?	-2	-1	0	+1	+2

Session	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
Staff	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2
	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
Equipment	Performance of Electronic Instruments?	-2	-1	0	+1	+2
	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2
	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

_____

_____

_____