VLSI Lab

LABORATORY MANUAL

Spring 2019

LAB 08

Title of Lab Experiment: Layout design of sequential circuits using available CAD tools using Gate Matrix mehtod

Engr. Rashid Karim

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STUDENT NAME ROLL NO SEC

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LAB ENGINEER SIGNATURE & DATE

MARKS AWARDED: /10

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LAB:	08	Layout design of sequential circuits using available CAD tools using Gate Matrix method

1. Learning Objectives:

a. Sequential digital circuits
b. Layout design using Gate matrix method

2. Equipment Required:

Software : L-Edit

3. Introduction:

Digital electronics is the basis of modern technological advancements. Digital devices are created using the principles of Boolean logic. Boolean logic, based on the nature of the outputs, is separated into combinational logic and sequential logic. Each type of logic can be used to implement different digital elements used today.

Combinational Logic

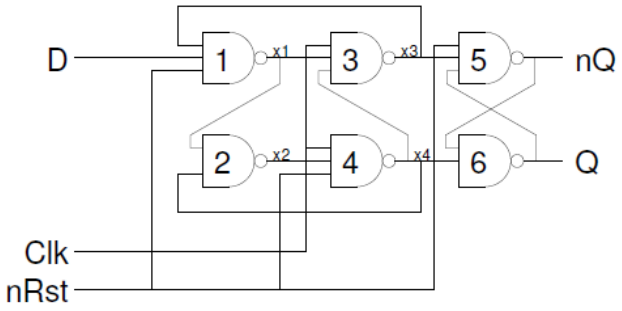
In combinational logic, the output is a function of the present inputs only. The output is independent of the previous outputs; therefore it is sometimes, called ***time independent logic***.
Combinational logic is used to perform Boolean operation on binary input signals and binary data. The arithmetic and logic unit of a CPU performs combinational operations on the data string. Half adders, full adders, multiplexers, demultiplexers, decoders and encoders are also built based on the combinational logic.

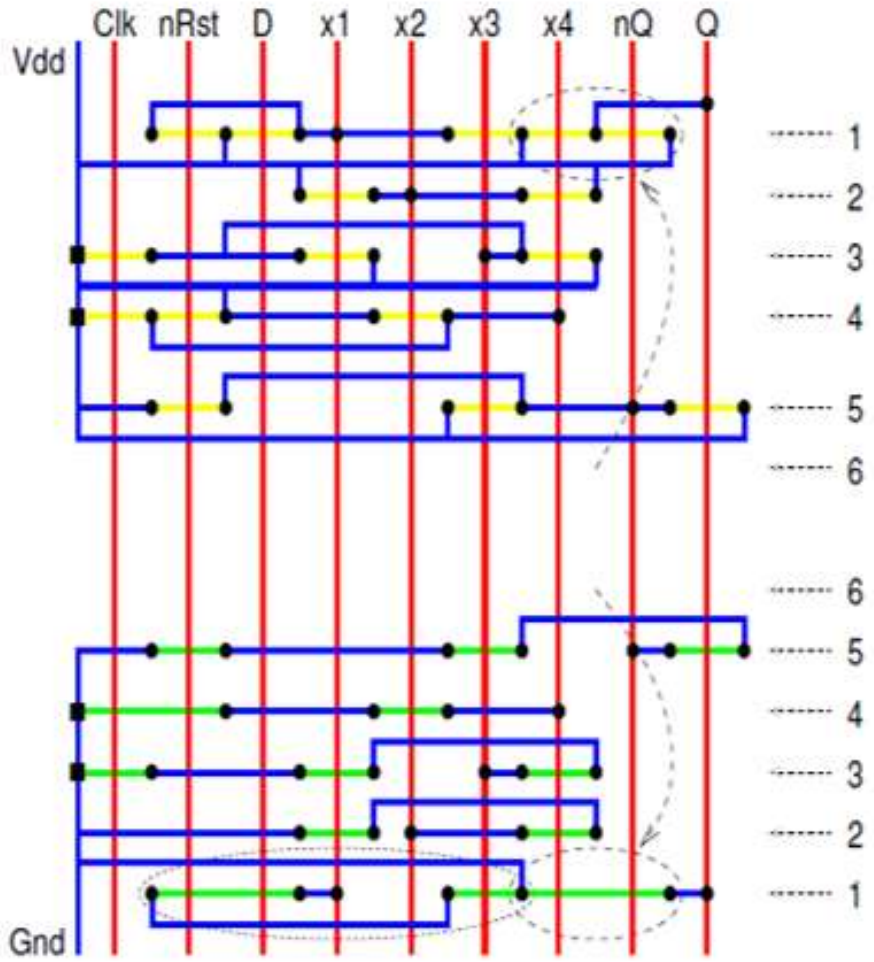
Sequential Logic

Sequential logic is the form of Boolean logic where the output is a function of both present inputs and past outputs. In most cases, the output signal is fed back into the circuit as a new input. Sequential logic is used to design and build finite state machines. The fundamental implementation of sequential logic is flip-flops. ***Flip-flops*** are designed to retain the state of the system, therefore, considered as a basic memory element.
Sequential logic is further divided into synchronous logic and asynchronous logic. In ***synchronous logic***, the logic operation is repeated cyclically through an oscillating signal supplied to every flip-flop in the circuit. This signal, often called the clock pulse, activates the logic circuit for a single operation.
The main advantage of synchronous logic is its simplicity. The main disadvantages of synchronous logic are the limited clock speed available and the requirement of a clock signal for every flip-flop. As a result, the speeds of the synchronous circuits are limited and energy wastage occurs when distributing the signal to every flip-flop element.

In ***asynchronous logic***, all the flip flops are not clocked at the same cycle. Rather, each individual flip-flop is clocked through the main clock signal or by an output of another flip-flop. Therefore, the speeds of the asynchronous logic circuits are much higher than the synchronous circuits. Even though asynchronous logic is efficient, they are difficult to design and implement and pose problems if two signals overlap.

Gate Matrix Method





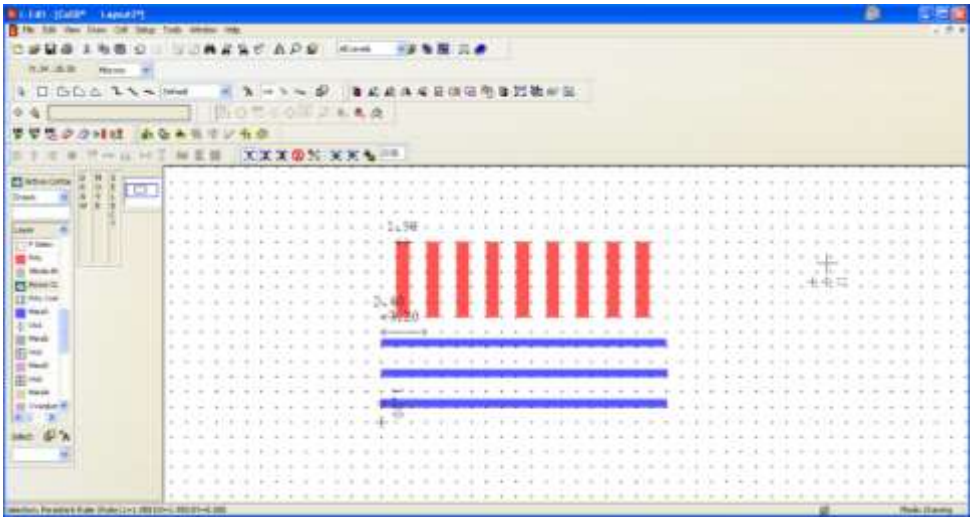
4. Procedure:

Designing layout of RAW D-flip flop.

Choose dimensions of your own choice.

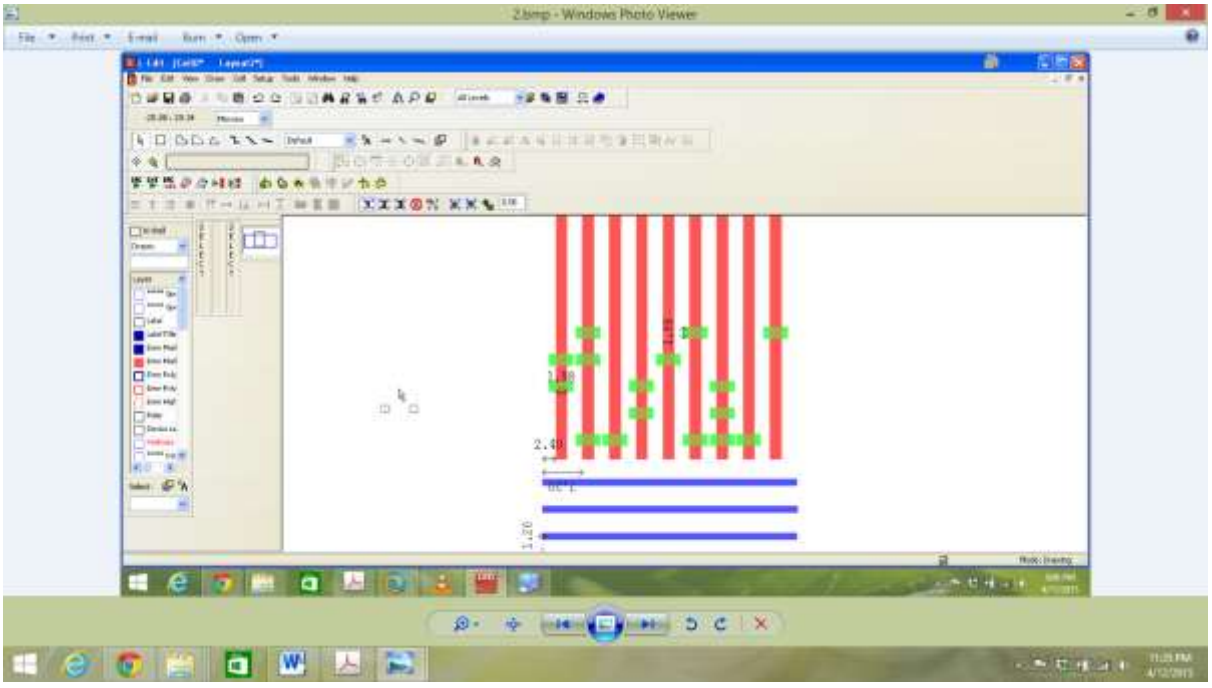
Step 1

Started from origin (0,0). Draw Metal1 layers. All dimensions are labeled.



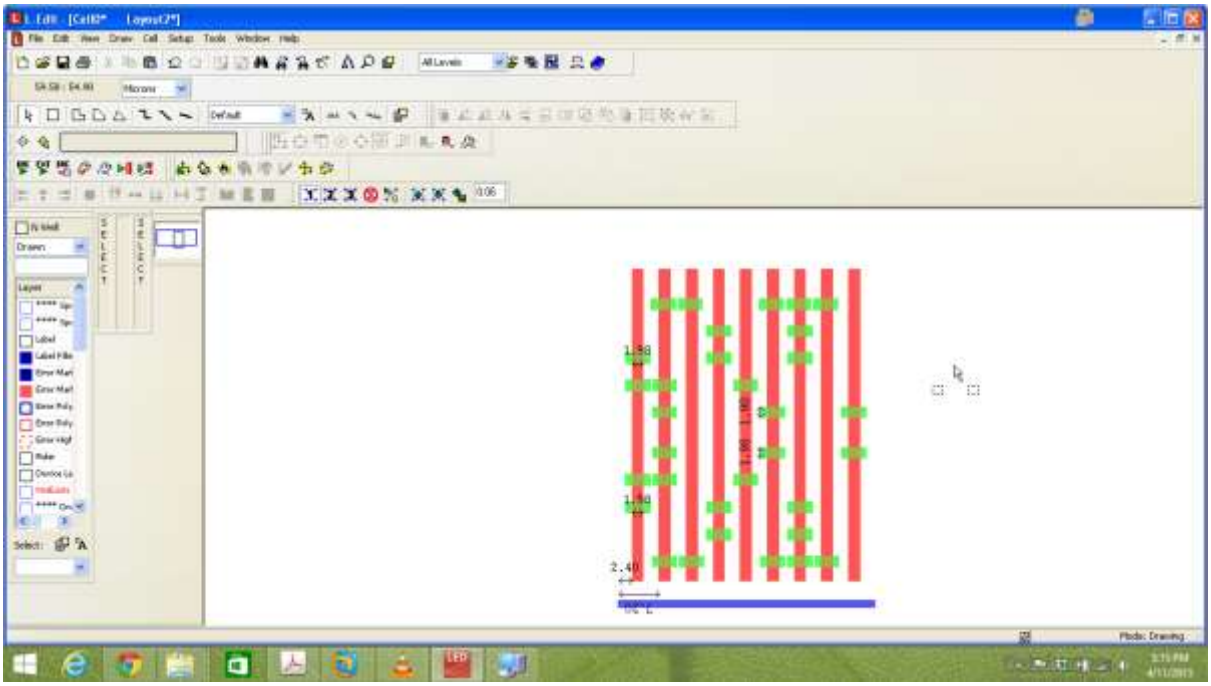
Step 2

Drawn Active layers of NMOS.



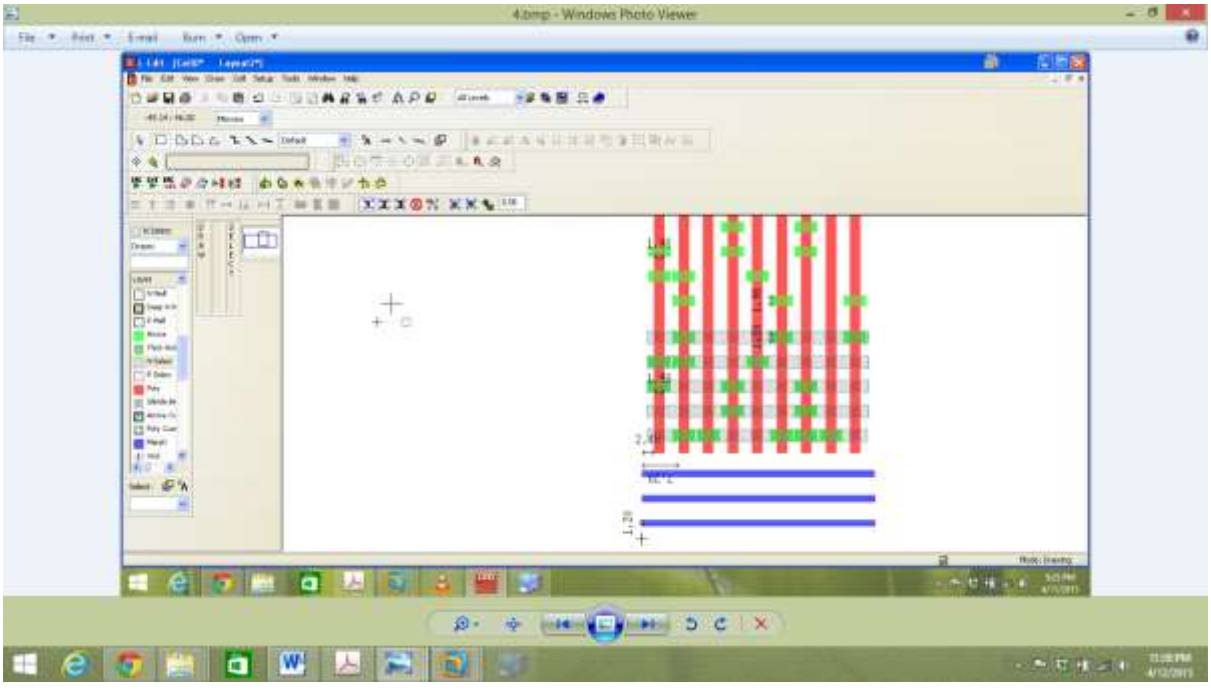
Step 3

Draw Active layers of PMOS.



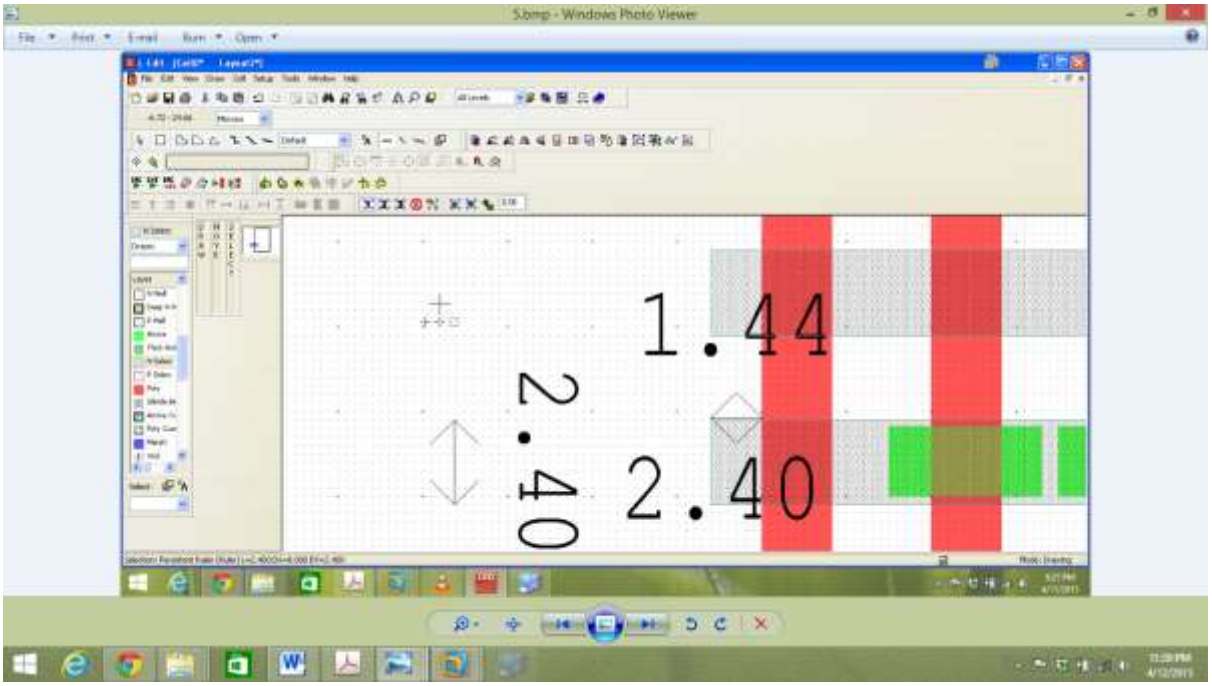
Step 4

Draw N-Select layers. One layer per row is an easy way to do that.



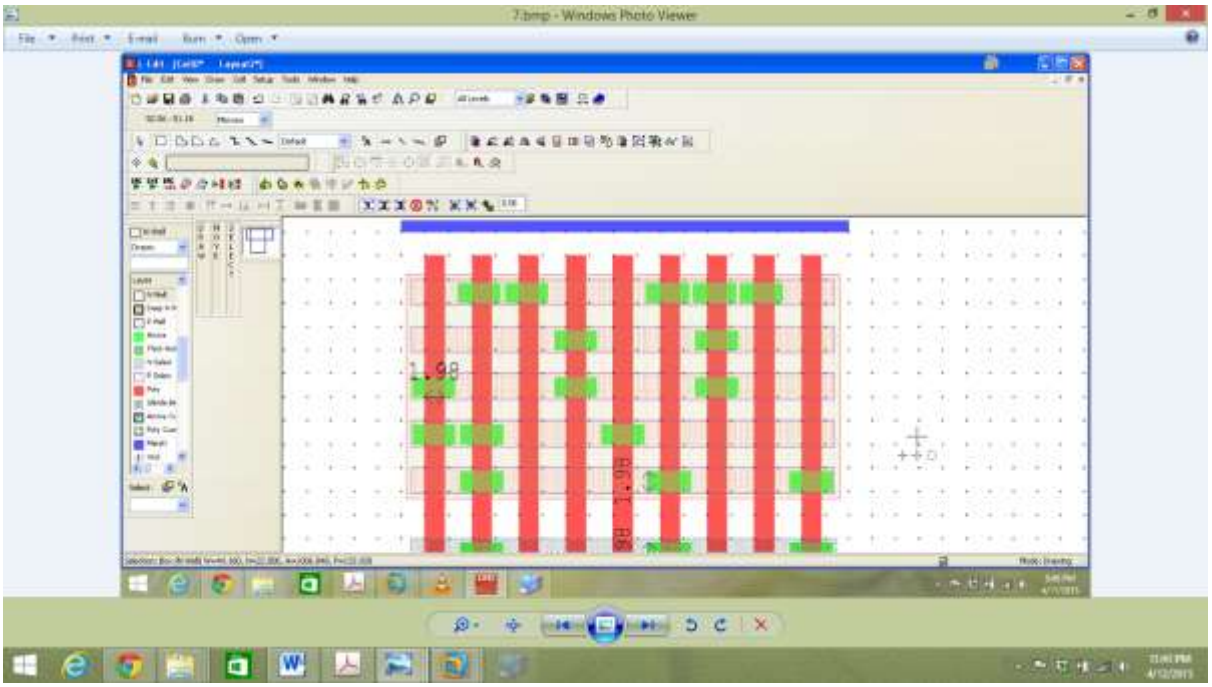
Step 5

Checked the dimensions.



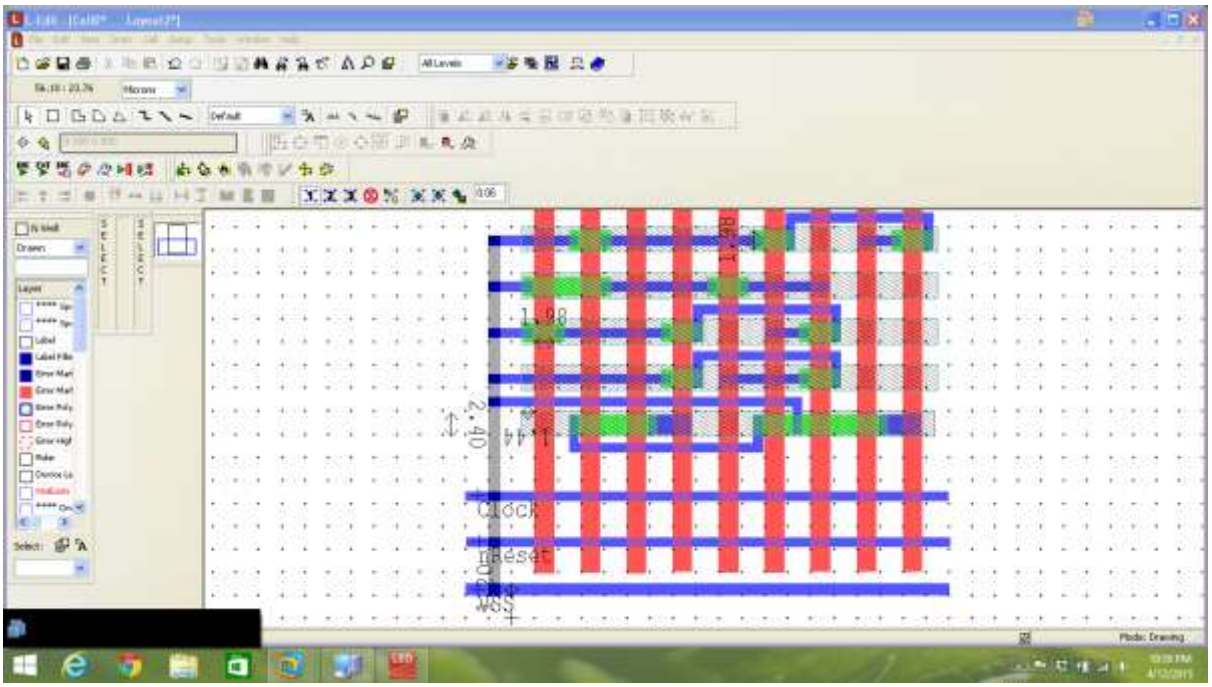
Step 6

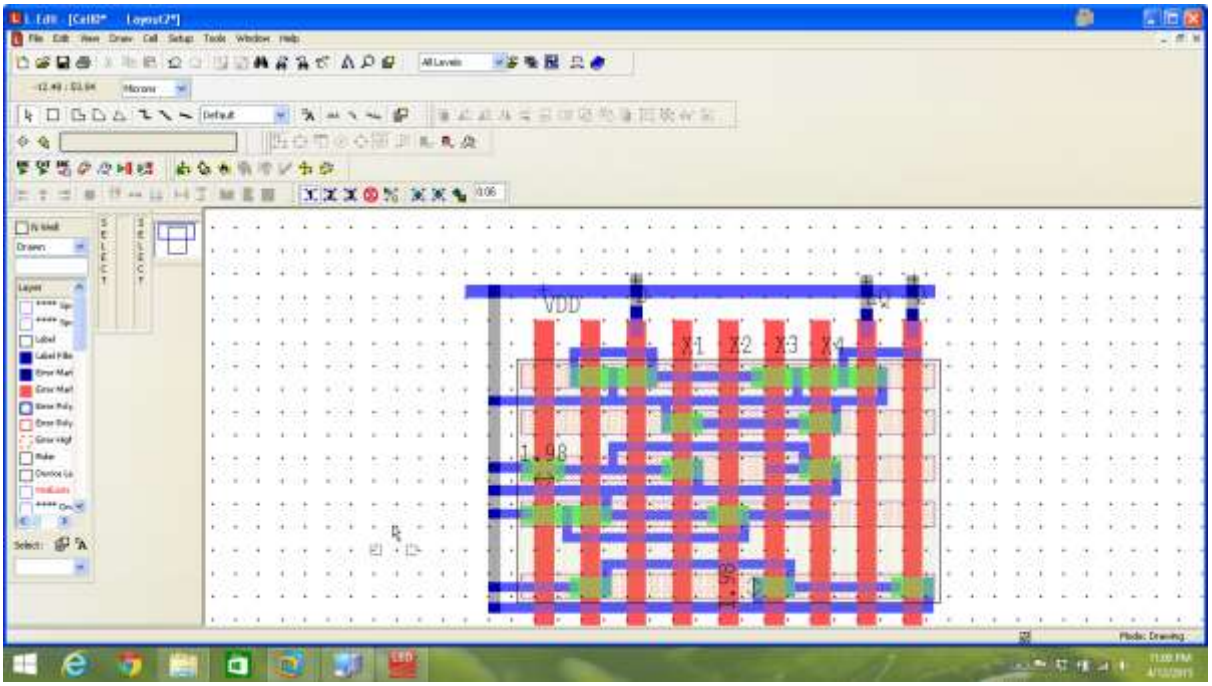
Draw a combined N-WELL for all PMOS devices.



Step 7

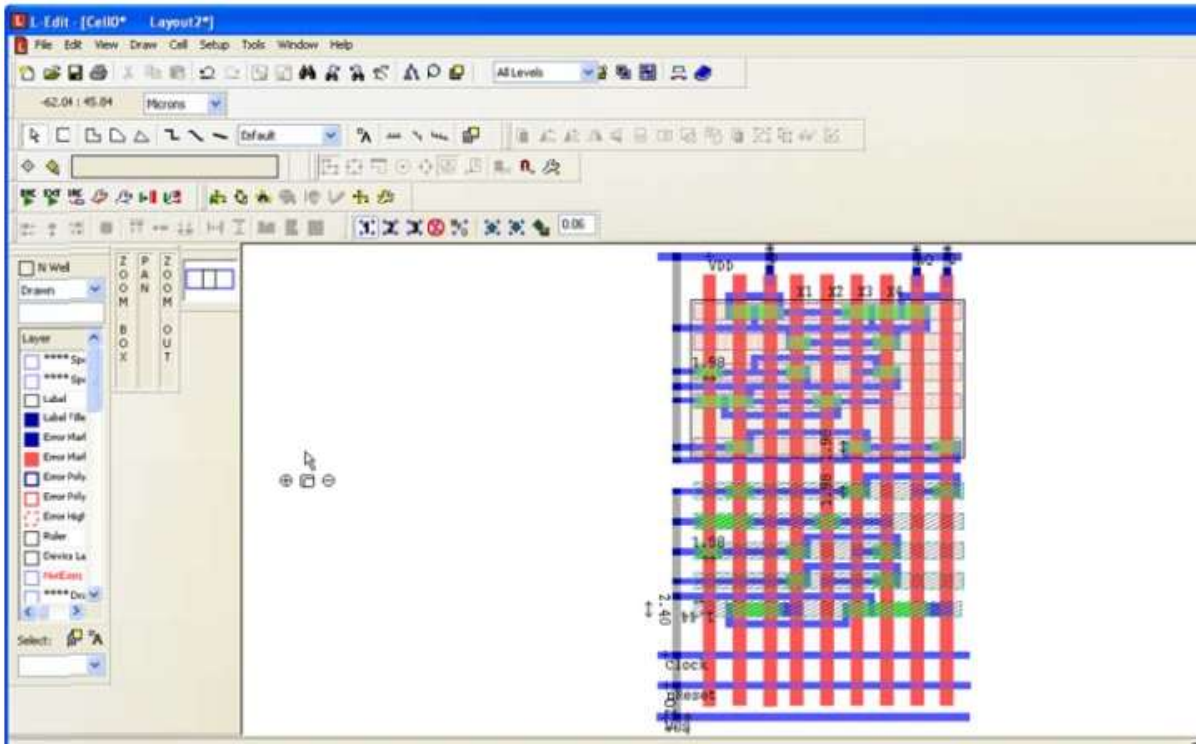
routing of NMOS & PMOS devices.





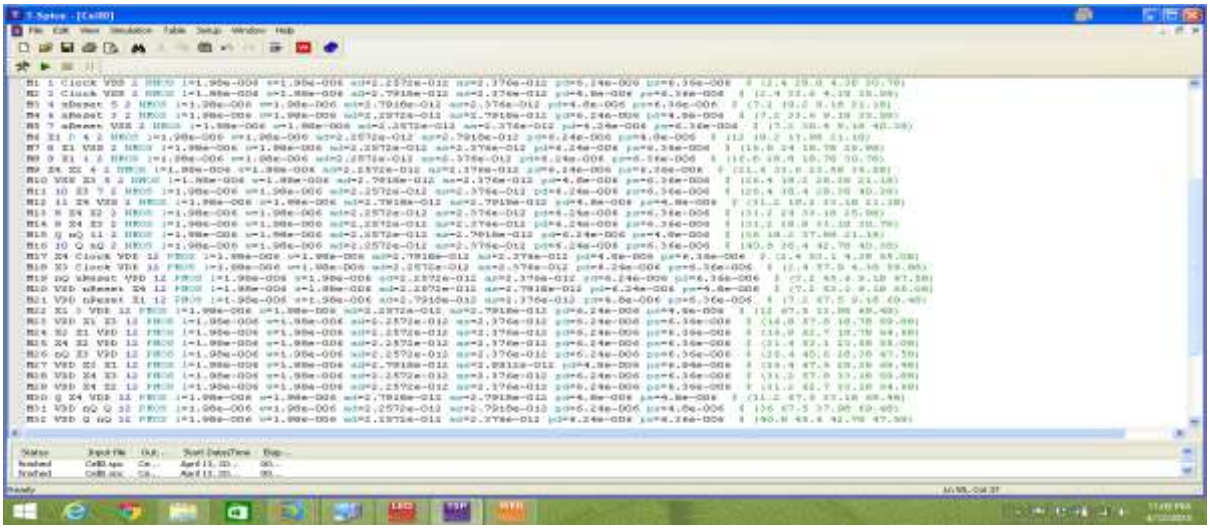
Step 8

Your complete design may look like this:



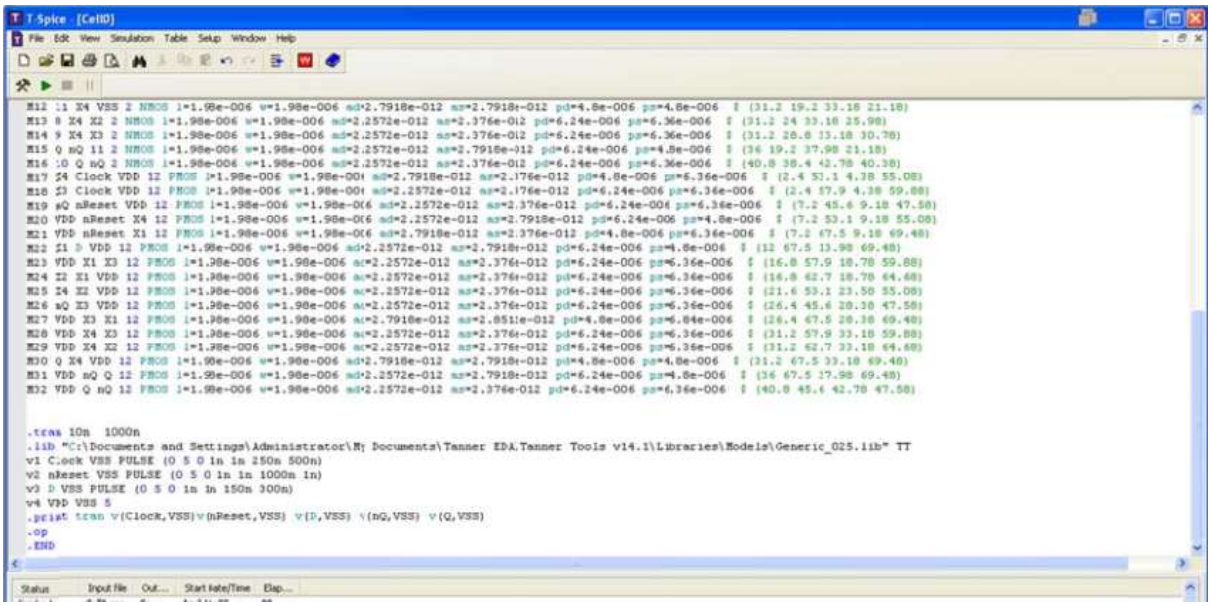
Step 9

Generated T-Spice file (extract)



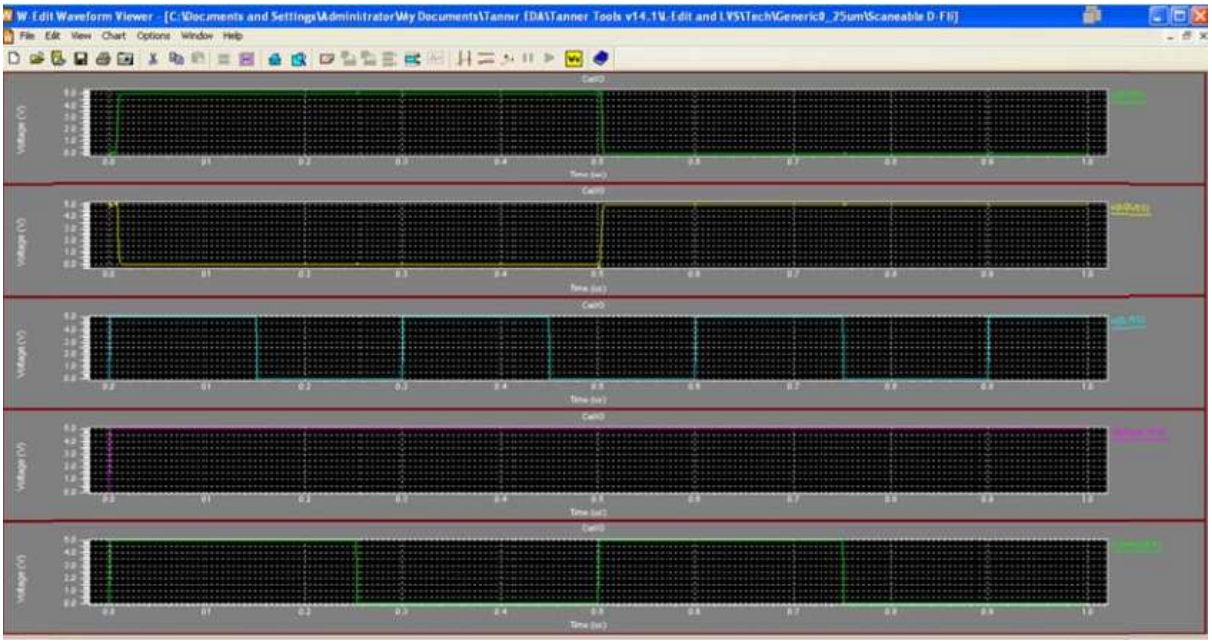
Step 10

Entered simulation commands.



Step 11

OUTPUT Waveform:



5. Task :

Make layout of D-Flip Flop.

Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

_____

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Student's signature and Date

Student Evaluation by the Lab Engineer:

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)
  _____/30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission
  _____/10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed?
  _____/10
- ☐ **TOTAL:**
  _____/50

Feedback on student behaviour:

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1 0 1 2

- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
- ☐ Did the student cause any distraction during the Lab? -2 -1 0 1 2
- ☐ Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

_____

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Lab Engineer's signature and Date

Student's feedback: [Separate this page; fill it; drop in the Drop Box.]

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisified
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedabck is for LAB session: LAB Number: _____, Date: _____
- ☐ General (to provide feedback on a persistent practice/ocurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

This feedback is:

- ☐ For a Particular
- ☐ Who conducted the LAB? _____
- ☐ Actual Start time: _____ Total Duration of Lab: _____

Layout design of sequential circuits using available CAD tools using Gate Matrix method	LAB:08

- Instruction Duration: _____ Practical Duration: _____
- LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- Had the theory related to lab been covered in theory class? Yes/No

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

Instruction Session	Was duration of instruction session adequate?	-2	-1	0	+1	+2
	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
Staff	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2
	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
Equipment	Performance of Electronic Instruments?	-2	-1	0	+1	+2
	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2
	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

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