EE309 VLSI
ASSIGNMENT #2

Assignment start date: 26-02-2019 **Assignment deadline: 12-03-2019 @in class**

Assessment for the CLO-02: Design transistor level, stick and layout diagrams of simple digital designs using MOS technologies (static NMOS, static CMOS, dynamic CMOS, Pass transistor and Transmission gate CMOS, Pseudo NMOS and PMOS, Complementary Pass Transistor CMOS)

- You are required to design a complete mask level layout of the following gates/compound gates using specifications/restrictions given below.
- Use Tanner's L-Edit for drawing layout designs and simulations.
- No need to submit simulation results of transistor level/schematic designs for this assignment.
- Only simulation results of a mask level/layout design are required.
- Technology to be used is static CMOS logic

GATES/COMPOUND GATES

(1) $F' = (A.B + C)(D.EF + G + H + IJ)$

(2) 2 x1 MUX

(3) $X' = (A + F + B) + (C + DE) + G$

- You need to find how to draw the transistor level diagram for 2 inputs XNOR gate.

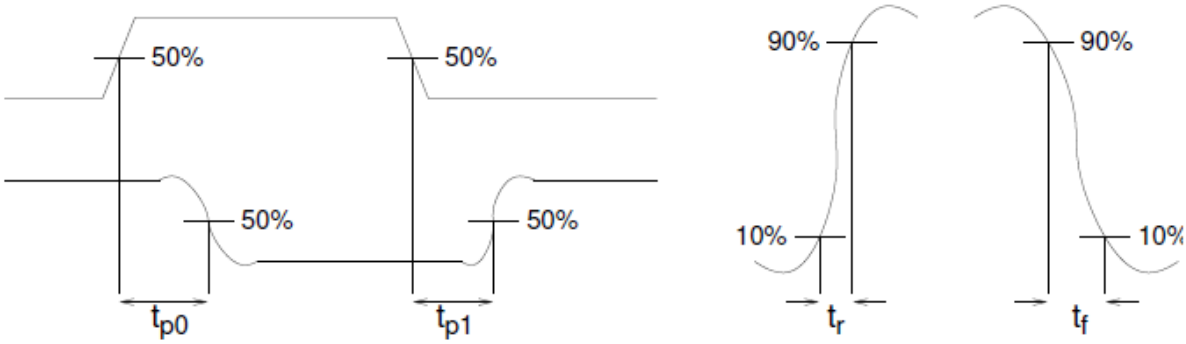
PERSONAL RESTRICTIONS

Please see following table for personal design restrictions.

Last digit of Student ID	Gates to design	CMOS Process	NMOS Size
1 and 7	3	CMOS025	$W = 1.0um, L =$ 0.4 um
0 and 9	1	CMOS025	$W = 1.2\ um, L =$ 0.6 um
4 and 6	3	CMOS025	$W = 1.2\ um, L =$ 0.8 um
3 and 8	2	CMOS025	$W = 1.4\ um, L =$ 0.3 um
2 and 5	1	CMOS025	$W = 1.6\ um, L = 0.5$

For PMOS, L (length) is same as NMOS. Keep W of PMOS 3 times that of NMOS.

MEASUREMENTS

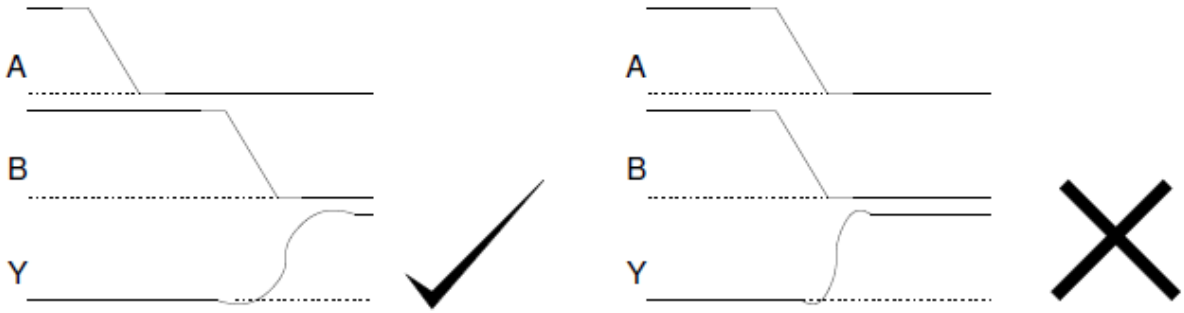


- Propagation delays are measured based on 50% of VDD.
- Rise and fall times are measured based on 10 and 90% of VDD

SIMULATION CONDITIONS

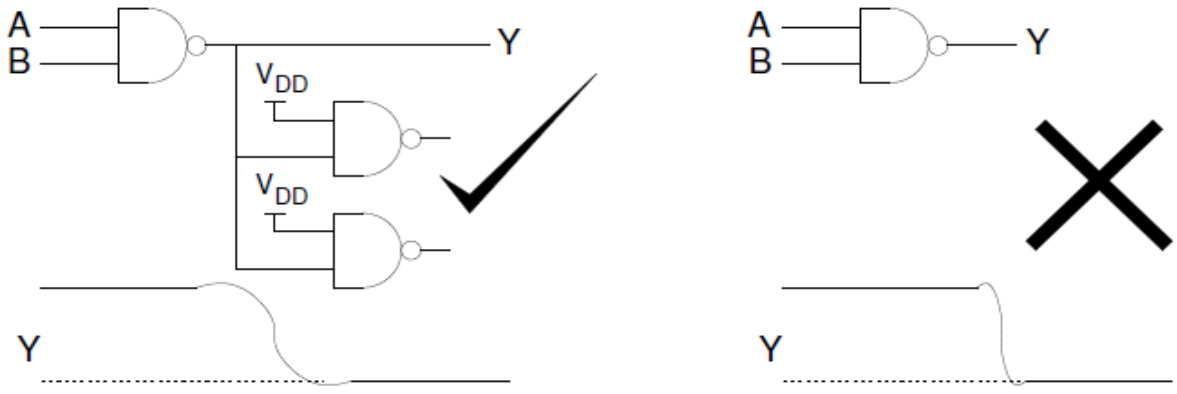
The measured performance of a gate will depend on the input drive conditions and the output load conditions. For useful results, we must ensure realistic drive and load conditions.

- **Do not allow 2 inputs to change simultaneously.**



- **All simulations loaded**

Load should be in proportion to the load experienced in the real circuit.

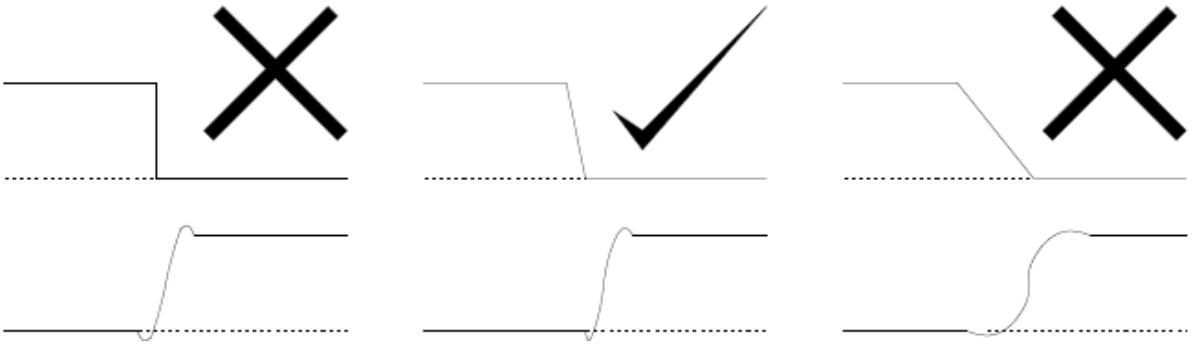


Use **3 inputs NOR gate** as a load. Keep dimensions (W and L) of the NAND gate same as of your design.

Remember to record the output at Y rather than at the output of one of the load devices!

- **Reasonable input slopes**

  -Not much faster nor much slower than the resulting output slope



SUBMISSION

You are required to write a report not more than 5 pages for the assignment. Information to be included in the report:

- Transistor sizes
- Transistor and stick diagrams (hand or Microsoft Visio-drawn)
- Area of gates (length and width) with abstract diagram; rise and fall times in tabular form
- Output & input waveforms showing the correct operation of the gates
- Print out of layout diagrams from L- Edit
- References if any

You are required to keep a copy of your design for a possible demo/quiz.

Only hard copy of the report is required for this assignment.

Plagiarized assignments will be dealt in accordance with the plagiarism policy.

There is no facility of late submission for this assignment. It is made clear that reports received after the deadline will not be marked.

Rashid Karim @ 26-02-2019