VLSI
MINI DESIGN PROJECT

Assignment start date: 02-04-2019 **Assignment deadline: 24-04-2019 @in Lab**
Assessment for the CLO-02: Design transistor level, stick and layout diagrams of simple digital designs using MOS technologies (static NMOS, static CMOS, dynamic CMOS, Pass transistor and Transmission gate CMOS, Pseudo NMOS and PMOS, Complementary Pass Transistor CMOS)

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8 Bits ALU unit Design

Note: It is not a group project

Design and Implement 8 bits ALU on L-Edit (till layout) with the following functionalities:

Arithmetic functionalities: AND, OR, XOR, XNOR, NAND, NOR, NOT,

Logical functionalities: Addition, Subtraction, Comparison, Right shift, Left Shift

Hint: You need to start from 1 bit system. Once completed, use bitslice technique, and convert it into 16 bits. Your bitslice and gate matrix lecture slides will help you a lot.

Optimized design (in terms of area, speed, delay) will get more marks.

Common Cell Specifications:

- Technology**:** 0.25 um CMOS
- All transistor fixed sizes: $W_P = 2.0\ um$, $W_N = 2.0\ um$, $L_P = L_N = 2.0\ um$
- Horizontal i/o in metal1 (including power/ground and global signals)
- Vertical i/o in metal2 (aligned on 1.2 um grid)
- Power rails: 1.2 um (all other dimensions kept to a minimum)
- Cell aligned to origin (0,0)
- Gate matrix construction (where possible)

Submission:

You need to write a report of at most 20 pages. Please include following in your report:

1- References

2- Design logic (step by step) of each of the arithmetic and logical functionalities on paper

3- 1 bit slice design (Gate level design on paper and layout design on L-Edit)

4- 8 bits slice design (Gate level design on paper and layout design on L-Edit)

5- Simulation results and Spice code of 1 bit and 8 bits systems

6- Comment/Reasons for wrong results if any

7- Conclusion/ Recommendation for design improvement

8- Transistor sizes, area of the design, rise and fall time, propagation delays of the cells

9- You need to submit the soft copy of the report (on slate) and hard copy (in class or office). Please keep a record of your design for the demo.

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10- Plagiarized assignments will be dealt with plagiarism policy.

11- Demo schedule of the assignment will be announced later.

12- The mini design project is worth 5 absolute marks.

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