

# VLSI Lab

## LABORATORY MANUAL

Spring 2019



## LAB 10

**Title of Lab Experiment : Layout VS Schematic of  
Digital Circuits on available CAD Tools**

**Engr. Rashid Karim**

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STUDENT NAME

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ROLL NO

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SEC

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LAB ENGINEER SIGNATURE & DATE

**MARKS AWARDED:** /10

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**NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES),  
ISLAMABAD**

Prepared by: Engr. Furqan Mehmood

Version:

2.00

<b>Layout VS Schematic of Digital Circuits on available CAD Tools</b>	<b>LAB:10</b>
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Last Edited by: Engr. Aneela Sabir

Date: 10 April,2019

<b>LAB:</b>	<b>10</b>	<b>Layout VS Schematic of Digital Circuits on available CAD Tools</b>
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Verified by: Engr. Rashid Karim.

## 1. Learning Objectives:

- Implimentation of Layout and Schematic of CMOS Inverter
- Checking Layout VS Schematic of Inverter.

## 2. Equipment Required:

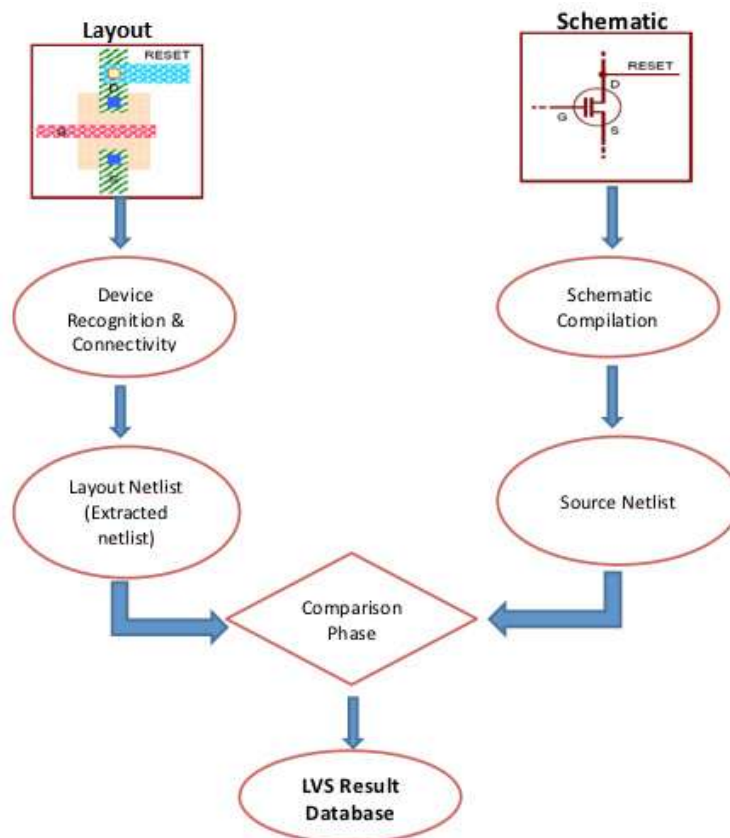
Software : L-Edit, S-Edit, LVS.

## 3. Introduction:

**Design rule check (DRC):** It verifies whether the designed layout can be manufactured by the fabrication lab with a good yield.

**Layout versus schematic (LVS):** It is a method of verifying that the layout of the design is functionally equivalent to the schematic of the design.

A successful Design rule check (DRC) ensures that the layout conforms to the rules designed/required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used

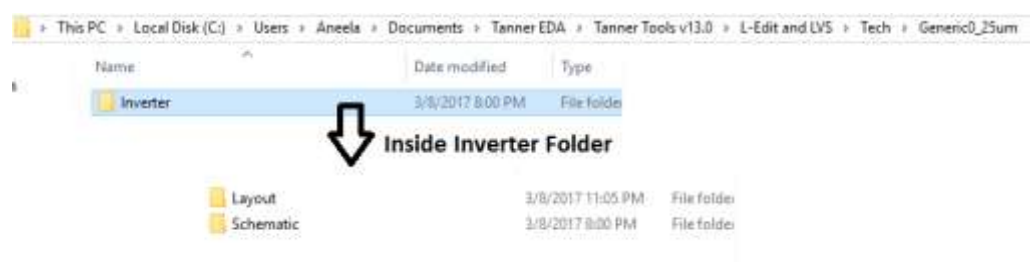


#### 4. Procedure:

**Create a folder named “Inverter” in a given path:**

C:\Users\Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\Tech\Generic0\_25um

Inside inverter folder, you have to create two new folders first named as Layout & second as Schematic.



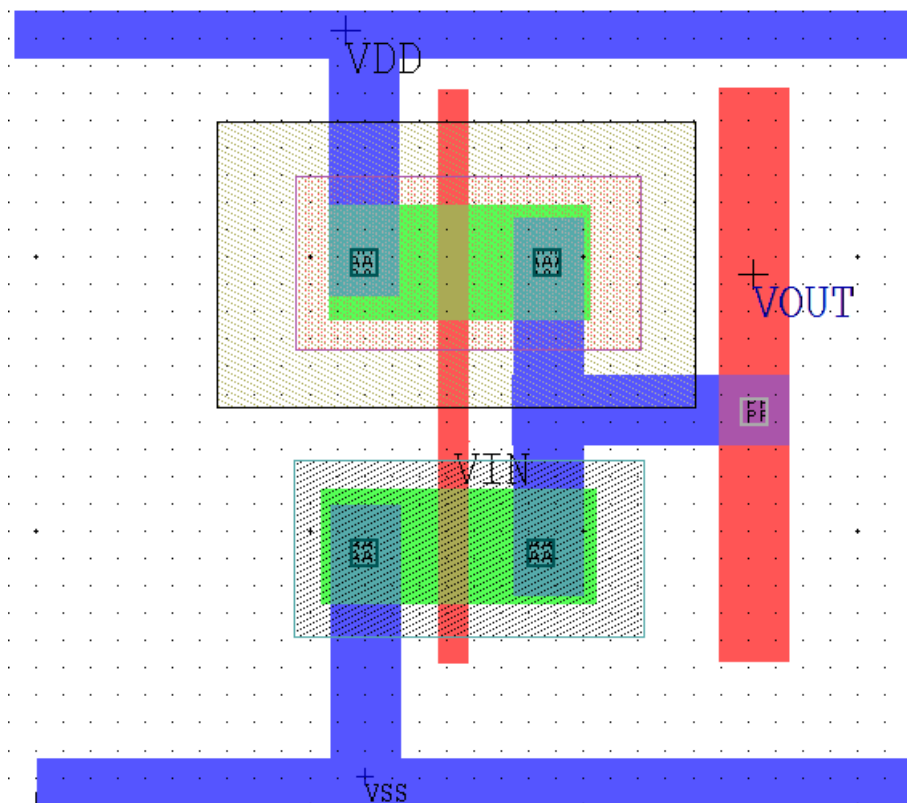
##### Step 1

Designing Layout of inverter. Save this layout in Inverter -> Layout Folder (created in last step).

Follow the steps of layout design of inverter as explained in previous labs.

Use given dimensions of Inverter:

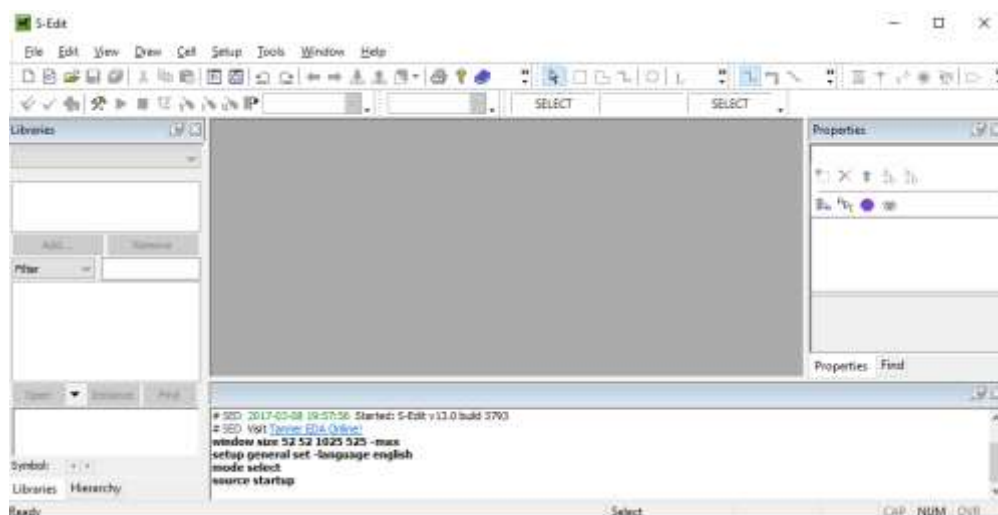
$$L_n = L_p = 0.6\mu\text{m} ; W_n = 0.3\mu\text{m}, W_p = 0.6\mu\text{m}$$



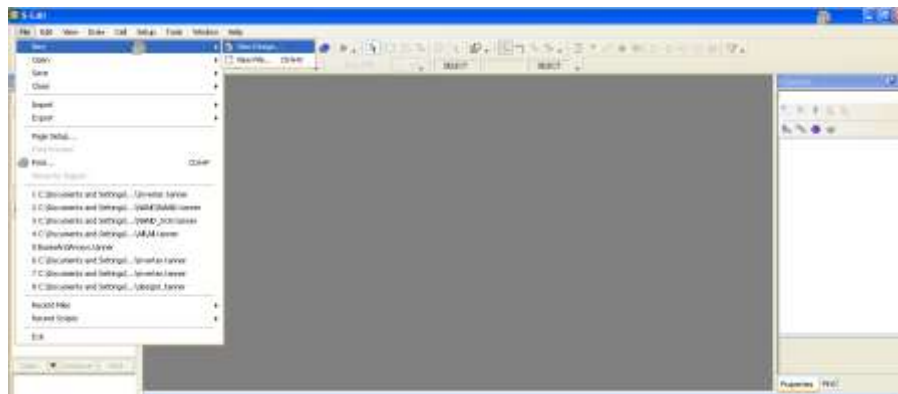
## Step 2

Now designing Schematic of inverter.

Run S-Edit .



File -> New -> New Design

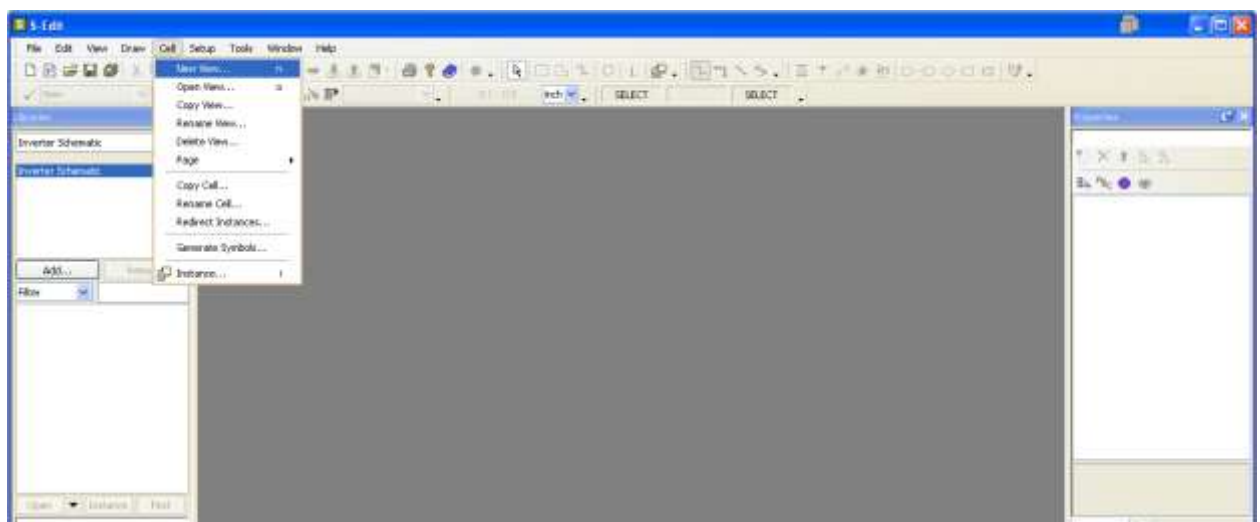


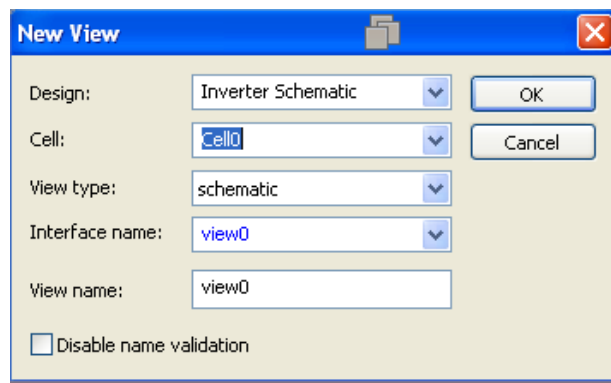
Design Name : Inverter Schematic

Creat in folder : C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools v13\L-Edit and LVS\Tech\Generic0\_25um\inverter\Schematic



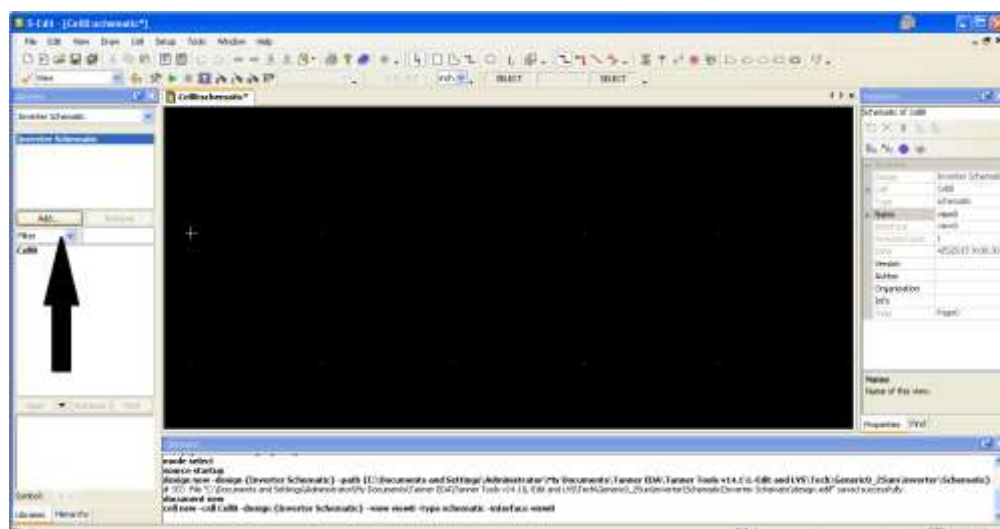
Cell -> New View





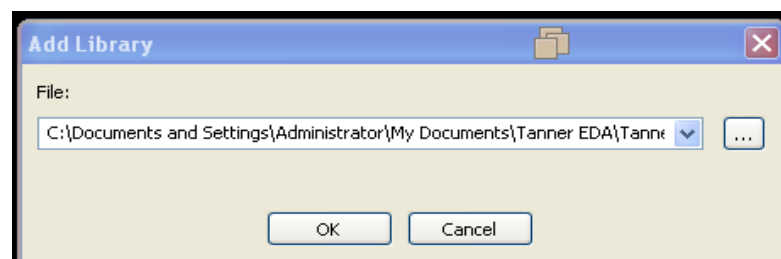
Click ok.

Laibraries -> ADD



Choose the following Laibrary

C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools v13\Libraries\All\All.tanner



Place the following elements from the list availble in Laibraries .

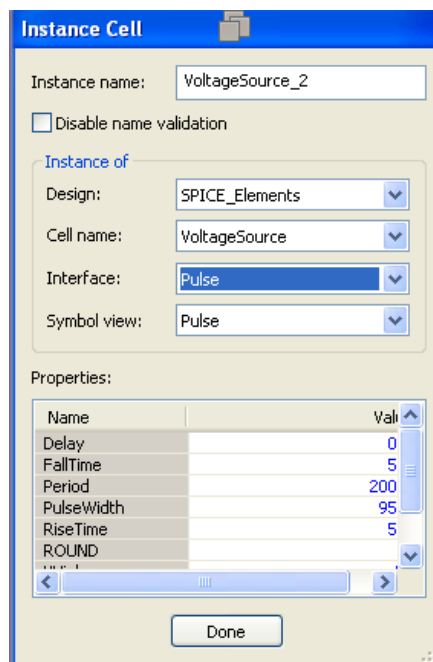
PMOS = Devices -> PMOS "Change name from PMOS\_1 To M1"

NMOS = Devices -> NMOS “Change name from NMOS\_1 To M2”

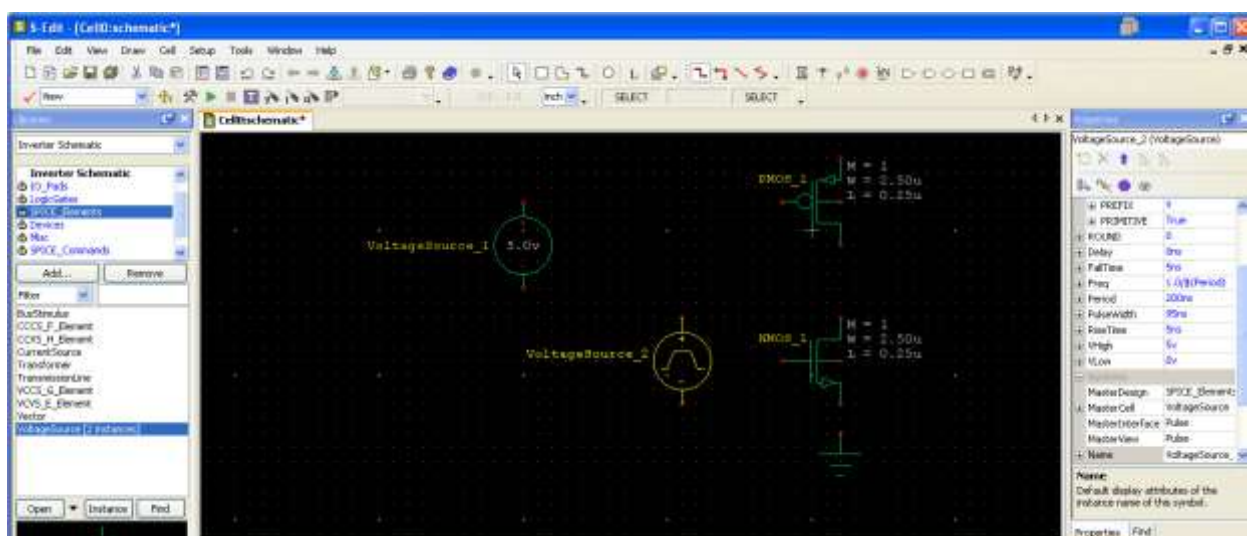
VDD = SPICE\_ELEMENTS -> Voltage Source

Ground = MISC -> Gnd

Input = SPICE\_ELEMENTS -> Voltage Source -> Interface (PULSE)



Design should look like this.

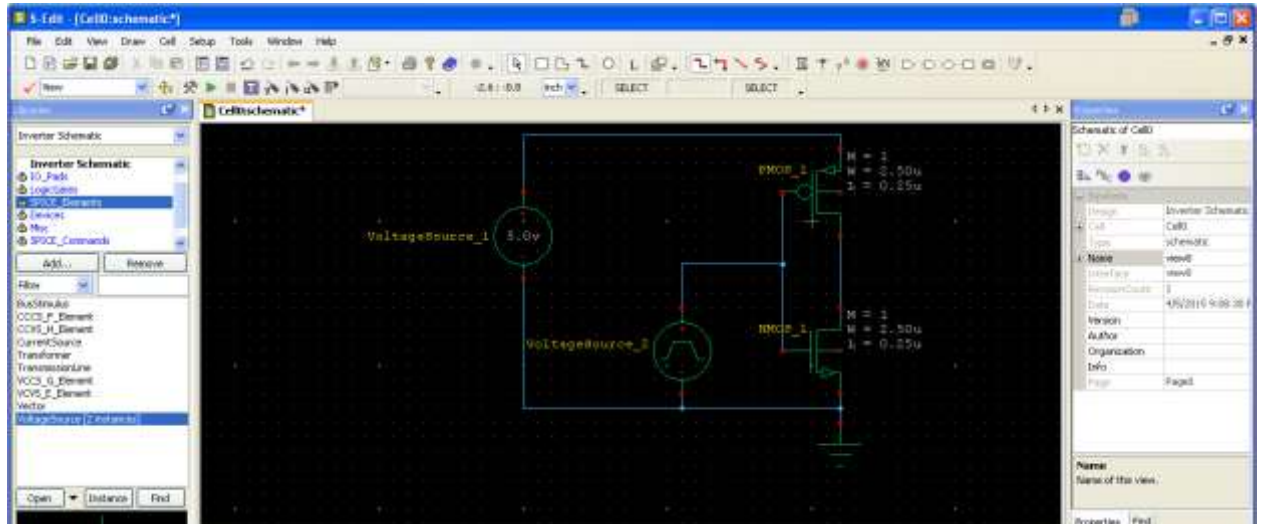


Now connect the circuit using wire.

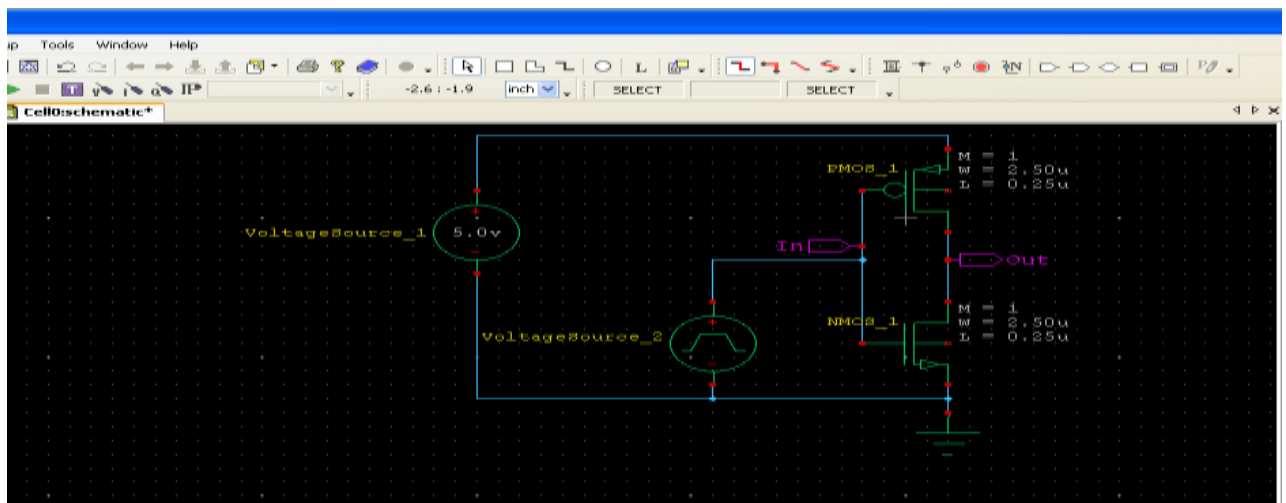




Design should look like this.

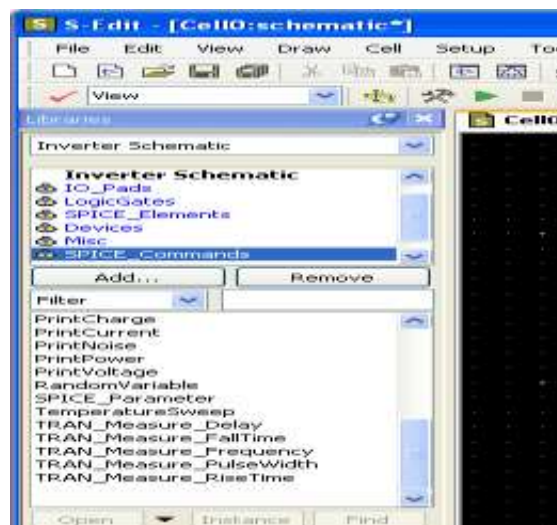


Place Input/Output ports.





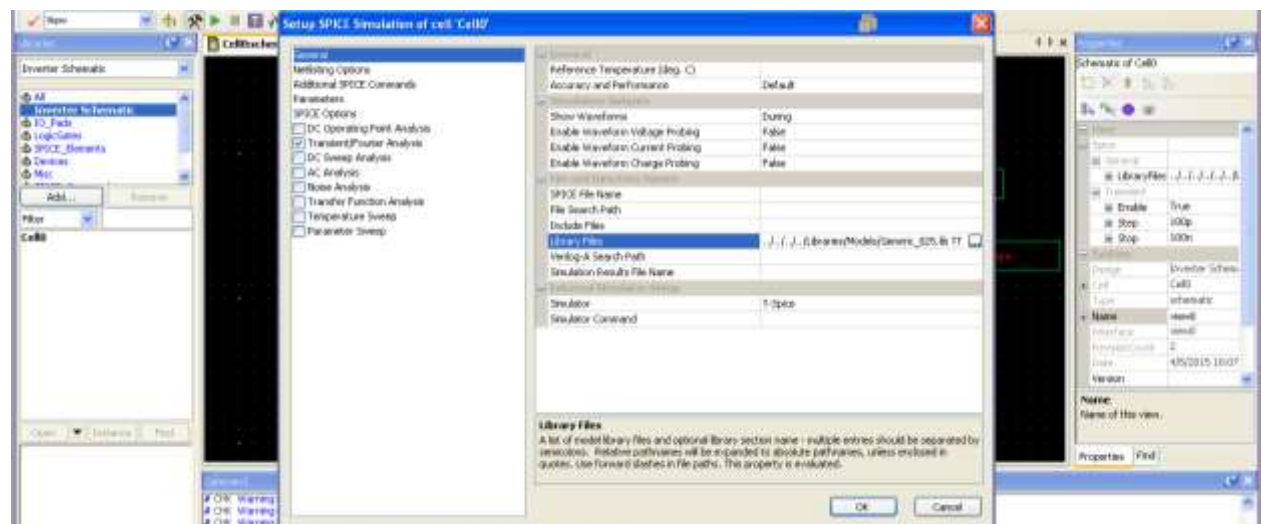
Print Voltages = SPICE Commands -> Print Voltage



Click on “RUN” Button and add the laibrary in “General”.

C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools v14.1\Libraries\Models\Generic\_025.

Type TT at the end .

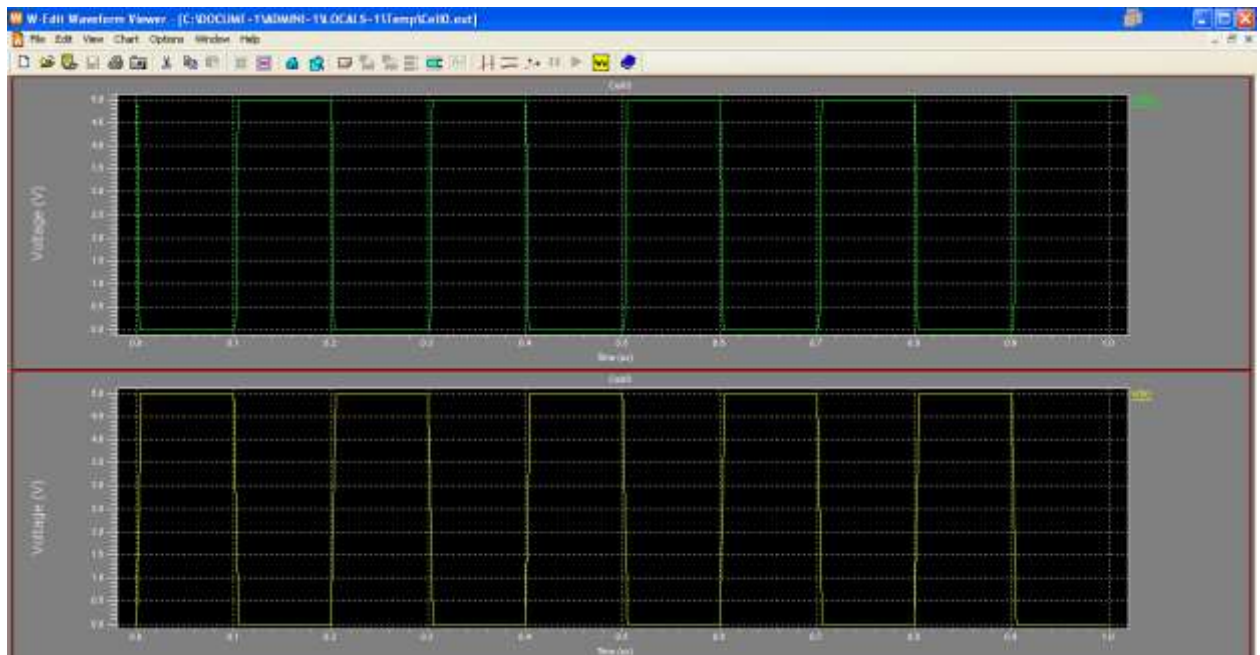


In “Transient enter the following values”.

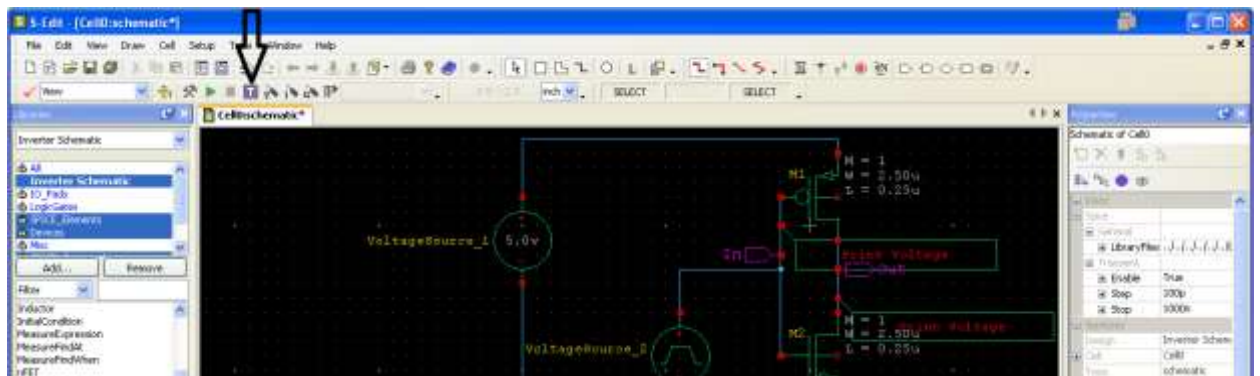
Stop Time =1000n

Maximum Time Step = 10p

Click “Start Simulaton Button”



Now Click Open in T-Spice.

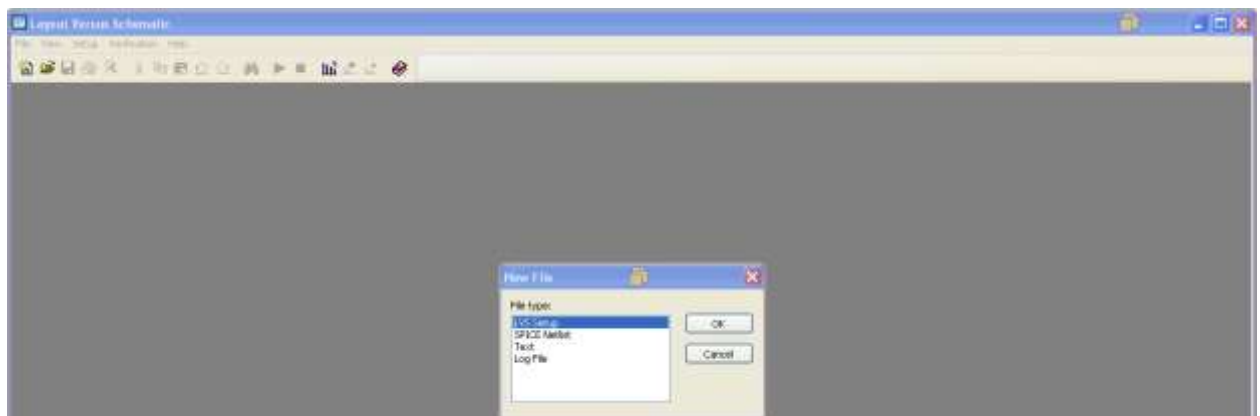


Save as This file in your design folder.

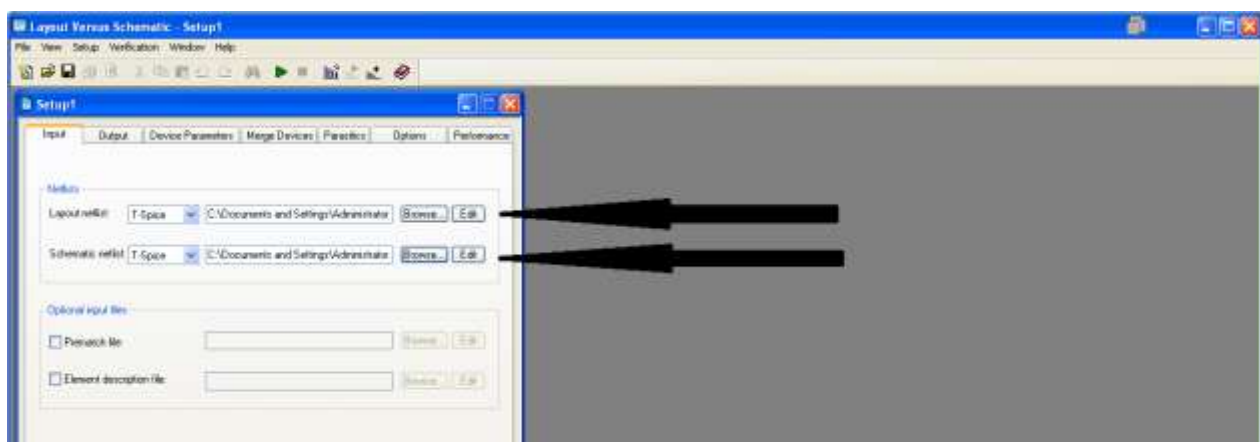


Now open "LVS program from Desktop icon"

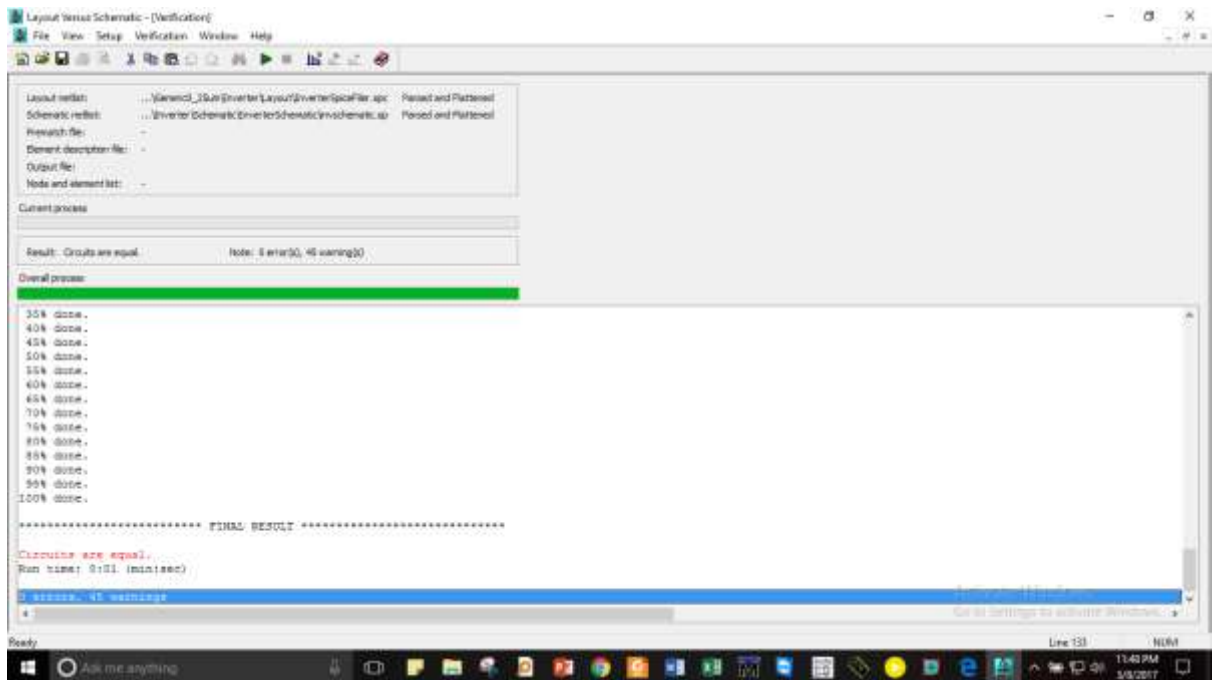
File -> New -> LVS Setup



Choose Layout Netlist and Schematic Netlist.



Click "RUN Verification".



## 5. Task :

### Question:

- 1) Design Layout of Inverter.
- 2) Design Schematic of Inverter.
- 3) Check “layout VS Schematic ” of your designs.

### Submission Declaration by the Student:

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

- ☐ I have performed all the practical work myself
- ☐ I have noted down actual measurements in this writeup from my own working
- ☐ I have written un-plagarised answers to various questions
- ☐ I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

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Student's signature and Date

**Student Evaluation by the Lab Engineer:**

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

- ☐ **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion)  
\_\_\_\_\_ /30
- ☐ **Lab Writeup:** Neatness, appropriateness, intime submission  
\_\_\_\_\_ /10
- ☐ **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposely changed?  
\_\_\_\_\_ /10
- ☐ **TOTAL:** \_\_\_\_\_ /50

**Feedback on student behaviour:**

**Encircle** your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

- ☐ Did the student join the lab at the start/remained in lab? -2 -1  
0 1 2
- ☐ Did the student remain focused on his/her work during lab? -2 -1  
0 1 2
- ☐ Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1  
0 1 2
- ☐ Did the student cause any distraction during the Lab? -2 -1  
0 1 2
- ☐ Was the student found in any sort of plagiarism? -2 -1  
0 1 2

Additional comments(if any) by the Lab Engineer:

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Lab Engineer's signature and Date

**Student's feedback:[Separate this page; fill it; drop in the Drop Box.]**

- ☐ Providing feedback for every lab session is optional. No feedback means you are satisfied
- ☐ The Lab Committee will consider only duly filled forms submitted within one week after the lab
- ☐ This feedback is for LAB session: LAB Number: \_\_\_\_\_, Date: \_\_\_\_\_
- ☐ General (to provide feedback on a persistent practice/occurrence in LABs).
- ☐ Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

**This feedback is:**

- ☐ For a Particular
- ☐ Who \_\_\_\_\_ conducted \_\_\_\_\_ the \_\_\_\_\_ LAB?
- ☐ Actual Start time: \_\_\_\_\_ Total Duration of Lab: \_\_\_\_\_
- ☐ Instruction Duration: \_\_\_\_\_ Practical Duration: \_\_\_\_\_
- ☐ LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
- ☐ Had the theory related to lab been covered in theory class? Yes/No

**Encircle** your choice. -2 means poorest/worst/extremely inadequate/irrelevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

<b>Instruction Session</b>	Was duration of instruction session adequate?	-2	-1	0	+1	+2
	How much did you understand about the practical?	-2	-1	0	+1	+2
	How much content was irrelevant to the practical?	-2	-1	0	+1	+2
	Did the instructor allowed Q/A and discussion?	-2	-1	0	+1	+2
<b>Practical</b>	Did you get sufficient time for practical?	-2	-1	0	+1	+2
<b>Lab Engineer</b>	Presence in lab at all time?	-2	-1	0	+1	+2
	Ability to convey?	-2	-1	0	+1	+2
	Readiness to help during practical?	-2	-1	0	+1	+2
	Readiness to discuss theoretical aspects?	-2	-1	0	+1	+2
	Helps in troubleshooting?	-2	-1	0	+1	+2
	Guides hows & whys of troubleshooting?	-2	-1	0	+1	+2
<b>Staff</b>	How friendly was the lab staff?	-2	-1	0	+1	+2
	Presence of staff throughout the lab session?	-2	-1	0	+1	+2

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	Impact of availability of staff on your practical?	-2	-1	0	+1	+2
	Performance of Electronic Instruments?	-2	-1	0	+1	+2
<b>Equipment</b>	Performance of Breadboard/experiment kit?	-2	-1	0	+1	+2
	Performance of circuit components esp. ICs?	-2	-1	0	+1	+2
<b>Overall</b>	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comments:

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