VLSI Lab

LABORATORY MANUAL Spring 2019



LAB 11

Title of Lab Experiment: Implementation of PLA structure using Pseudo NMOS Logic Engr. Rashid Karim

	MAI	RKS AWARDED:	/10
		LAB ENGINEER SIGNATI	JRE & DATE
STUDI	ENT NAME	ROLL NO	SEC

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD

Prepared by: Engr. Aneela Sabir Version: 1.00
Last Edited by: Engr. Aneela Sabir Date: 16th April,2019

Verified by: Engr. Rashid Karim.

Implementation of PLA structure using Pseudo	LAB:11
NMOS Logic	

LAB:	11	Implementation of PLA structure using Pseudo NMOS
		Logic

1. Learning Objectives:

a. Layout design and verification of Pseudo NMOS based digital designs

2. Equipment Required:

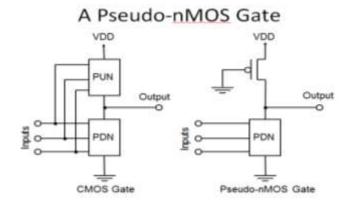
Software: L-Edit, T-Spice, W-Edit

3. Introduction:

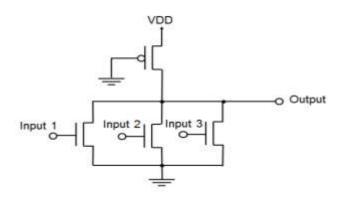
Static CMOS: Pros and Cons

- > Advantages: Static (robust) operation, low power.
- Disadvantages:
 - o Large size: An N input gate requires 2N transistors.
- ➤ Alternatives: Pass-transistor logic (PTL), pseudo-nMOS, dynamic CMOS.

A Pseudo-nMOS Gate



Pseudo-nMOS NOR



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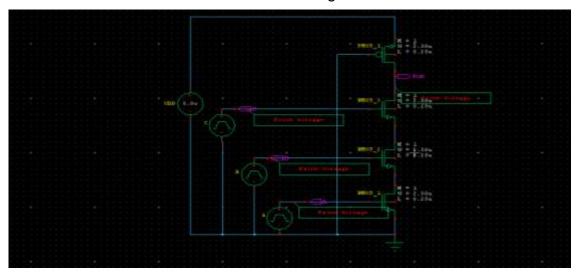
Negative Aspects of Pseudo-nMOS

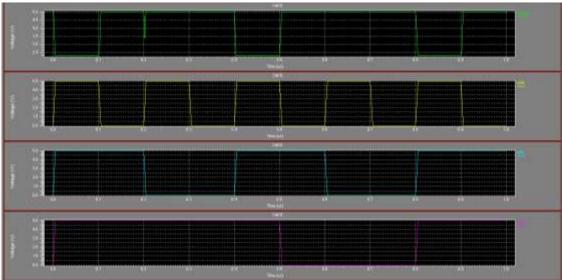
- > Faster gates mean higher static power.
- > Low static power means slow gates.

4. Procedure:

2-Input NAND Gate

Schematic verification of Pseudo NMOS using S-Edit.

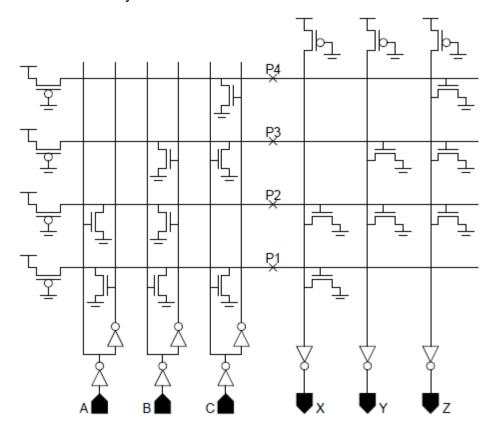




Implementation of PLA structure using Pseudo NMOS Logic LAB:11

5. Task:

Design an optimized layout for the transistor level diagram of the following PLA structure which has been implemented using Pseudo NMOS technology. Also, test its functionality.



Implementation of PLA structure using Pseudo NMOS Logic LAB:11

In s	submission Declaration by the Student: submitting this lab write-up to the Lab Engineer/Instructor, I hereby decla I have performed all the practical work myself I have noted down actual measurements in this writeup from my own wo I have written un-plagarised answers to various questions I have/have not obtained the desired objectives of the lab. asons of not obtaining objectoves (if applicable):		
	Student's signature and Date		
The ow	udent Evaluation by the Lab Engineer: e Lab Engineer can separate this page from the writeup and keep it for h n record. It must be signed by the student with date on it. Lab Work: objectives achieved (correctness of measurements, cal answers to questions posed, conclusion) /30 Lab Writeup: Neatness, appropriateness, intime submission /10 Troubleshooting: Were the student able to troubleshoot his/her wor was purposedly changed? /10 TOTAL: /50	cula	ations,
En	edback on student behaviour: circle your choice2 means poorest/worst/extremely inadequate/irreverse an average score, and +2 means best/most relevant/most adequate.	/lev	ant, 0
	Did the student join the lab at the start/remained in lab? 0 1 2 Did the student remain focused on his/her work during lab? 0 1 2	-2	-1 -1
	Rate student's behaviour with fellows/staff/Lab Engineer? 0 1 2	-2	-1

Implementation of PLA	A structure using Pseudo	LAB:11
NMOS Logic		
☐ Did the student cause an 0 1 2	y distraction during the Lab?	-2 -1
□ Was the student found in 0 1 2	any sort of plagiarism?	-2 -1
Additional comments (if any)) by the Lab Engineer:	
Lab Engine	er's signature and Date	
 □ Providing feedback for exactisified □ The Lab Committee will exafter the lab □ This feedabck is for LAB □ LAB Number:		e in LABs).
This feedback is: ☐ For a Particular ☐ Who conducted the LAB	?	
□ Actual Start time:		
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Implementation of PLA structure using Pseudo			LAB:11			
NMOS L	ogic					
□ Had the	iteup available before LAB? Yes/No with the Photo e theory related to lab been covered in theory class your choice2 means poorest/worst/extremely in werage score, and +2 means best/most relevant/m	s? <u>Yes</u> nadeq	<u>s/No</u> uate/	/irrev		
Instruction Session	Was duration of instruction session adequate? How much did you understand about the practical? How much content was irrelevant to the practical? Did the instructor allowed Q/A and discussion?	-2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -	-1 -1 -1	0 0 0	+1 +1 +1	+2 +2 +2 +2
Practical	Did you get sufficient time for practical?	-2	-1	0	+1	+2
Lab Engineer	Presence in lab at all time? Ability to convey? Readiness to help during practical? Readiness to discuss theoretical aspects? Helps in troubleshooting? Guides hows & whys of troubleshooting?	-2 -2 -2 -2 -2 -2	-1 -1 -1 -1 -1 -1	0 0 0 0 0	+1 +1 +1 +1 +1 +1	+2 +2 +2 +2 +2 +2 +2
Staff	How friendly was the lab staff? Presence of staff throughout the lab session? Impact of availability of staff on your practical?	-2 -2 -2	-1 -1 -1	0 0	+1 +1	+2 +2 +2
Equipment	Performance of Electronic Instruments? Performance of Breadboard/experiment kit? Performance of circuit components esp. ICs?	-2 -2 -2	-1 -1	0 0	+1 +1 +1	+2 +2 +2
Overall	Your overall rating for the whole lab session?	-2	-1	0	+1	+2

Other comm	nents:			
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