VLSI Lab

LABORATORY MANUAL Spring 2019



LAB 12

Title of Lab Experiment: Symbol generation of bsic digital designs using Pseudo NMOS Technology on S-Edit Engr. Rashid Karim

SEC	ROLL NO	STUDENT NAME	
URE & DATE	LAB ENGINEER SIGNATU		
/10	MARKS AWARDED:		

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD

Prepared by: Engr. Furqan Mehmood Version: 2.00
Last Edited by: Engr. Aneela Sabir Date: 18th April, 2019

Verified by: Engr. Rashid Karim.

LAB:12

LAB:	12	2 Symbol generation of basic digital designs using	
		Pseudo NMOS Technology on S-Edit	

1. Learning Objectives:

a. Symbol generation in S-Edit of Pseudo NMOS.

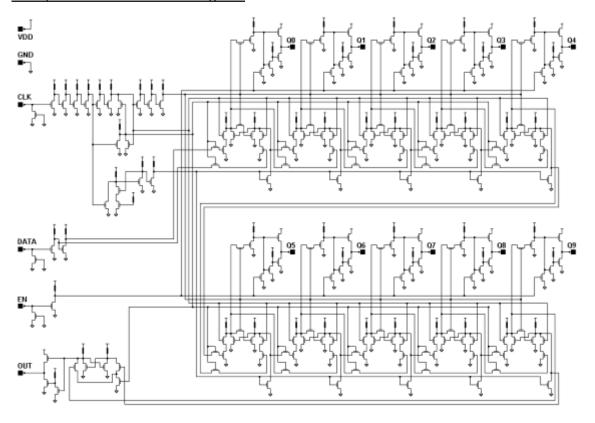
2. Equipment Required:

Software: S-Edit

3. Introduction:

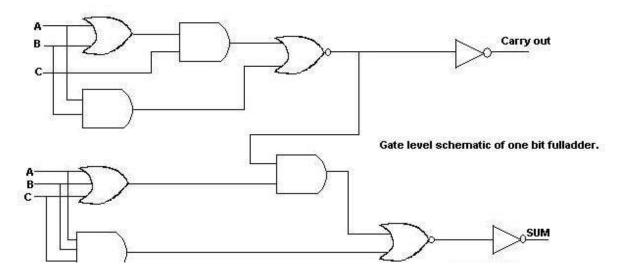
Block diagrams are typically used for higher level, less detailed descriptions that are intended to clarify overall concepts without concern for the details of implementation. Contrast this with the schematic diagrams and layout diagrams used in electrical engineering, which show the implementation details of electrical components and physical construction.

Complex transistor level diagram:



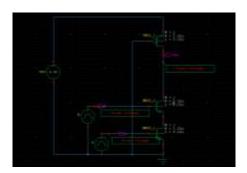
VLSI LAB	NUCES, ISLAMABAD	Page 2 of 10
----------	------------------	----------------------------

Simple and easy to understand Gate (symbol) level diagram:

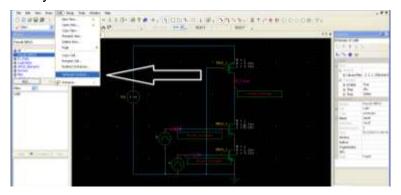


4. Procedure:

Symbol generation:



Cell -> Generate symbol



Modify



Symbol generated.



Now user-defined symbol:

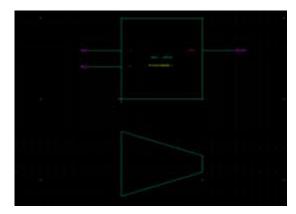
1) Click on path



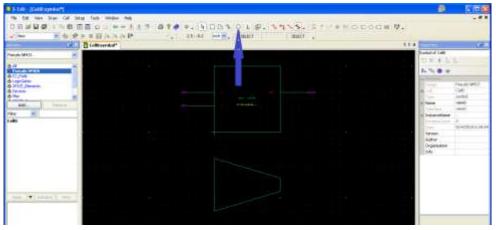
2) Now click on all angle(to draw line at any angle. There are other option as well e.g. draw line at 90 degree angle)

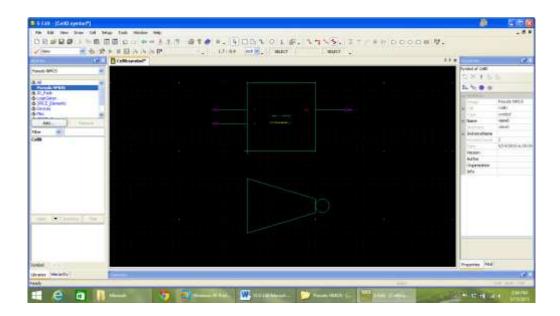
The first control of the first

3) Now draw any sybol shape of your choice. I,II darw NAND gate.

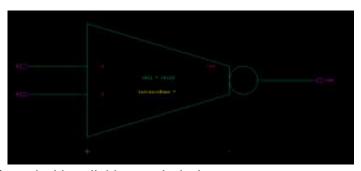


4) Now placing circle(not). Click on circle symbol available at toolbar.

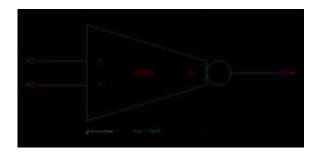




5) Delete automatically generated symbol and place new symbol between input/output ports



6) Type name of symbol by clicking on Label.



LAB:12

5. Task:

Do the following tasks for (i) 2 inputs XOR, (ii) 2 inputs XNOR, (iii) 4 inputs NAND, (iv) 6 inputs NOR Gate, and (v) a full adder circuit on S-Edit

- 1) Schematic Design and testing
- 2) Symbol generation.

LAB:12

	submission Declaration by the Student: submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that: I have performed all the practical work myself I have noted down actual measurements in this write up from my own working I have written un-plagiarized answers to various questions
	I <u>have/have not</u> obtained the desired objectives of the lab. asons of not obtaining objectives (if applicable):
	Student's signature and Date
C +	udent Evaluation by the Lab Engineer:
	e Lab Engineer can separate this page from the writeup and keep it for his/her
	n record. It must be signed by the student with date on it.
	Lab Work: objectives achieved (correctness of measurements, calculations,
	answers to questions posed, conclusion)
	/30
	Lab Writeup: Neatness, appropriateness, intime submission /10
	Troubleshooting: Were the student able to troubleshoot his/her work when it was purposedly changed? /10
	TOTAL:
Fe	edback on student behaviour:
En	circle your choice2 means poorest/worst/extremely inadequate/irrevlevant, 0
giv	es an average score, and +2 means best/most relevant/most adequate.
	Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
	Did the student remain focused on his/her work during lab? -2 -1 0 1 2
	Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
	Did the student cause any distraction during the Lab? -2 -1 0 1 2

VLSI LAB	NUCES, ISLAMABAD	Page 8 of 10
----------	------------------	----------------------------

^o se	udo NMOS Technology on S-Edit	
	Was the student found in any sort of plagiarism? 0 1 2	-2 -1
Ac	dditional comments (if any) by the Lab Engineer:	
	Lab Engineer's signature and Date	
91	udent's feedback: [Separate this page; fill it; drop in the	Dron Boy 1
	Providing feedback for every lab session is optional. No feedba	· -
	satisified	-
	The Lab Committee will consider only duly filled forms submitte after the lab	ed within one week
	This feedabck is for LAB session:	
	LAB Number:,	
	Date:	
	General (to provide feedback on a persistent practice/ocurrence	•
	Your current CGPA is in the range <u>4.00 to 3.00/2.99 to 2.00/1</u> <u>0.00</u>	. <u>99 to 1.00/0.99 to</u>
Th	nis feedback is:	
	For a Particular	
	Who conducted the LAB?	
	Actual Start time:	
	Total Duration of Lab:	
	Instruction Duration:	
	Practical Duration:	r/in I AD/in CLATE
	LAB writeup available before LAB? Yes/No with the Photocopie Had the theory related to lab been covered in theory class? Yes	
		<u>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</u>

NUCES, ISLAMABAD

Page **9** of **10**

VLSI LAB

LAB:12

Symbol generation of basic digital designs using

LAB:12

Encircle your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

	Was duration of instruction session adequate?	-2 -1 0 +1 +2
	How much did you understand about the practical?	-2 -1 0 +1 +2
Instruction Session	How much content was irrelevant to the practical? Did the instructor allowed Q/A and	-2 -1 0 +1 +2
	discussion?	-2 -1 0 +1 +2
Practical	Did you get sufficient time for practical?	-2 -1 0 +1 +2
	Presence in lab at all time?	-2 -1 0 +1 +2
	Ability to convey?	-2 -1 0 +1 +2
Lab	Readiness to help during practical?	-2 -1 0 +1 +2
Engineer	Readiness to discuss theoretical aspects?	-2 -1 0 +1 +2
	Helps in troubleshooting?	-2 -1 0 +1 +2
	Guides hows & whys of troubleshooting?	-2 -1 0 +1 +2
	How friendly was the lab staff?	-2 -1 0 +1 +2
Staff	Presence of staff throughout the lab session?	-2 -1 0 +1 +2
	Impact of availability of staff on your practical?	-2 -1 0 +1 +2
	Performance of Electronic Instruments?	-2 -1 0 +1 +2
Equipment	Performance of Breadboard/experiment kit?	-2 -1 0 +1 +2
_	Performance of circuit components esp. ICs?	-2 -1 0 +1 +2
Overall	Your overall rating for the whole lab session?	-2 -1 0 +1 +2
Other comn	nents:	

VLSI LAB	NUCES, ISLAMABAD	Page 10 of 10
----------	------------------	-----------------------------