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| **VLSI Lab** |
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| **LABORATORY REPORT** |
| **Spring 2019** |

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| **LAB 05** | | | | |
| **Title of Lab Experiment: Implementation and Simulation of Basic Cells Layout using L-Edit** | | | | |
| **Engr. Rashid Karim** | | | | |
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| \_\_\_\_\_\_\_\_\_\_\_\_Kamran\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | \_\_\_\_\_i140420\_\_ | \_A\_ |
| STUDENT NAME | | | ROLL NO | SEC |
| Submission Date: \_\_\_\_\_27/2/19\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | |
| LAB ENGINEER SIGNATURE & DATE | | | | |
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| **MARKS AWARDED:**  /**10** | | | | |
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| **NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), ISLAMABAD** | | | | |
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| **LAB:** | **05** | **Implementation and Simulation of Basic Cells Layout using L-Edit** | | | |

#### **Learning Objectives:**

a. Mask level implementation of all basic cells

b. Functional verification through output/input waveforms.

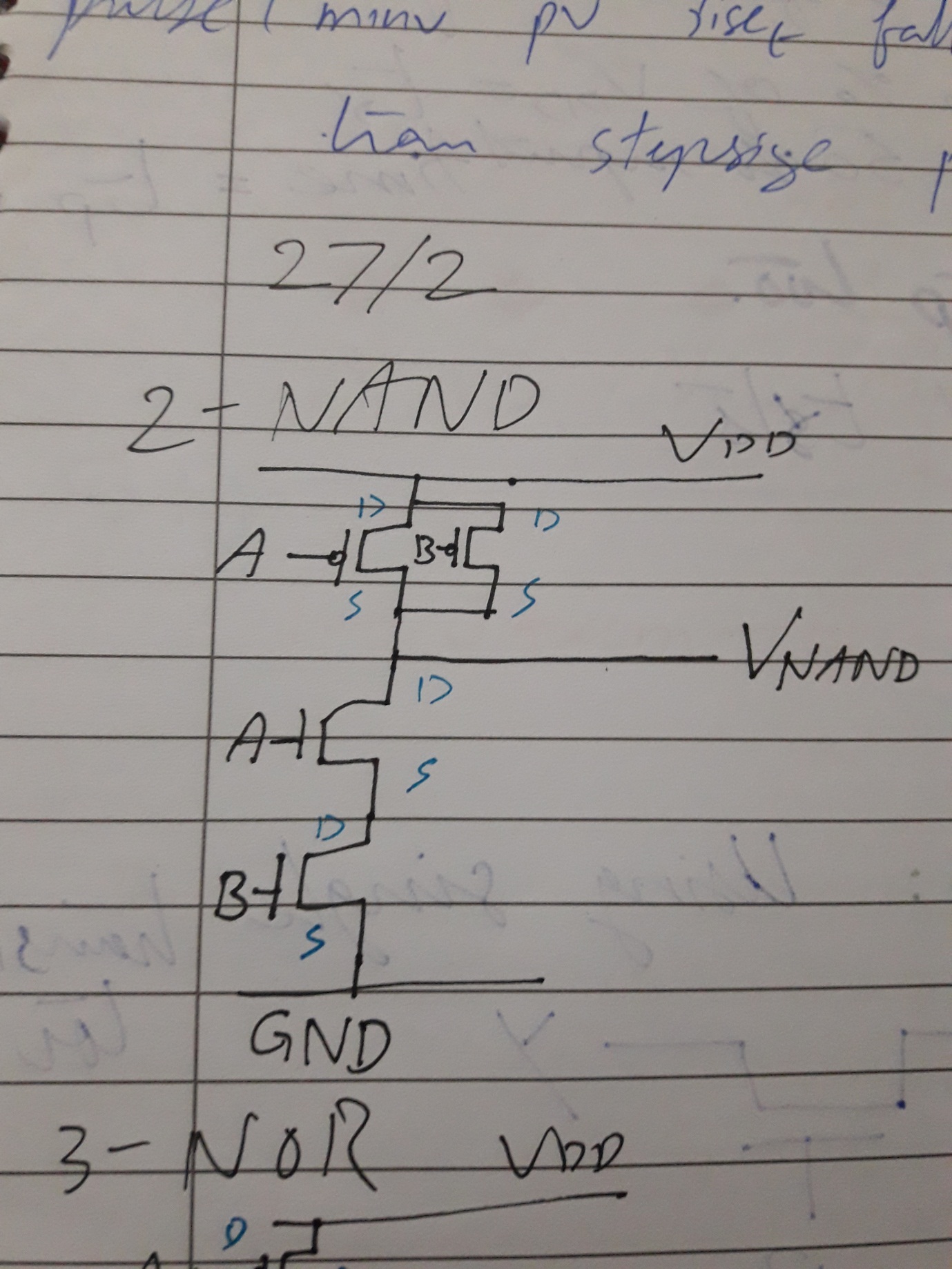
#### **Equipment Required:**

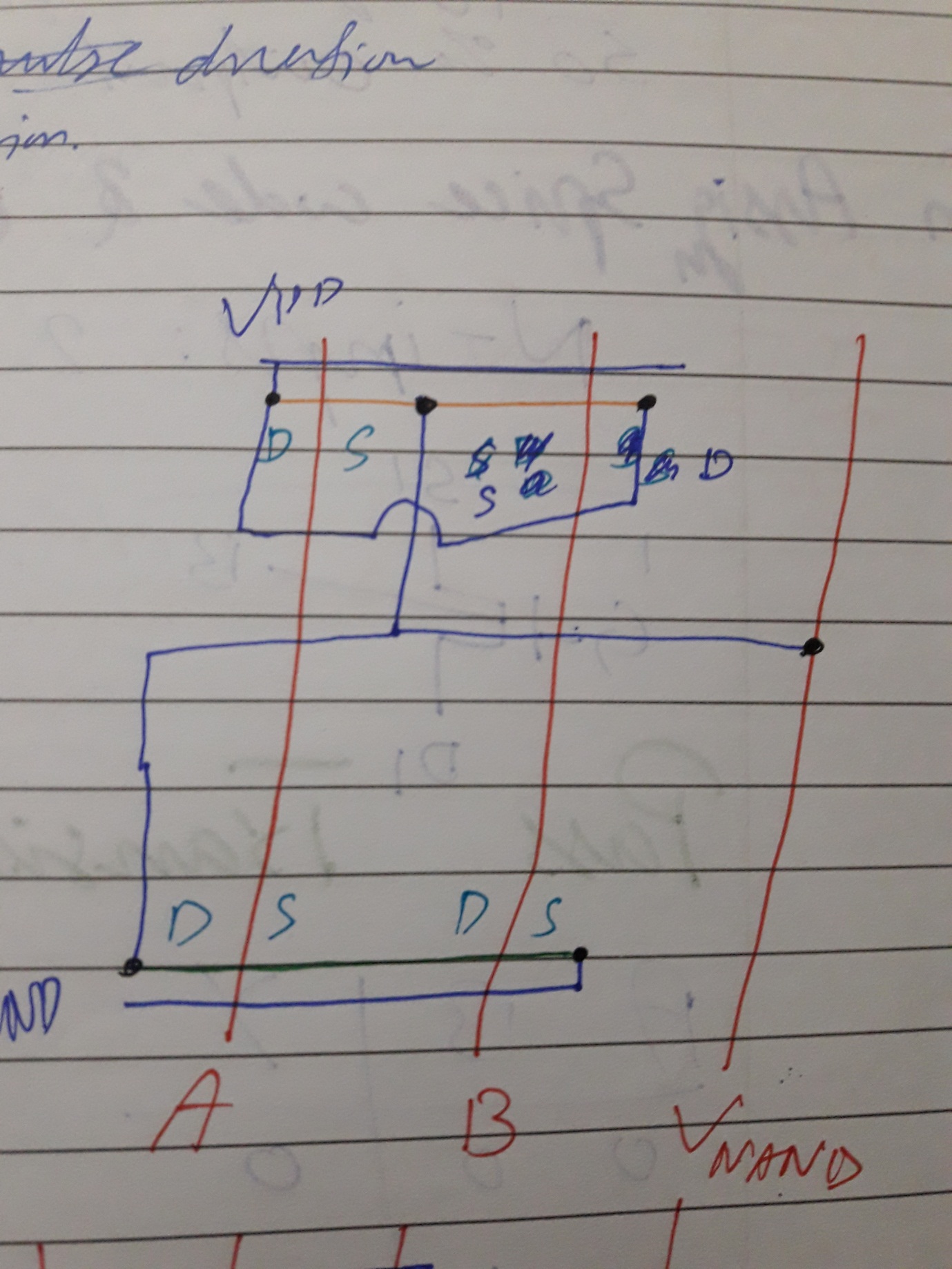
Software : L-Edit , T-Spice, W-Edit

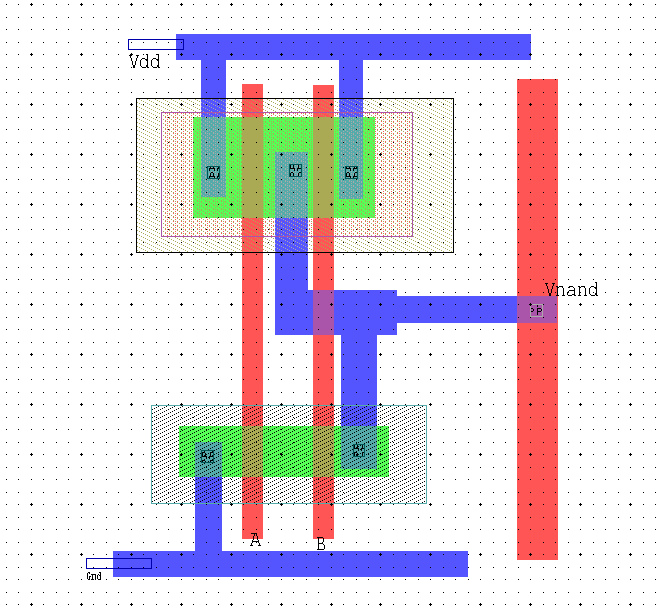
1. Lab Summary:

In this lab,we implemented layout of multiple input gates in L-edit,extracted into a spice file,wrote FORTRAN code in S-edit and simulated using W-edit.

1. Tasks
2. **2 INPUT NAND:**

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**Layout:**

**Spice File Code**

\* Circuit Extracted by Tanner Research's L-Edit Version 13.00 / Extract Version 13.00 ;

\* TDB File: C:\Users\i140420\Desktop\Kamran\_VLSI\_5\L5\_NAND.tdb

\* Cell: Cell0 Version 1.13

\* Extract Definition File: ..\..\Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\Tech\Generic0\_25um\Generic\_025.ext

\* Extract Date and Time: 03/01/2019 - 08:51

.INCLUDE SpecialDevices.md

.lib "C:\Users\i140420\Documents\Tanner EDA\Tanner Tools v13.0\Libraries\Models\Generic\_025.lib" TT

\* NODE NAME ALIASES

\* 1 = Vnand (20.27 , 5.54)

\* 2 = Gnd (11.1 , -0.28)

\* 3 = Vdd (11.95 , 10.1)

M1 Vnand A Vdd 4 PMOS L=400n W=2u AD=1.02p PD=3.02u AS=1.96p PS=5.96u $ (14.22 6.75 14.62 8.75)

M2 Vdd B Vnand 4 PMOS L=400n W=2u AD=1.68p PD=5.68u AS=1.02p PS=3.02u $ (15.64 6.75 16.04 8.75)

M3 6 A Gnd 5 NMOS L=400n W=1u AD=510f PD=2.02u AS=1.26p PS=4.52u $ (14.22 1.56 14.62 2.56)

M4 Vnand B 6 5 NMOS L=400n W=1u AD=1.12p PD=4.24u AS=510f PS=2.02u $ (15.64 1.56 16.04 2.56)

.tran 10n 100n

v1 A Gnd PULSE (0 5 0 1n 1n 10n 20n)

v2 B Gnd PULSE (0 5 5n 1n 1n 10n 20n)

v3 Vdd Gnd 5

.print tran v(Vnand,Gnd) v(A,Gnd) v(B,Gnd)

\* Total Nodes: 8

\* Total Elements: 4

\* Total Number of Shorted Elements not written to the SPICE file: 0

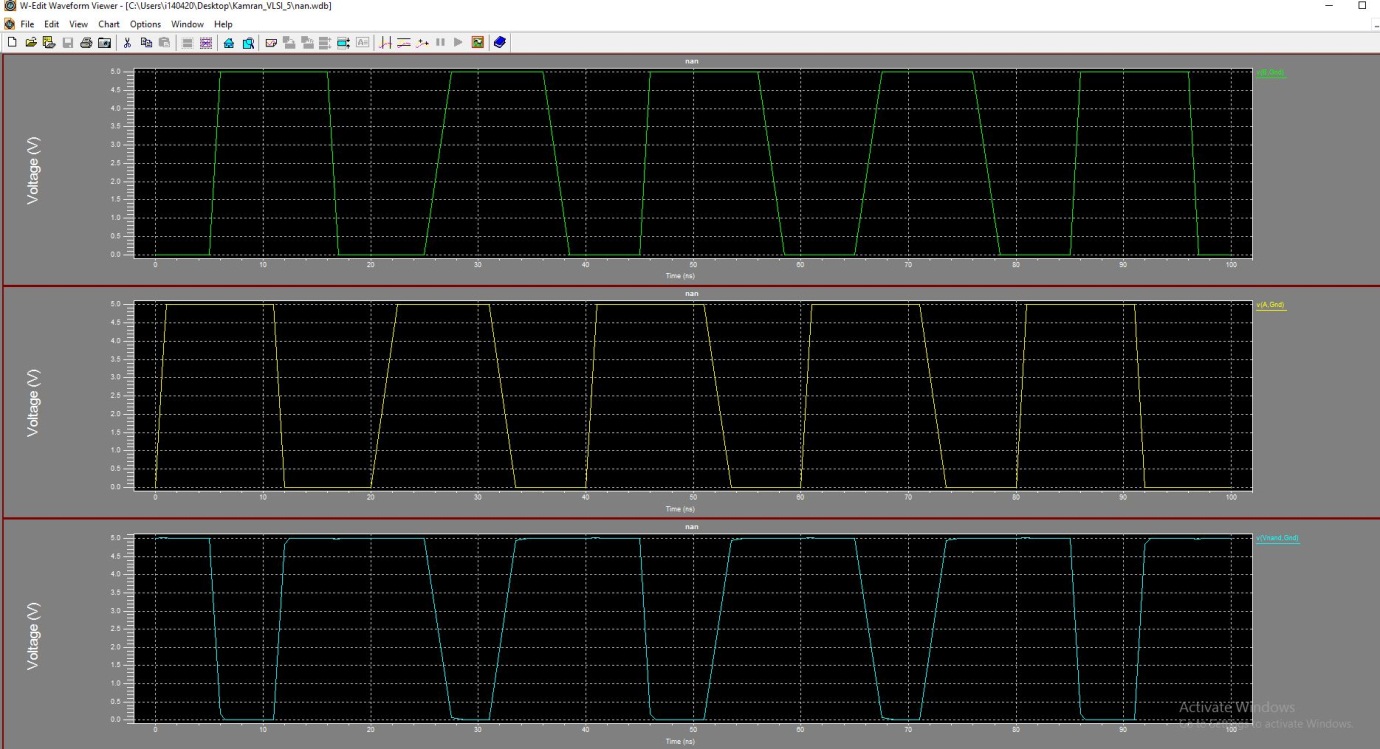
\* Output Generation Elapsed Time: 0.000 sec

\* Total Extract Elapsed Time: 1.293 sec

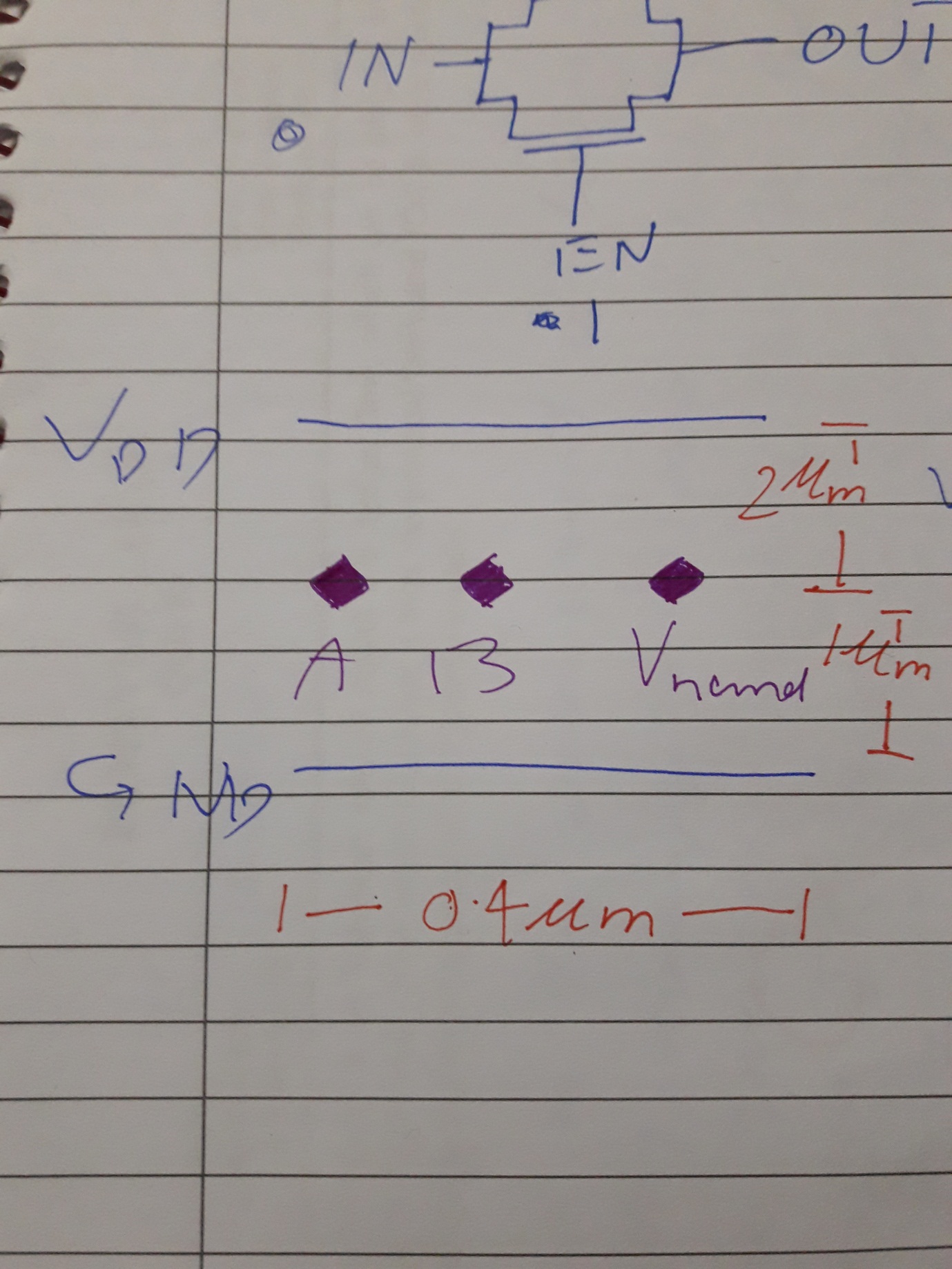
.op

.END

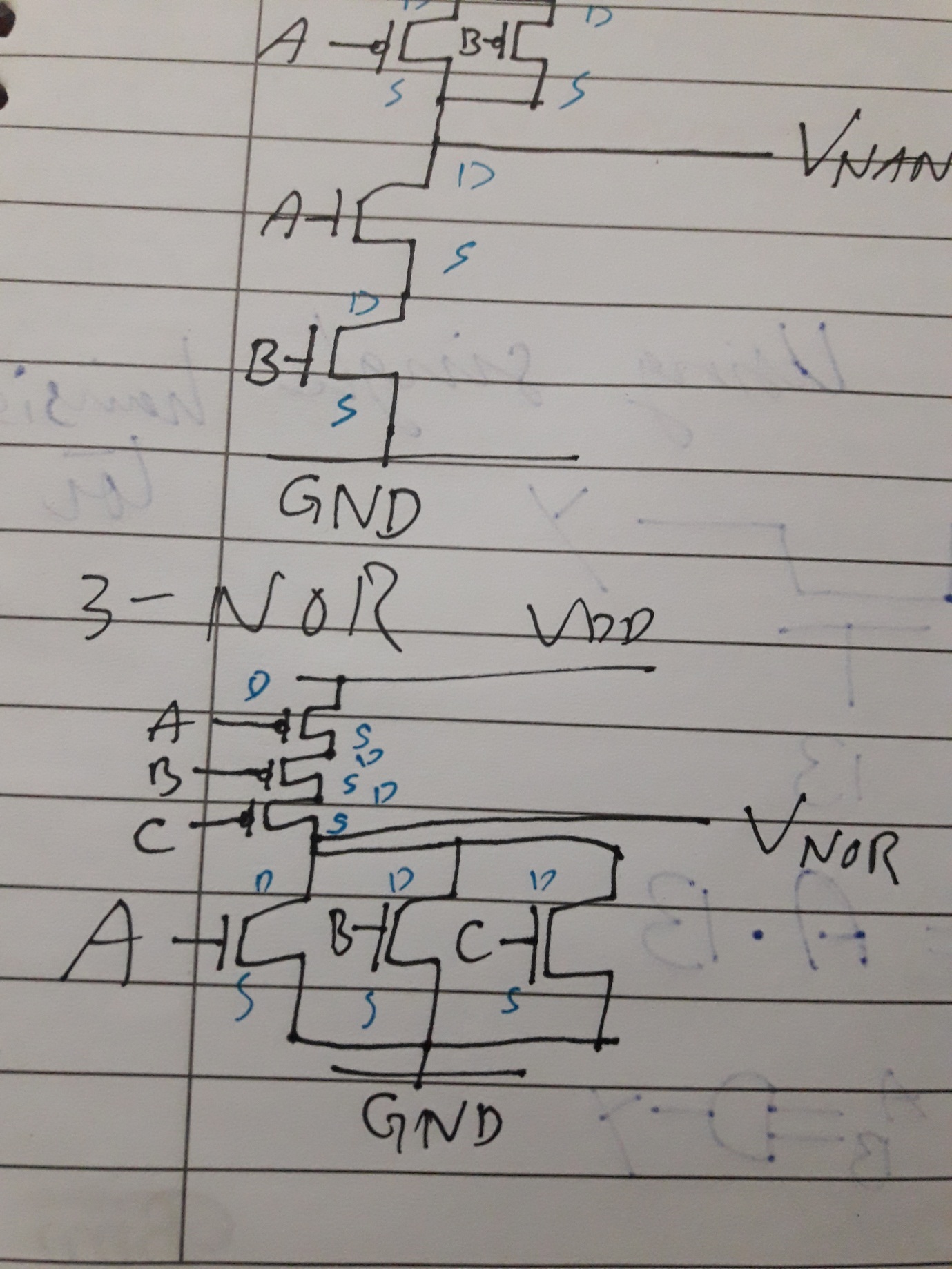
**Simulation Results/Waveforms**

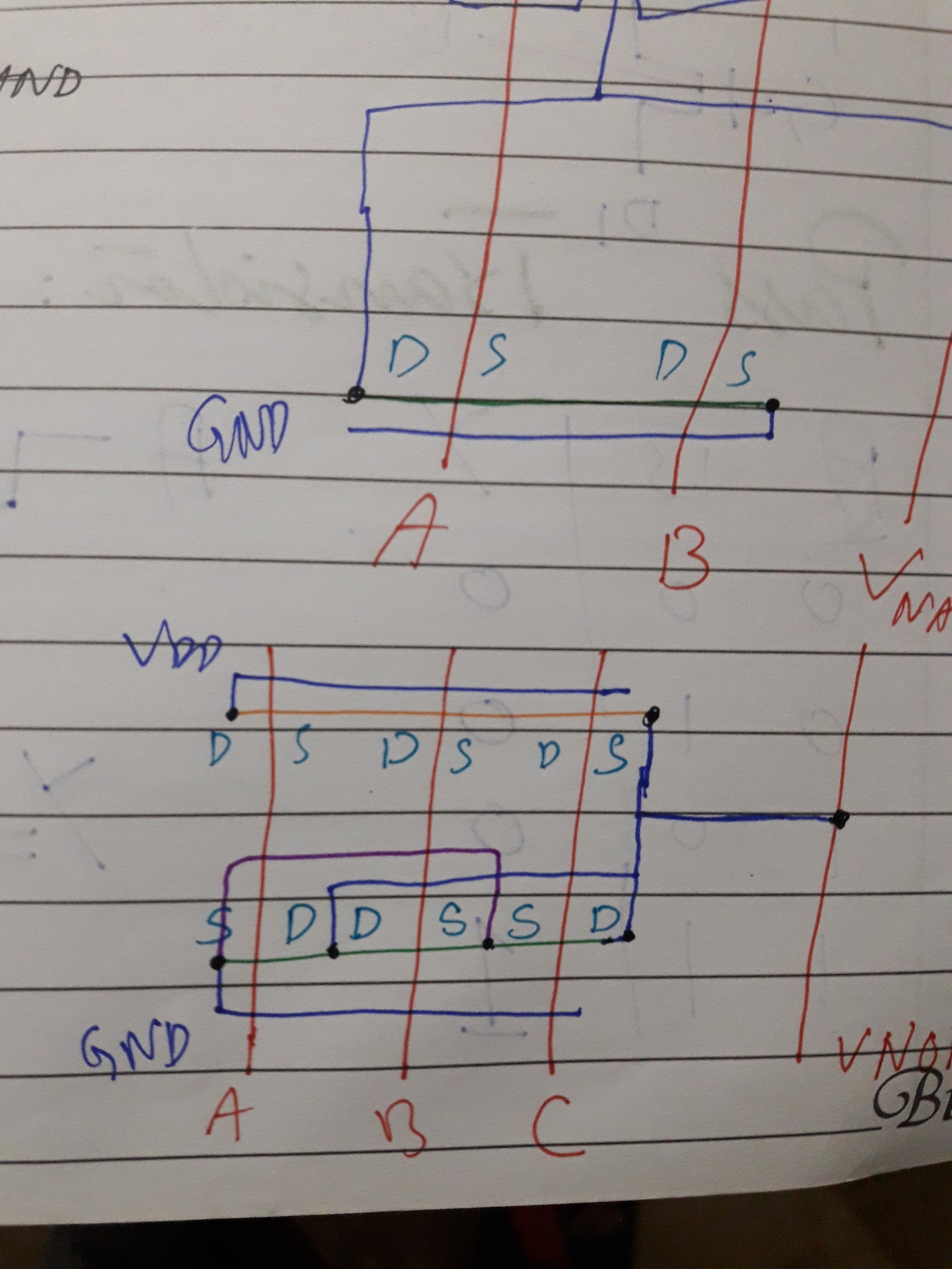
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**Abstract**

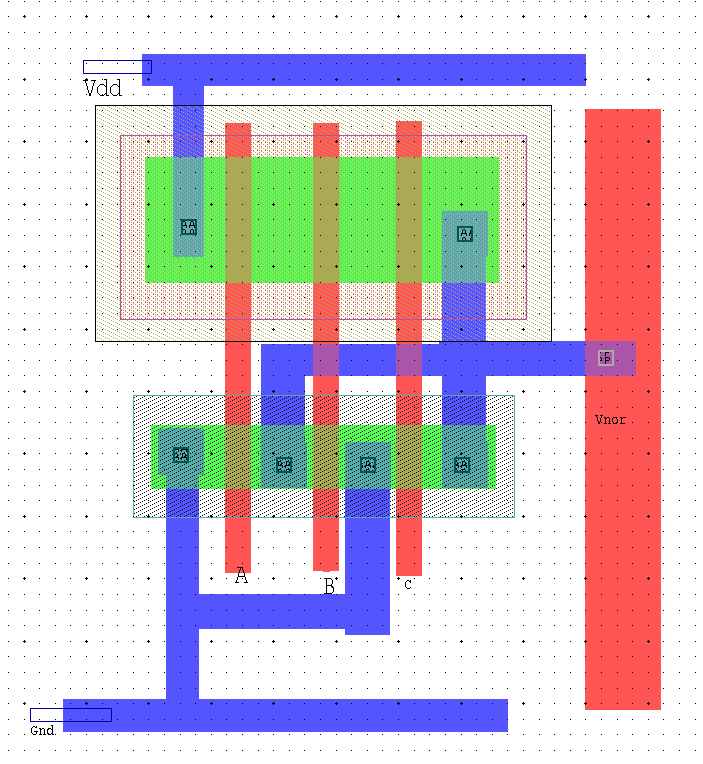
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1. **3 INPUT NOR:**

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**Layout:**



**Spice File Code**

\* Circuit Extracted by Tanner Research's L-Edit Version 13.00 / Extract Version 13.00 ;

\* TDB File: C:\Users\i140420\Desktop\Kamran\_VLSI\_5\L5\_NOR.tdb

\* Cell: Cell0 Version 1.20

\* Extract Definition File: Generic\_025.ext

\* Extract Date and Time: 03/01/2019 - 15:58

\* Extract Date and Time: 03/01/2019 - 08:51

.INCLUDE SpecialDevices.md

.lib "C:\Users\i140420\Desktop\Kamran\_VLSI\_5\Generic\_025\_2.lib" TT

\* NODE NAME ALIASES

\* 1 = Gnd (11.1 , -0.28)

\* 2 = Vnor (20.15 , 4.7)

\* 3 = Vdd (11.95 , 10.1)

\* 8 = C (17.1 , 2.05)

\* 9 = B (15.79 , 2.12)

\* 10 = A (14.39 , 2.29)

M1 Vnor A Gnd 4 NMOS L=400n W=1u AD=510f PD=2.02u AS=1.17p PS=4.34u $ (14.22 3.45 14.62 4.45)

M2 Gnd B Vnor 4 NMOS L=400n W=1u AD=465f PD=1.93u AS=510f PS=2.02u $ (15.64 3.45 16.04 4.45)

M3 Vnor C Gnd 4 NMOS L=400n W=1u AD=1.18p PD=4.36u AS=465f PS=1.93u $ (16.97 3.45 17.37 4.45)

M4 7 A Vdd 5 PMOS L=400n W=2u AD=1.02p PD=3.02u AS=2.56p PS=6.56u $ (14.22 6.75 14.62 8.75)

M5 6 B 7 5 PMOS L=400n W=2u AD=930f PD=2.93u AS=1.02p PS=3.02u $ (15.64 6.75 16.04 8.75)

M6 Vnor C 6 5 PMOS L=400n W=2u AD=2.46p PD=6.46u AS=930f PS=2.93u $ (16.97 6.75 17.37 8.75)

.tran 10n 100n

v1 A Gnd PULSE (0 5 0 1n 1n 10n 20n)

v2 B Gnd PULSE (0 5 5n 1n 1n 10n 20n)

v3 Vdd Gnd 5

.print tran v(Vnand,Gnd) v(A,Gnd) v(B,Gnd)

\* Total Nodes: 10

\* Total Elements: 6

\* Total Number of Shorted Elements not written to the SPICE file: 0

\* Output Generation Elapsed Time: 0.000 sec

\* Total Extract Elapsed Time: 1.027 sec

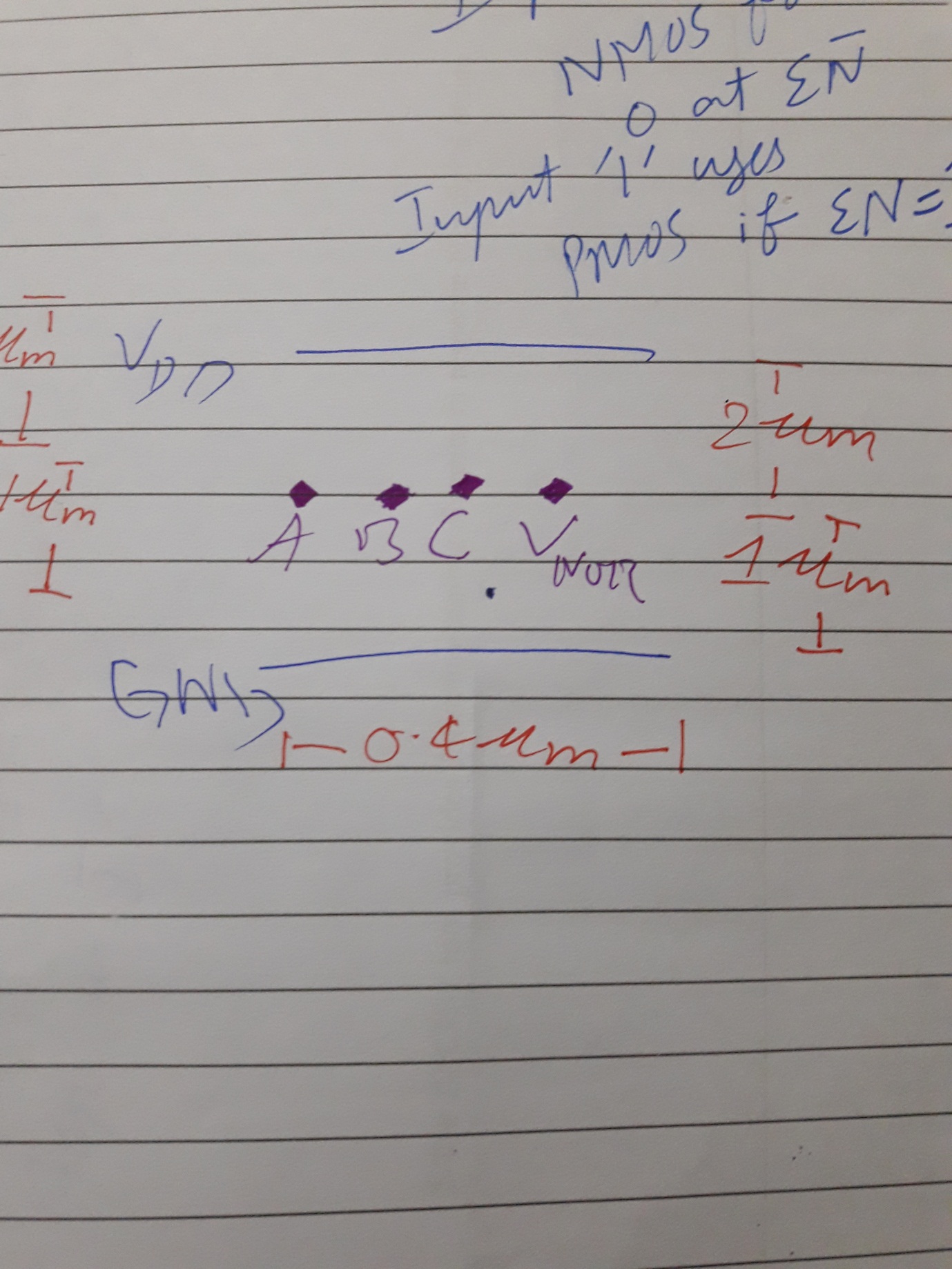
.op

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**Simulation Results/Waveforms**



**Abstract**



**Submission Declaration by the Student:**

In submitting this lab write-up to the Lab Engineer/Instructor, I hereby declare that:

* I have performed all the practical work myself
* I have noted down actual measurements in this writeup from my own working
* I have written un-plagarised answers to various questions
* I have/have not obtained the desired objectives of the lab.

Reasons of not obtaining objectoves (if applicable):

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Student’s signature and Date

**Student Evaluation by the Lab Engineer:**

The Lab Engineer can separate this page from the writeup and keep it for his/her own record. It must be signed by the student with date on it.

* **Lab Work:** objectives achieved (correctness of measurements, calculations, answers to questions posed, conclusion) \_\_\_\_\_\_\_\_/30
* **Lab Writeup:** Neatness, appropriateness, intime submission \_\_\_\_\_\_\_\_/10
* **Troubleshooting:** Were the student able to troubleshoot his/her work when it was purposedly changed? \_\_\_\_\_\_\_\_/10
* **TOTAL:** \_\_\_\_\_\_\_\_/50

**Feedback on student behaviour:**

***Encircle*** your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

* Did the student join the lab at the start/remained in lab? -2 -1 0 1 2
* Did the student remain focused on his/her work during lab? -2 -1 0 1 2
* Rate student's behaviour with fellows/staff/Lab Engineer? -2 -1 0 1 2
* Did the student cause any distraction during the Lab? -2 -1 0 1 2
* Was the student found in any sort of plagiarism? -2 -1 0 1 2

Additional comments (if any) by the Lab Engineer:

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Lab Engineer’s signature and Date

**Student's feedback: [Separate this page; fill it; drop in the Drop Box.]**

* Providing feedback for every lab session is optional. No feedback means you are satisified
* The Lab Committee will consider only duly filled forms submitted within one week after the lab
* This feedabck is for LAB session: LAB Number: \_\_\_\_\_, Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* General (to provide feedback on a persistent practice/ocurrence in LABs).
* Your current CGPA is in the range 4.00 to 3.00/2.99 to 2.00/1.99 to 1.00/0.99 to 0.00

**This feedback is:**

* For a Particular
* Who conducted the LAB? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* Actual Start time: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Total Duration of Lab: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* Instruction Duration: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Practical Duration: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* LAB writeup available before LAB? Yes/No with the Photocopier/in LAB/in SLATE
* Had the theory related to lab been covered in theory class? Yes/No

***Encircle*** your choice. -2 means poorest/worst/extremely inadequate/irrevlevant, 0 gives an average score, and +2 means best/most relevant/most adequate.

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| **Instruction Session** | Was duration of instruction session adequate? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| How much did you understand about the practical? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| How much content was irrelevant to the practical? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Did the instructor allowed Q/A and discussion? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| **Practical** | Did you get sufficient time for practical? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| **Lab**  **Engineer** | Presence in lab at all time? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Ability to convey? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Readiness to help during practical? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Readiness to discuss theoretical aspects? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Helps in troubleshooting? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Guides hows & whys of troubleshooting? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| **Staff** | How friendly was the lab staff? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Presence of staff throughout the lab session? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Impact of availability of staff on your practical? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| **Equipment** | Performance of Electronic Instruments? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Performance of Breadboard/experiment kit? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| Performance of circuit components esp. ICs? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |
| **Overall** | Your overall rating for the whole lab session? | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **-2** | **-1** | **0** | **+1** | **+2** | |

Other comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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